

## Features

- Fast Read Access Time – 70 ns
- Automatic Page Write Operation
  - Internal Address and Data Latches for 64 Bytes
  - Internal Control Timer
- Fast Write Cycle Times
  - Page Write Cycle Time: 3 ms or 10 ms Maximum
  - 1 to 64-byte Page Write Operation
- Low Power Dissipation
  - 80 mA Active Current
  - 3 mA Standby Current
- Hardware and Software Data Protection
- $\overline{\text{DATA}}$  Polling for End of Write Detection
- High Reliability CMOS Technology
  - Endurance:  $10^4$  or  $10^5$  Cycles
  - Data Retention: 10 Years
- Single  $5\text{V} \pm 10\%$  Supply
- CMOS and TTL Compatible Inputs and Outputs
- JEDEC Approved Byte-wide Pinout
- Full Military, Commercial, and Industrial Temperature Ranges

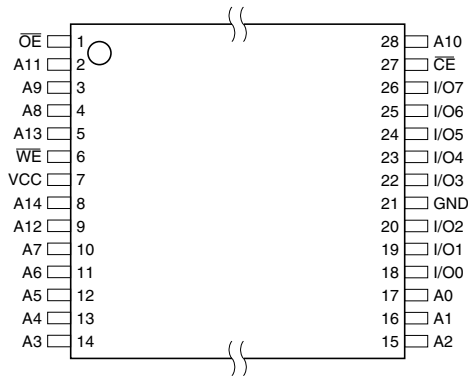
## Description

The AT28HC256 is a high-performance electrically erasable and programmable read only memory. Its 256K of memory is organized as 32,768 words by 8 bits. Manufactured with Atmel's advanced nonvolatile CMOS technology, the AT28HC256 offers *(continued)*

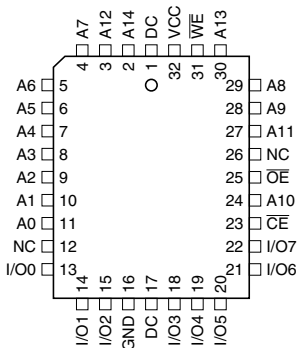
## Pin Configurations

Pin Name	Function
A0 - A14	Addresses
$\overline{\text{CE}}$	Chip Enable
$\overline{\text{OE}}$	Output Enable
$\overline{\text{WE}}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
NC	No Connect
DC	Don't Connect

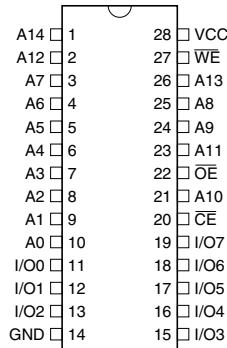
TSOP  
Top View



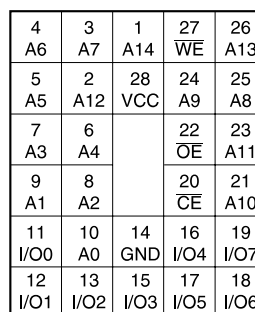
LCC, PLCC  
Top View



CERDIP, PDIP, FLATPACK  
Top View



PGA  
Top View



Note: PLCC package pins 1 and 17 are DON'T CONNECT.



# 256 (32K x 8) High-speed Parallel EEPROM

## AT28HC256



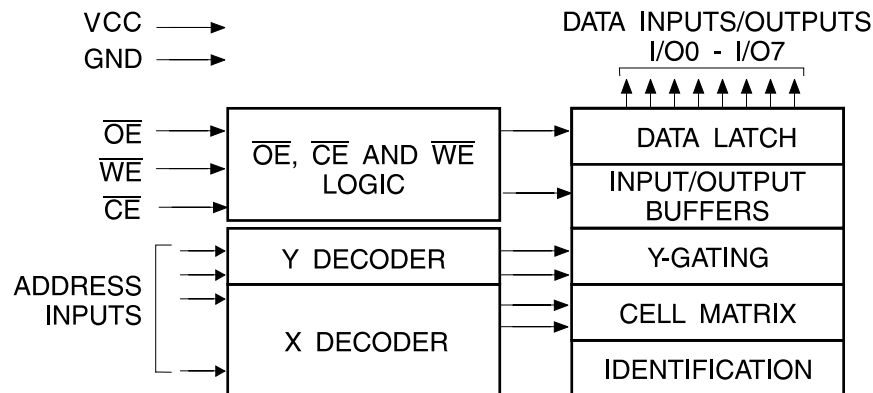
access times to 70 ns with power dissipation of just 440 mW. When the AT28HC256 is deselected, the standby current is less than 5 mA.

The AT28HC256 is accessed like a Static RAM for the read or write cycle without the need for external components. The device contains a 64-byte page register to allow writing of up to 64 bytes simultaneously. During a write cycle, the address and 1 to 64 bytes of data are internally latched, freeing the addresses and data bus for other operations. Following the initiation of a write cycle, the device will automatically write the latched data using an internal control

timer. The end of a write cycle can be detected by  $\overline{\text{DATA}}$  Polling of I/O<sub>7</sub>. Once the end of a write cycle has been detected a new access for a read or write can begin.

Atmel's 28HC256 has additional features to ensure high quality and manufacturability. The device utilizes internal error correction for extended endurance and improved data retention characteristics. An optional software data protection mechanism is available to guard against inadvertent writes. The device also includes an extra 64 bytes of EEPROM for device identification or tracking.

## Block Diagram



## Absolute Maximum Ratings\*

Temperature under Bias .....	-55°C to +125°C
Storage Temperature .....	-65°C to +150°C
All Input Voltages (including NC Pins) with Respect to Ground .....	-0.6V to +6.25V
All Output Voltages with Respect to Ground .....	-0.6V to $V_{CC} + 0.6V$
Voltage on $\overline{\text{OE}}$ and A9 with Respect to Ground .....	-0.6V to +13.5V

\*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

## Device Operation

**READ:** The AT28HC256 is accessed like a Static RAM. When  $\overline{CE}$  and  $\overline{OE}$  are low and  $\overline{WE}$  is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in the high impedance state when either  $\overline{CE}$  or  $\overline{OE}$  is high. This dual-line control gives designers flexibility in preventing bus contention in their system.

**BYTE WRITE:** A low pulse on the  $\overline{WE}$  or  $\overline{CE}$  input with  $\overline{CE}$  or  $\overline{WE}$  low (respectively) and  $\overline{OE}$  high initiates a write cycle. The address is latched on the falling edge of  $\overline{CE}$  or  $\overline{WE}$ , whichever occurs last. The data is latched by the first rising edge of  $\overline{CE}$  or  $\overline{WE}$ . Once a byte write has been started it will automatically time itself to completion. Once a programming operation has been initiated and for the duration of  $t_{WC}$ , a read operation will effectively be a polling operation.

**PAGE WRITE:** The page write operation of the AT28HC256 allows 1 to 64 bytes of data to be written into the device during a single internal programming period. A page write operation is initiated in the same manner as a byte write; the first byte written can then be followed by 1 to 63 additional bytes. Each successive byte must be written within  $150 \mu s$  ( $t_{BLC}$ ) of the previous byte. If the  $t_{BLC}$  limit is exceeded the AT28HC256 will cease accepting data and commence the internal programming operation. All bytes during a page write operation must reside on the same page as defined by the state of the A6 - A14 inputs. That is, for each  $\overline{WE}$  high to low transition during the page write operation, A6 - A14 must be the same.

The A0 to A5 inputs are used to specify which bytes within the page are to be written. The bytes may be loaded in any order and may be altered within the same load period. Only bytes which are specified for writing will be written; unnecessary cycling of other bytes within the page does not occur.

**DATA POLLING:** The AT28HC256 features  $\overline{DATA}$  Polling to indicate the end of a write cycle. During a byte or page write cycle an attempted read of the last byte written will result in the complement of the written data to be presented on I/O<sub>7</sub>. Once the write cycle has been completed, true data is valid on all outputs, and the next write cycle may begin.  $\overline{DATA}$  Polling may begin at anytime during the write cycle.

**TOGGLE BIT:** In addition to  $\overline{DATA}$  Polling the AT28HC256 provides another method for determining the end of a write cycle. During the write operation, successive attempts to read data from the device will result in I/O<sub>6</sub> toggling between one and zero. Once the write has completed, I/O<sub>6</sub> will stop toggling and valid data will be read. Testing the toggle bit may begin at any time during the write cycle.

**DATA PROTECTION:** If precautions are not taken, inadvertent writes to any 5-volt-only nonvolatile memory may

occur during transition of the host system power supply. Atmel has incorporated both hardware and software features that will protect the memory against inadvertent writes.

**HARDWARE PROTECTION:** Hardware features protect against inadvertent writes to the AT28HC256 in the following ways: (a)  $V_{CC}$  sense – if  $V_{CC}$  is below 3.8V (typical) the write function is inhibited; (b)  $V_{CC}$  power-on delay – once  $V_{CC}$  has reached 3.8V the device will automatically time out 5 ms (typical) before allowing a write; (c) write inhibit – holding any one of  $\overline{OE}$  low,  $\overline{CE}$  high or  $\overline{WE}$  high inhibits write cycles; and (d) noise filter – pulses of less than 15 ns (typical) on the  $\overline{WE}$  or  $\overline{CE}$  inputs will not initiate a write cycle.

**SOFTWARE DATA PROTECTION:** A software controlled data protection feature has been implemented on the AT28HC256. When enabled, the software data protection (SDP), will prevent inadvertent writes. The SDP feature may be enabled or disabled by the user; the AT28HC256 is shipped from Atmel with SDP disabled.

SDP is enabled by the host system issuing a series of three write commands; three specific bytes of data are written to three specific addresses (refer to “Software Data Protection” algorithm). After writing the 3-byte command sequence and after  $t_{WC}$  the entire AT28HC256 will be protected against inadvertent write operations. It should be noted, that once protected the host may still perform a byte or page write to the AT28HC256. This is done by preceding the data to be written by the same 3-byte command sequence.

Once set, SDP will remain active unless the disable command sequence is issued. Power transitions do not disable SDP and SDP will protect the AT28HC256 during power-up and power-down conditions. All command sequences must conform to the page write timing specifications. It should also be noted that the data in the enable and disable command sequences is not written to the device and the memory addresses used in the sequence may be written with data in either a byte or page write operation.

After setting SDP, any attempt to write to the device without the three byte command sequence will start the internal write timers. No data will be written to the device; however, for the duration of  $t_{WC}$ , read operations will effectively be polling operations.

**DEVICE IDENTIFICATION:** An extra 64 bytes of EEPROM memory are available to the user for device identification. By raising A9 to  $12V \pm 0.5V$  and using address locations 7FC0H to 7FFFH the additional bytes may be written to or read from in the same manner as the regular memory array.

**OPTIONAL CHIP ERASE MODE:** The entire device can be erased using a 6-byte software code. Please see “Software Chip Erase” application note for details.



## DC and AC Operating Range

		AT28HC256-70	AT28HC256-90	AT28HC256-12
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
	Mil.		-55°C - 125°C	-55°C - 125°C
V <sub>CC</sub> Power Supply		5V ± 10%	5V ± 10%	5V ± 10%

## Operating Modes

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
Read	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IH</sub>	D <sub>OUT</sub>
Write <sup>(2)</sup>	V <sub>IL</sub>	V <sub>IH</sub>	V <sub>IL</sub>	D <sub>IN</sub>
Standby/Write Inhibit	V <sub>IH</sub>	X <sup>(1)</sup>	X	High Z
Write Inhibit	X	X	V <sub>IH</sub>	
Write Inhibit	X	V <sub>IL</sub>	X	
Output Disable	X	V <sub>IH</sub>	X	High Z
Chip Erase	V <sub>IL</sub>	V <sub>H</sub> <sup>(3)</sup>	V <sub>IL</sub>	High Z

- Notes: 1. X can be V<sub>IL</sub> or V<sub>IH</sub>.  
 2. Refer to AC programming waveforms.  
 3. V<sub>H</sub> = 12.0V ± 0.5V.

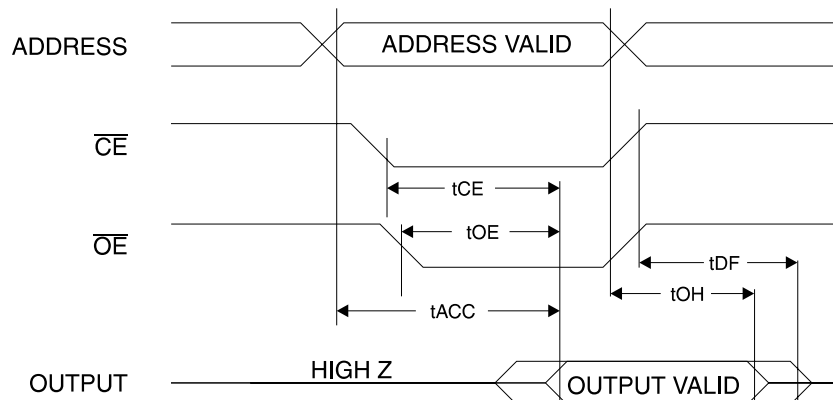
## DC Characteristics

Symbol	Parameter	Condition	Min	Max	Units
I <sub>LI</sub>	Input Load Current	V <sub>IN</sub> = 0V to V <sub>CC</sub> + 1V		10	μA
I <sub>LO</sub>	Output Leakage Current	V <sub>I/O</sub> = 0V to V <sub>CC</sub>		10	μA
I <sub>SB1</sub>	V <sub>CC</sub> Standby Current TTL	$\overline{CE} = 2.0V$ to V <sub>CC</sub>	AT28HC256-90, -12	3	mA
			AT28HC256-70	60	mA
I <sub>SB2</sub>	V <sub>CC</sub> Standby Current CMOS	$\overline{CE} = V_{CC} - 0.3V$ to V <sub>CC</sub>	AT28HC256-90, -12	300	μA
I <sub>CC</sub>	V <sub>CC</sub> Active Current	f = 5 MHz; I <sub>OUT</sub> = 0 mA		80	mA
V <sub>IL</sub>	Input Low Voltage			0.8	V
V <sub>IH</sub>	Input High Voltage		2.0		V
V <sub>OL</sub>	Output Low Voltage	I <sub>OL</sub> = 6.0 mA		0.45	V
V <sub>OH</sub>	Output High Voltage	I <sub>OH</sub> = -4 mA	2.4		V

## AC Read Characteristics

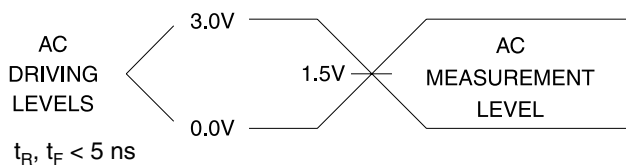
Symbol	Parameter	AT28HC256-70		AT28C256-90		AT28HC256-12		Units
		Min	Max	Min	Max	Min	Max	
$t_{ACC}$	Address to Output Delay		70		90		120	ns
$t_{CE}^{(1)}$	$\overline{CE}$ to Output Delay		70		90		120	ns
$t_{OE}^{(2)}$	$\overline{OE}$ to Output Delay	0	35	0	40	0	50	ns
$t_{DF}^{(3)(4)}$	$\overline{CE}$ or $\overline{OE}$ to Output Float	0	35	0	40	0	50	ns
$t_{OH}$	Output Hold from $\overline{OE}$ , $\overline{CE}$ or Address, whichever occurred first	0		0		0		ns

## AC Read Waveforms<sup>(1)(2)(3)(4)</sup>

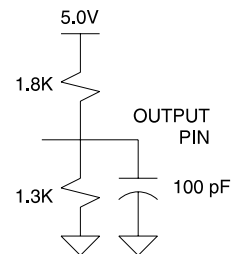


- Notes:
- $\overline{CE}$  may be delayed up to  $t_{ACC} - t_{CE}$  after the address transition without impact on  $t_{ACC}$ .
  - $\overline{OE}$  may be delayed up to  $t_{CE} - t_{OE}$  after the falling edge of  $\overline{CE}$  without impact on  $t_{CE}$  or by  $t_{ACC} - t_{OE}$  after an address change without impact on  $t_{ACC}$ .
  - $t_{DF}$  is specified from  $\overline{OE}$  or  $\overline{CE}$  whichever occurs first ( $C_L = 5$  pF).
  - This parameter is characterized and is not 100% tested.

## Input Test Waveforms and Measurement Level



## Output Test Load



## Pin Capacitance

$f = 1$  MHz,  $T = 25^\circ\text{C}^{(1)}$

Symbol	Typ	Max	Units	Conditions
$C_{IN}$	4	6	pF	$V_{IN} = 0V$
$C_{OUT}$	8	12	pF	$V_{OUT} = 0V$

Note: 1. This parameter is characterized and is not 100% tested.

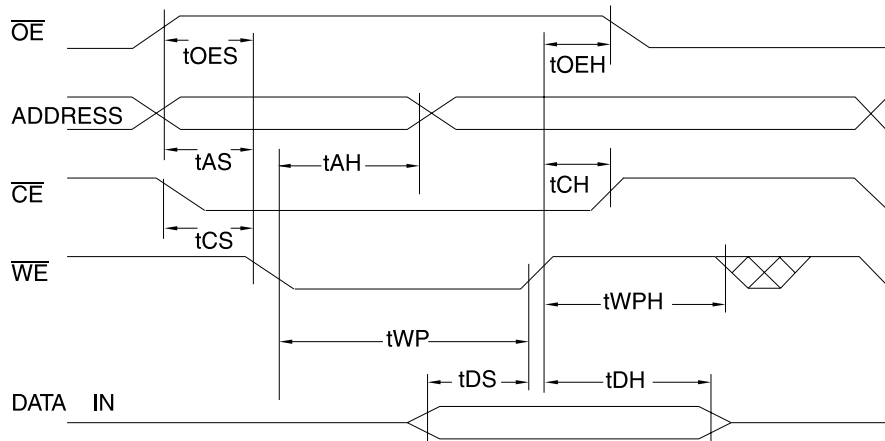
## AC Write Characteristics

Symbol	Parameter	Min	Max	Units
$t_{AS}, t_{OES}$	Address, $\overline{OE}$ Setup Time	0		ns
$t_{AH}$	Address Hold Time	50		ns
$t_{CS}$	Chip Select Setup Time	0		ns
$t_{CH}$	Chip Select Hold Time	0		ns
$t_{WP}$	Write Pulse Width ( $\overline{WE}$ or $\overline{CE}$ )	100		ns
$t_{DS}$	Data Setup Time	50		ns
$t_{DH}, t_{OEH}$	Data, $\overline{OE}$ Hold Time	0		ns
$t_{DV}$	Time to Data Valid	NR <sup>(1)</sup>		

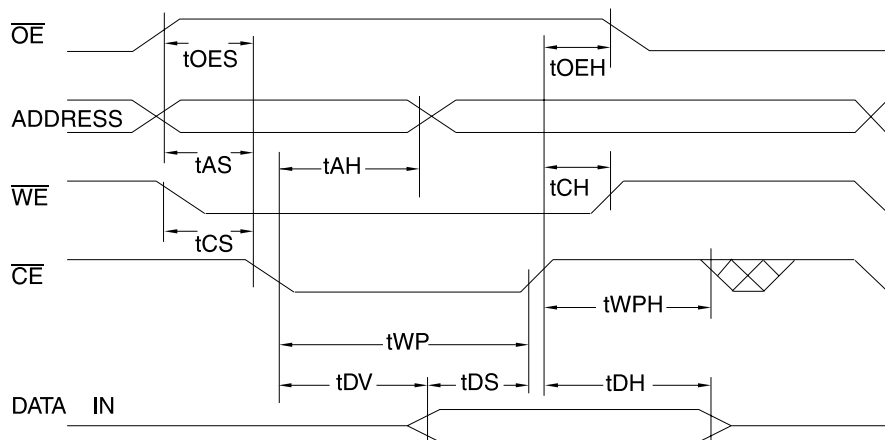
Note: 1. NR = No Restriction.

## AC Write Waveforms

### $\overline{WE}$ Controlled



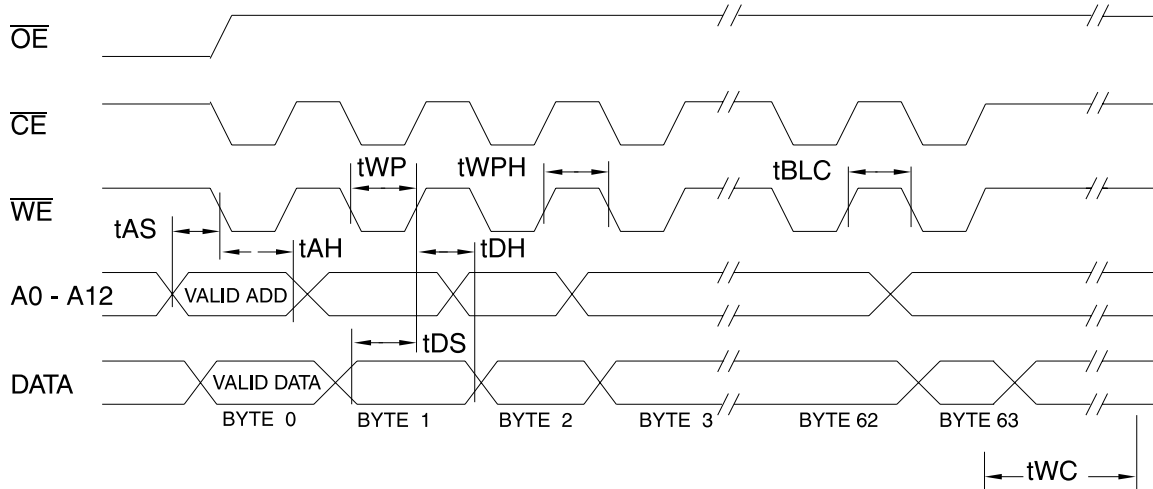
### $\overline{CE}$ Controlled



## Page Mode Write Characteristics

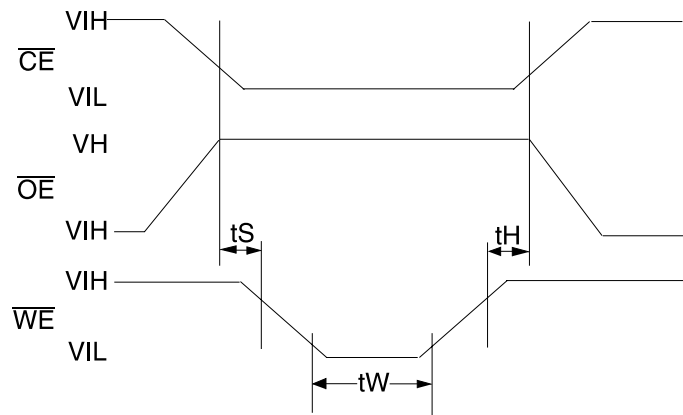
Symbol	Parameter	Min	Typ	Max	Units
$t_{WC}$	Write Cycle Time (option available)	AT28HC256	5	10	ms
		AT28HC256F		2	3
$t_{AS}$	Address Setup Time	0			ns
$t_{AH}$	Address Hold Time	50			ns
$t_{DS}$	Data Setup Time	50			ns
$t_{DH}$	Data Hold Time	0			ns
$t_{WP}$	Write Pulse Width	100			ns
$t_{BLC}$	Byte Load Cycle Time			150	$\mu$ s
$t_{WPH}$	Write Pulse Width High	50			ns

## Page Mode Write Waveforms<sup>(1)(2)</sup>



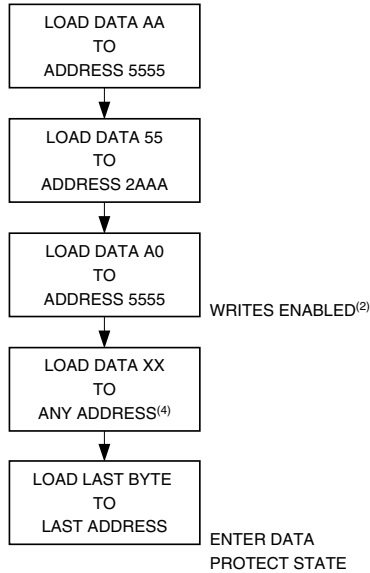
- Notes:
1. A6 through A14 must specify the same page address during each high to low transition of  $\overline{WE}$  (or  $\overline{CE}$ ).
  2.  $\overline{OE}$  must be high only when  $\overline{WE}$  and  $\overline{CE}$  are both low.

## Chip Erase Waveforms

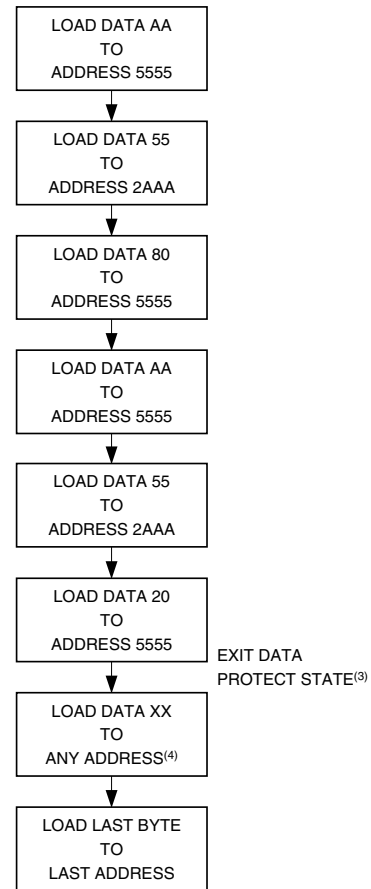


$t_S = t_H = 5 \mu\text{sec (min.)}$   
 $t_W = 10 \text{ msec (min.)}$   
 $V_H = 12.0V \pm 0.5V$

## Software Data Protection Enable Algorithm<sup>(1)</sup>



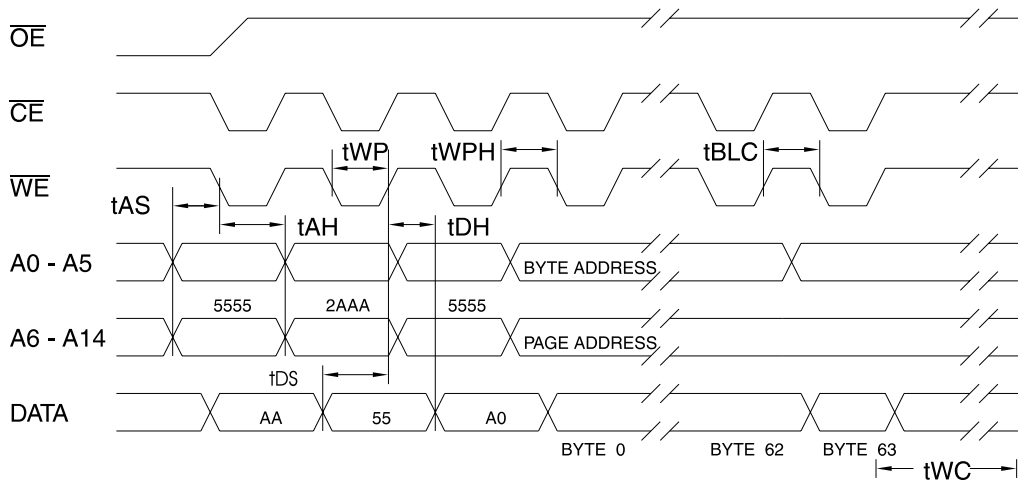
## Software Data Protection Disable Algorithm<sup>(1)</sup>



Notes for software program code:

1. Data Format: I/O7 - I/O0 (Hex);  
Address Format: A14 - A0 (Hex).
2. Write Protect state will be activated at end of write even if no other data is loaded.
3. Write Protect state will be deactivated at end of write period even if no other data is loaded.
4. 1 to 64 bytes of data are loaded.

## Software Protected Write Cycle Waveforms<sup>(1)(2)</sup>



- Notes:
1. A6 through A14 must specify the same page address during each high to low transition of  $\overline{WE}$  (or  $\overline{CE}$ ) after the software code has been entered.
  2.  $\overline{OE}$  must be high only when  $\overline{WE}$  and  $\overline{CE}$  are both low.

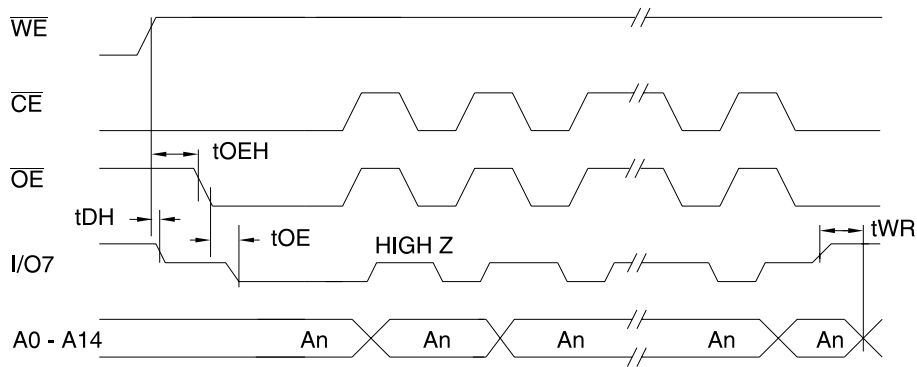


### Data Polling Characteristics<sup>(1)</sup>

Symbol	Parameter	Min	Typ	Max	Units
$t_{DH}$	Data Hold Time	0			ns
$t_{OE\overline{H}}$	$\overline{OE}$ Hold Time	0			ns
$t_{OE}$	$\overline{OE}$ to Output Delay <sup>(2)</sup>				ns
$t_{WR}$	Write Recovery Time	0			ns

Notes: 1. These parameters are characterized and not 100% tested.  
 2. See “AC Read Characteristics” on page 5.

### Data Polling Waveforms

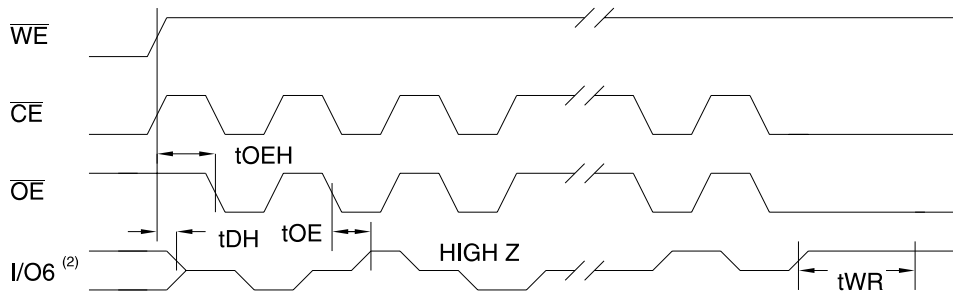


### Toggle Bit Characteristics<sup>(1)</sup>

Symbol	Parameter	Min	Typ	Max	Units
$t_{DH}$	Data Hold Time	10			ns
$t_{OE\overline{H}}$	$\overline{OE}$ Hold Time	10			ns
$t_{OE}$	$\overline{OE}$ to Output Delay <sup>(2)</sup>				ns
$t_{OEHP}$	$\overline{OE}$ High Pulse	150			ns
$t_{WR}$	Write Recovery Time	0			ns

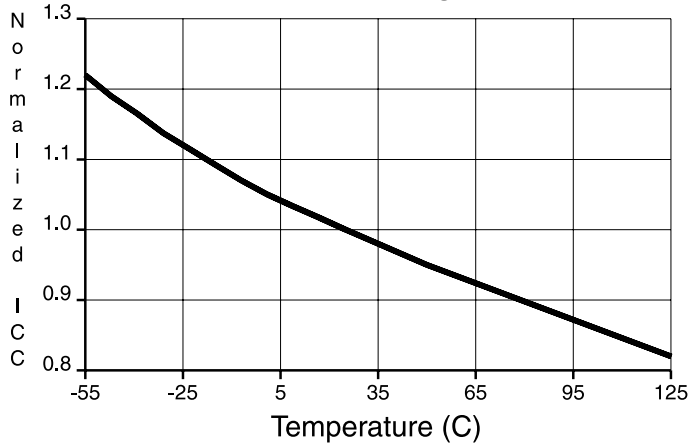
Notes: 1. These parameters are characterized and not 100% tested.  
 2. See “AC Read Characteristics” on page 5.

### Toggle Bit Waveforms

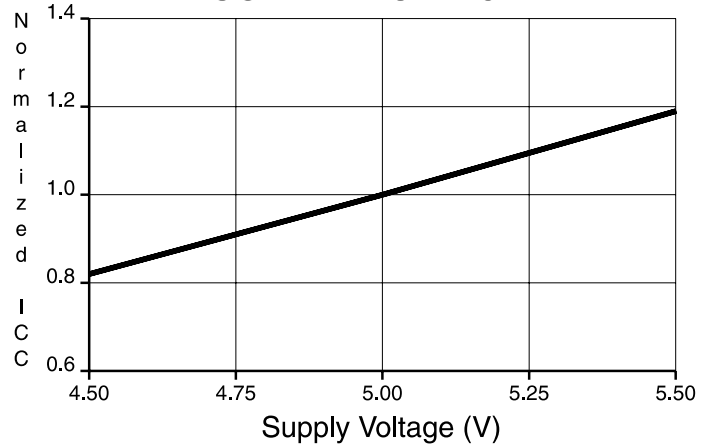


Notes: 1. Toggling either  $\overline{OE}$  or  $\overline{CE}$  or both  $\overline{OE}$  and  $\overline{CE}$  will operate toggle bit.  
 2. Beginning and ending state of I/O6 will vary.  
 3. Any address location may be used but the address should not vary.

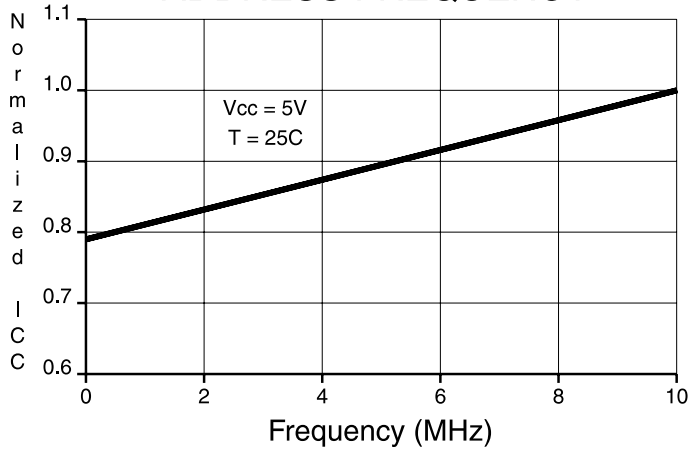
NORMALIZED SUPPLY CURRENT vs. TEMPERATURE



NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



NORMALIZED SUPPLY CURRENT vs. ADDRESS FREQUENCY



## Ordering Information<sup>(1)</sup>

t <sub>ACC</sub> (ns)	I <sub>CC</sub> (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
70	80	60	AT28HC256(E,F)-70JC AT28HC256(E,F)-70PC	32J 28P6	Commercial (0°C to 70°C)
		0.3	AT28HC256(E,F)-70JI AT28HC256(E,F)-70PI	32J 28P6	Industrial (-40°C to 85°C)
90	80	0.3	AT28HC256(E,F)-90JC AT28HC256(E,F)-90PC	32J 28P6	Commercial (0°C to 70°C)
			AT28HC256(E,F)-90JI AT28HC256(E,F)-90PI	32J 28P6	Industrial (-40°C to 85°C)
	80	0.3	AT28HC256(E,F)-90DM/883 AT28HC256(E,F)-90FM/883 AT28HC256(E,F)-90LM/883 AT28HC256(E,F)-90UM/883	28D6 28F 32L 28U	Military/883C Class B, Fully Compliant (-55°C to 125°C)
120	80	0.3	AT28HC256(E,F)-12JC AT28HC256(E,F)-12PC AT28HC256(E,F)-12SC AT28HC256(E,F)-12TC	32J 28P6 28S 28T	Commercial (0°C to 70°C)
			80	0.3	AT28HC256(E,F)-12JI AT28HC256(E,F)-12PI AT28HC256(E,F)-12SI AT28HC256(E,F)-12TI
	80	0.3	AT28HC256(E,F)-12DM/883 AT28HC256(E,F)-12FM/883 AT28HC256(E,F)-12LM/883 AT28HC256(E,F)-12UM/883	28D6 28F 32L 28U	Military/883C Class B, Fully Compliant (-55°C to 125°C)

Package Type	
<b>28D6</b>	28-lead, 0.600" Wide, Non-windowed, Ceramic Dual Inline Package (Cerdip)
<b>28F</b>	28-lead, Non-windowed, Ceramic Bottom-brazed Flat Package (Flatpack)
<b>32J</b>	32-lead, Plastic J-leaded Chip Carrier (PLCC)
<b>32L</b>	32-pad, Non-windowed, Ceramic Leadless Chip Carrier (LCC)
<b>28P6</b>	28-lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
<b>28S</b>	28-lead, 0.300" Wide Plastic Gull Wing Small Outline (SOIC)
<b>28T</b>	28-lead, Plastic Thin Small Outline Package (TSOP)
<b>28U</b>	28-pin, Ceramic Pin Grid Array (PGA)
<b>W</b>	Die
Options	
<b>Blank</b>	Standard Device: Endurance = 10K Write Cycles; Write Time = 10 ms
<b>E</b>	High Endurance Option: Endurance = 100K Write Cycles
<b>F</b>	Fast Write Option: Write Time = 3 ms



## Ordering Information<sup>(1)</sup> (Continued)

t <sub>ACC</sub> (ns)	I <sub>CC</sub> (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
90	80	0.3	5962-88634 03 UX 5962-88634 03 XX 5962-88634 03 YX 5962-88634 03 ZX	28U 28D6 32L 28F	Military/883C Class B, Fully Compliant (-55°C to 125°C)
	80	0.3	5962-88634 04 UX 5962-88634 04 XX 5962-88634 04 YX 5962-88634 04 ZX	28U 28D6 32L 28F	Military/883C Class B, Fully Compliant (-55°C to 125°C)
120	80	0.3	5962-88634 01 UX 5962-88634 01 XX 5962-88634 01 YX 5962-88634 01 ZX	28U 28D6 32L 28F	Military/883C Class B, Fully Compliant (-55°C to 125°C)
	80	0.3	5962-88634 02 UX 5962-88634 02 XX 5962-88634 02 YX 5962-88634 02 ZX	28U 28D6 32L 28F	Military/883C Class B, Fully Compliant (-55°C to 125°C)

Note: 1. See "Valid Part Numbers" table on next page.

Package Type	
<b>28D6</b>	28-lead, 0.600" Wide, Non-windowed, Ceramic Dual Inline Package (Cerdip)
<b>28F</b>	28-lead, Non-windowed, Ceramic Bottom-brazed Flat Package (Flatpack)
<b>32J</b>	32-lead, Plastic J-leaded Chip Carrier (PLCC)
<b>32L</b>	32-pad, Non-windowed, Ceramic Leadless Chip Carrier (LCC)
<b>28P6</b>	28-lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
<b>28S</b>	28-lead, 0.300" Wide Plastic Gull Wing Small Outline (SOIC)
<b>28T</b>	28-lead, Plastic Thin Small Outline Package (TSOP)
<b>28U</b>	28-pin, Ceramic Pin Grid Array (PGA)
<b>W</b>	Die
Options	
<b>Blank</b>	Standard Device: Endurance = 10K Write Cycles; Write Time = 10 ms
<b>E</b>	High Endurance Option: Endurance = 100K Write Cycles
<b>F</b>	Fast Write Option: Write Time = 3 ms

## Ordering Information Note

Previous data sheets included the low power suffixes L, LE and LF on the At28HC256 for 120 ns and 90 ns speeds. The low power parameters are now standard; therefore, the L, LE and LF suffixes are no longer required.

## Valid Part Numbers

The following table lists standard Atmel products that can be ordered:

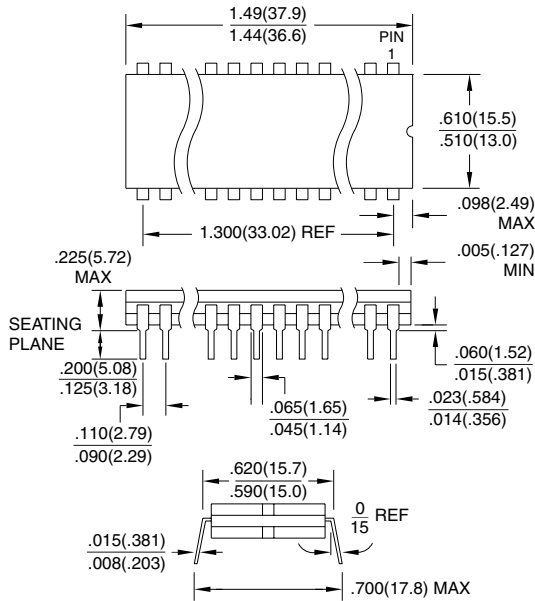
Device Numbers	Speed	Package and Temperature Combinations
AT28HC256	70	JC, JI, PC, PI
AT28HC256	90	JC, JI, PC, PI, TC, TI, DM/883, FM/883, UM/883
AT28HC256E	90	JC, JI, PC, PI, TC, TI, DM/883, FM/883, UM/883
AT28HC256F	90	JC, JI, PC, PI, TC, TI, DM/883, FM/883, UM/883
AT28HC256	12	JC, JI, PC, PI, TC, TI, DM/883, FM/883, UM/883
AT28HC256E	12	JC, JI, PC, PI, TC, TI, DM/883, FM/883, UM/883
AT28HC256F	12	JC, JI, PC, PI, TC, TI, DM/883, FM/883, UM/883

## Die Products

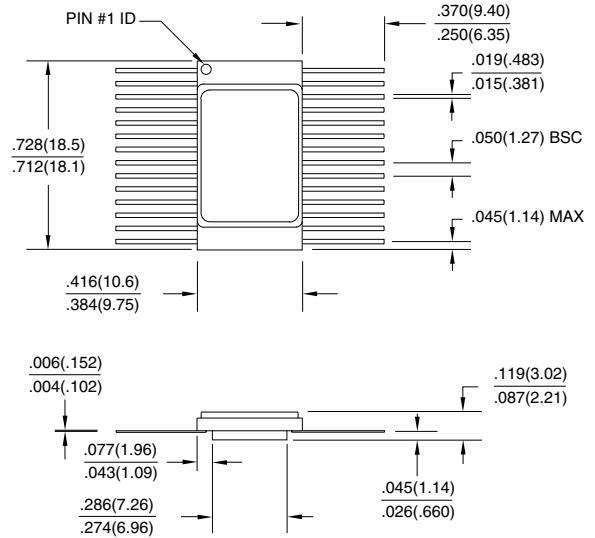
Reference Section: Parallel EEPROM Die Products

## Packaging Information

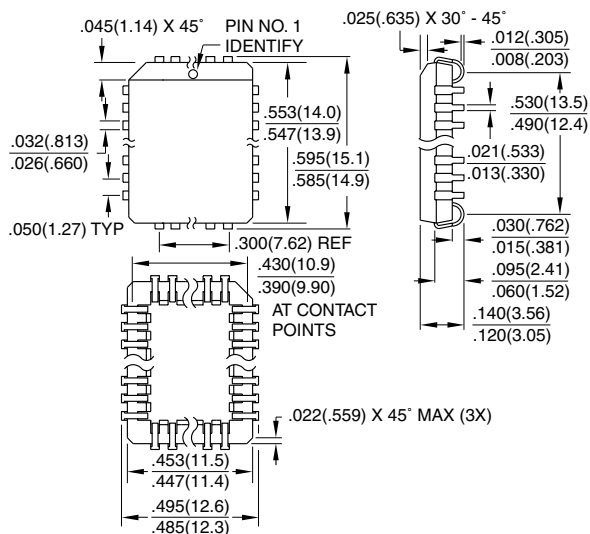
**28D6**, 28-lead, 0.600" Wide, Non-windowed, Ceramic Dual Inline Package (Cerdip)  
 Dimensions in Inches and (Millimeters)  
 MIL-STD-1835 D-10 CONFIG A



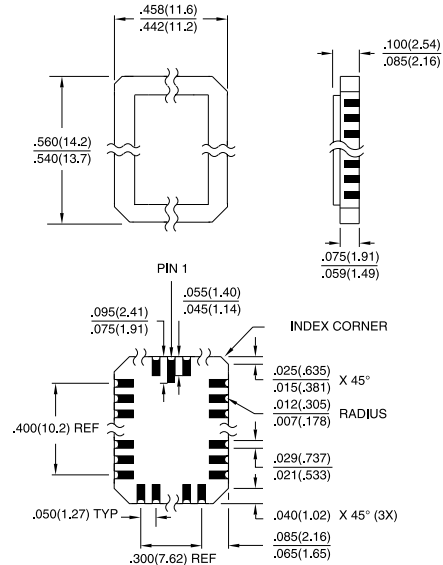
**28F**, 28-lead, Non-windowed, Ceramic Bottom-brazed Flat Package (Flatpack)  
 Dimensions in Inches and (Millimeters)  
 MIL-STD-1835 F-12 CONFIG B



**32J**, 32-lead, Plastic J-leaded Chip Carrier (PLCC)  
 Dimensions in Inches and (Millimeters)  
 JEDEC STANDARD MS-016 AE



**32L**, 32-pad, Non-windowed, Ceramic Leadless Chip Carrier (LCC)  
 Dimensions in Inches and (Millimeters)\*  
 MIL-STD-1835 C-12

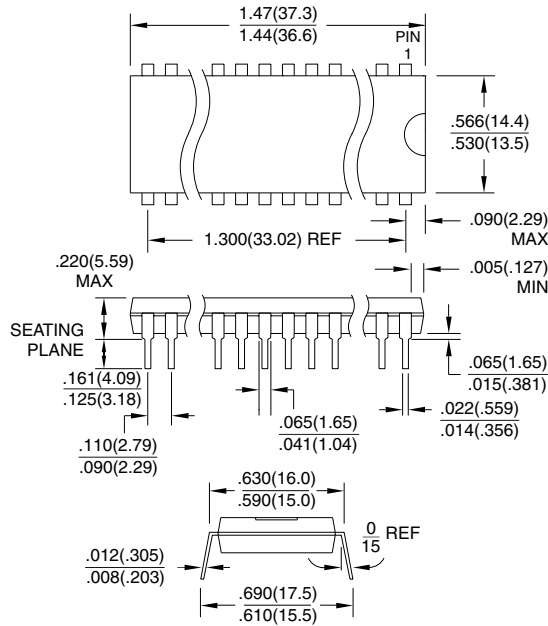


\*Controlling dimension: millimeters

## Packaging Information

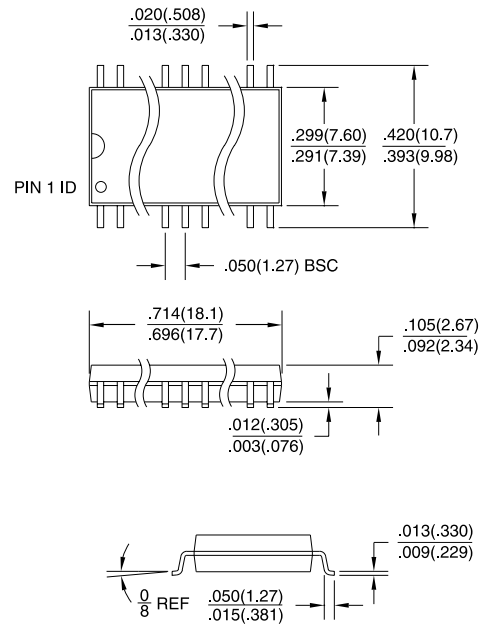
**28P6**, 28-lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)

Dimensions in Inches and (Millimeters)  
JEDEC STANDARD MS-011 AB



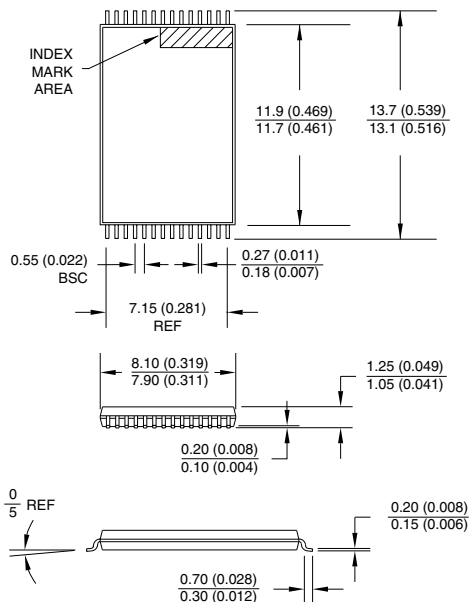
**28S**, 28-lead, 0.300" Wide, Plastic Gull Wing Small Outline (SOIC)

Dimensions in Inches and (Millimeters)



**28T**, 28-lead, Plastic Thin Small Outline Package (TSOP)

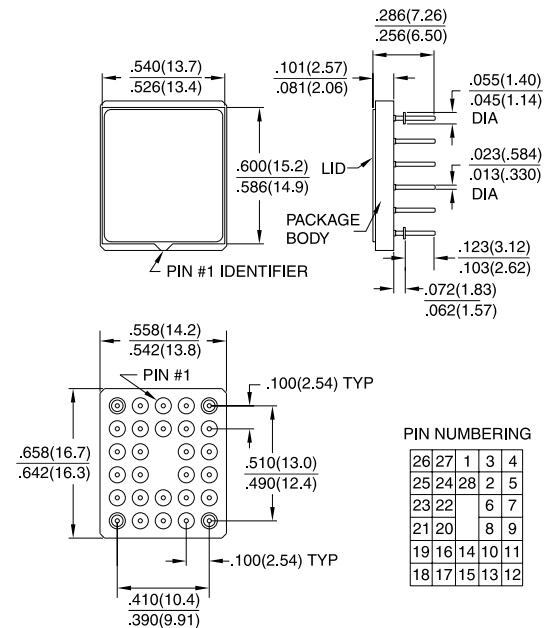
Dimensions in Millimeters and (Inches)\*



\*Controlling dimension: millimeters

**28U**, 28-pin, Ceramic Pin Grid Array (PGA)

Dimensions in Inches and (Millimeters)





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