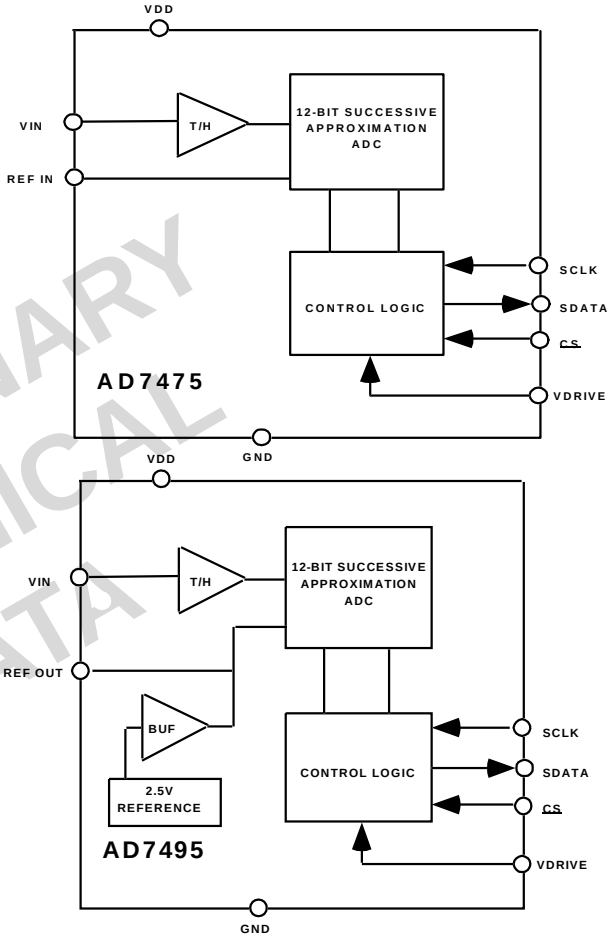
1MSPS, 12-Bit ADCs in µSO-8

Preliminary Technical Data — AD7475/95

FEATURES

Fast Throughput Rate: 1MSPS
Specified for V_{DD} of 2.7 V to 5.25 V
Low Power:
3mW typ at 1MSPS with 3V Supplies
9mW typ at 1MSPS with 5V Supplies
Wide Input Bandwidth:
70dB SNR at 500kHz Input Frequency
Flexible Power/Serial Clock Speed Management
No Pipeline Delays
High Speed Serial Interface SPI/QSPI/µWire/DSP Compatible
Onboard Reference 2.5V (AD7495 only)
Standby Mode: 1µA max
8-Pin µSOIC and SOIC Packages

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7475 /AD7495 are 12-bit high speed, low power, successive-approximation ADCs. The parts operate from a single 2.7 V to 5.25 V power supply and feature throughput rates up to 1MSPS. The parts contain a low-noise, wide bandwidth track/hold amplifier which can handle input frequencies in excess of 1MHz.

The conversion process and data acquisition are controlled using $\overline{CS}$ and the serial clock allowing the devices to interface with microprocessors or DSPs. The input signal is sampled on the falling edge of $\overline{CS}$ and conversion is also initiated at this point. There are no pipelined delays associated with the part.

The AD7475/AD7495 uses advanced design techniques to achieve very low power dissipation at high throughput rates. With 3V supplies and 1MSPS throughput rate, the AD7475 consumes just 1mA, while the AD7495 consumes 1.2mA. With 5V supplies and 1MSPS, the current consumption is 1.8mA for the AD7475 and 2mA for the AD7495.

The analog input range for the part is 0 to REF IN. The +2.5V reference for the AD7475 is applied externally to the REF IN pin while the AD7495 has an onboard 2.5V reference. The conversion rate is determined by the SCLK.

PRODUCT HIGHLIGHTS

1. High Throughput with Low Power Consumption
   The AD7475 offers 1MSPS throughput rates with 3mW power consumption.
2. Flexible Power/Serial Clock Speed Management
   The conversion rate is determined by the serial clock allowing the power to be reduced as the conversion time is reduced through the serial clock speed increase. The part also features a shutdown mode to maximize power efficiency at lower throughput rates. Power consumption is 1µA max when in shutdown.
3. No Pipeline Delay
   The part features a standard successive-approximation ADC with accurate control of the sampling instant via a $\overline{CS}$ input and once off conversion control.

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AD7475—SPECIFICATIONS[1]

(V_{DD} = +2.7 V to +5.25 V, REF IN = 2.5 V, f_{SCLK} = 18.5 MHz unless otherwise noted; T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

Parameter	A Version[1]	B Version[1]	Units	Test Conditions/Comments
DYNAMIC PERFORMANCE				
Signal to Noise + Distortion Ratio[2] (SINAD)	69	69	dB min	F_{IN} =455kHz Sine Wave, f_{SAMPLE} = 1Msps
Signal to Noise Ratio (SNR)[2]	70	70	dB min	F_{IN} =455kHz Sine Wave, f_{SAMPLE} = 1Msps
Total Harmonic Distortion (THD)	–76	-76	dB max	F_{IN} = 455kHz Sine Wave, f_{SAMPLE} = 1Msps
Peak Harmonic or Spurious Noise (SFDR)	–76	-76	dB max	F_{IN} =455kHz Sine Wave, f_{SAMPLE} = 1Msps
Intermodulation Distortion (IMD)				
Second Order Terms	–78	-78	dB typ	
Third Order Terms	–78	-78	dB typ	
Aperture Delay	20	20	ns max	
Aperture Jitter	50	50	ps typ	
Full Power Bandwidth	tbd	tbd	MHz typ	@ 3 dB
DC ACCURACY				
Resolution	12	12	Bits	
Integral Nonlinearity	±2	±1	LSB max	
Differential Nonlinearity	±0.9	±0.9	LSB max	Guaranteed No Missed Codes to 12 Bits. (B Grade)
Offset Error	±3	±3	LSB max	
Gain Error	±3	±3	LSB max	
ANALOG INPUT				
Input Voltage Ranges	0 to REF IN		Volts	
DC Leakage Current	±1	±1	µA max	
Input Capacitance	20	20	pF typ	
REFERENCE INPUT				
REF IN Input Voltage Range	2.5	2.5	Volts	±1% for specified performance
dc Leakage Current	±1	±1	µA max	
Input Capacitance	20	20	pF typ	
LOGIC INPUTS				
Input High Voltage, V_{INH}	2.8	2.8	V min	VDRIVE = 5V
	2.4	2.4	V min	VDRIVE = 3V
Input Low Voltage, V_{INL}	0.4	0.4	V max	
Input Current, I_{IN}	±1	±1	µA max	Typically 10 nA, V_{IN} = 0 V or VDRIVE
Input Capacitance, C_{IN}[3]	10	10	pF max	
LOGIC OUTPUTS				
Output High Voltage, V_{OH}	VDRIVE -0.2		V min	I_{SOURCE} = 200 µA; V_{DD} = 2.7 V to 5.25 V
Output Low Voltage, V_{OL}	0.4	0.4	V max	I_{SINK} =200µA
Floating-State Leakage Current	±10	±10	µA max	
Floating-State Output Capacitance[3]	10	10	pF max	
Output Coding	Straight (Natural) Binary			
CONVERSION RATE				
Conversion Time	865	865	ns max	16 SCLK cycles with SCLK at 18.5MHz
Track/Hold Acquisition Time	250	250	ns max	
Throughput Rate	1	1	MSPS max	Conversion Time + Quiet Time.

AD7475—SPECIFICATIONS[1]

(V_{DD} = +2.7 V to +5.25 V, REF IN = 2.5 V, f_{SCLK} = 18.5 MHz unless otherwise noted; T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

Parameter	A Version[1]	B Version[1]	Units	Test Conditions/Comments
POWER REQUIREMENTS				
V_{DD}	+2.7/+5.25	+2.7/+5.25	V min/max	
VDRIVE	+2.7/+5.25	+2.7/+5.25	V min/max	
I_{DD}[4]				Digital I/Ps = 0V or V_{DD}.
Normal Mode(Static)	750	750	µA typ	V_{DD} = 4.75V to 5.25V. SCLK on or off.
Normal Mode (Operational)	1.8	1.8	mA max	V_{DD} = 4.75V to 5.25V. F_{SAMPLE} = 1MSPS
	1	1	mA max	V_{DD} = 2.7V to 3.3V. F_{SAMPLE} = 1MSPS
Partial Power-Down Mode	tbd	tbd	µA typ	F_{SAMPLE} = 750kSPS
Partial Power-Down Mode	90	90	µA max	(Static)
Full Power-Down Mode	1	1	µA max	SCLK on or off.
Power Dissipation[4]				
Normal Mode (Operational)	9	9	mW max	V_{DD} = 5V. F_{SAMPLE} = 1MSPS
	3	3	mW max	V_{DD} = 3V. F_{SAMPLE} = 1MSPS
Partial Power-Down	tbd	tbd		V_{DD} = 5V.
	tbd	tbd		V_{DD} = 3V.
Full Power-Down	5	5	µW max	V_{DD} = 5 V.
	3	3	µW max	V_{DD} = 3 V.

NOTES
[1]Temperature ranges as follows: A, B Versions: –40°C to +85°C.
[2]SNR calculation includes distortion and noise components.
[3]Sample tested @ +25°C to ensure compliance.
[4]See POWER VERSUS THROUGHPUT RATE section.
Specifications subject to change without notice.

AD7495—SPECIFICATIONS[1] (V_{DD} = +2.7 V to +5.25 V, f_{SCLK} = 18.5 MHz unless otherwise noted; T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

Parameter	A Version[1]	B Version[1]	Units	Test Conditions/Comments
DYNAMIC PERFORMANCE				
Signal to Noise + Distortion [2] (SINAD)	69	69	dB min	F_{IN} =500kHz Sine Wave, f_{SAMPLE} = 1Msps
Signal to Noise Ratio (SNR)[2]	70	70	dB min	F_{IN} =500kHz Sine Wave, f_{SAMPLE} = 1Msps
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Peak Harmonic or Spurious Noise (SFDR)	–76	-76	dB max	F_{IN} =500kHz Sine Wave, f_{SAMPLE} = 1Msps
Intermodulation Distortion (IMD)				
Second Order Terms	–78	-78	dB typ	
Third Order Terms	–78	-78	dB typ	
Aperture Delay	20	20	ns max	
Aperture Jitter	50	50	ps typ	
Full Power Bandwidth	tbd	tbd	MHz typ	@ 3 dB
DC ACCURACY				
Resolution	12	12	Bits	
Integral Nonlinearity	±2	±1	LSB max	
Differential Nonlinearity	±0.9	±0.9	LSB max	Guaranteed No Missed Codes to 12 Bits. (B Grade)
Offset Error	±3	±3	LSB max	
Gain Error	±3	±3	LSB max	
ANALOG INPUT				
Input Voltage Ranges	0 to 2.5	0 to 2.5	Volts	
DC Leakage Current	±1	±1	µA max	
Input Capacitance	20	20	pF typ	
REFERENCE OUTPUT				
REF OUT Output Voltage	tbd	tbd	Volts	
REF OUT Impedance	tbd	tbd		
REF OUT Temperature Coefficient	50	50	ppm/°C	
LOGIC INPUTS				
Input High Voltage, V_{INH}	2.8	2.8	V min	VDRIVE = 5V
	2.4	2.4	V min	VDRIVE = 3V
Input Low Voltage, V_{INL}	0.8	0.8	V max	
Input Current, I_{IN}	±1	±1	µA max	Typically 10 nA, V_{IN} = 0 V or VDRIVE
Input Capacitance, C_{IN}[3]	10	10	pF max	
LOGIC OUTPUTS				
Output High Voltage, V_{OH}	VDRIVE -0.2		V min	I_{SOURCE} = 200 µA; V_{DD} = 2.7 V to 5.25 V
Output Low Voltage, V_{OL}	0.4	0.4	V max	I_{SINK} =200µA
Floating-State Leakage Current	±10	±10	µA max	
Floating-State Output Capacitance[3]	10	10	pF max	
Output Coding	Straight (Natural) Binary			
CONVERSION RATE				
Conversion Time	865	865	ns max	16 SCLK cycles with SCLK at 18.5MHz
Track/Hold Acquisition Time	250	250	ns max	
Throughput Rate	1	1	MSPS max	Conversion Time + Quiet Time.

AD7495–SPECIFICATIONS[1] (V_{DD} = +2.7 V to +5.25 V, f_{SCLK} = 18.5 MHz unless otherwise noted; T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

Parameter	A Version[1]	B Version[1]	Units	Test Conditions/Comments
POWER REQUIREMENTS				
V_{DD}	+2.7/+5.25	+2.7/+5.25	V min/max	
VDRIVE	+2.7/+5.25	+2.7/+5.25	V min/max	
I_{DD}[4]				Digital I/Ps = 0V or V_{DD}.
Normal Mode(Static)	1.1	1.1	mA typ	V_{DD} = 4.75V to 5.25V. SCLK on or off.
Normal Mode (Operational)	2	2	mA max	V_{DD} = 4.75V to 5.25V. F_{SAMPLE} = 1MSPS
	1.2	1.2	mA max	V_{DD} = 2.7V to 3.3V. F_{SAMPLE} = 1MSPS
Partial Power-Down Mode			µA typ	F_{SAMPLE} = 750kSPS
Partial Power-Down Mode	190	190	µA max	(Static)
Full Power-Down Mode	90	90	µA typ	V_{DD} = 4.75V to 5.25V F_{SAMPLE} = 1kSPS
Full Power-Down Mode	1	1	µA max	(Static) SCLK on or off.
Power Dissipation[4]				
Normal Mode (Operational)	10	10	mW max	V_{DD} = 5V. F_{SAMPLE} = 1MSPS
	3.6	3.6	mW max	V_{DD} = 3V. F_{SAMPLE} = 1MSPS
Partial Power-Down				V_{DD} = 5V.
				V_{DD} = 3V.
Full Power-Down	5	5	µW max	V_{DD} = 5 V.
	3	3	µW max	V_{DD} = 3 V.

NOTES
[1]Temperature ranges as follows: A, B Versions: –40°C to +85°C.
[2]SNR calculation includes distortion and noise components.
[3]Sample tested @ +25°C to ensure compliance.
[4]See POWER VERSUS THROUGHPUT RATE section.

Specifications subject to change without notice.

TIMING SPECIFICATIONS[1] (V_{DD} = +2.7 V to +5.25 V, REF IN = 2.5 V (AD7475); $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.)

Parameter	Limit at T_{MIN}, T_{MAX} AD7475/AD7495	Units	Description
f_{SCLK}[2]	1	kHz min	
	18.5	MHz max	
$t_{CONVERT}$	16* t_{SCLK}		$t_{SCLK} = 1/f_{SCLK}$
	865	ns max	f_{SCLK} = 18.5MHz
t_{quiet}	100	ns min	Minimum Quiet Time required between conversions
t_2	tbd	ns min	$\overline{CS}$ to SCLK Setup Time
t_3[3]	tbd	ns max	Delay from $\overline{CS}$ Until SDATA 3-State Disabled
t_4[3]	10	ns max	Data Access Time After SCLK Falling Edge
t_5	tbd	ns min	Data Setup Time prior to SCLK Falling Edge
t_6	$0.4t_{SCLK}$	ns min	SCLK High Pulse Width
t_7	$0.4t_{SCLK}$	ns min	SCLK Low Pulse Width
t_8	5	ns min	SCLK to Data Valid Hold Time
t_9[4]	25	ns max	SCLK falling Edge to SDATA High Impedance
t_{10}	tbd	µs typ	Power up time from Full power-down

NOTES

[1]Sample tested at +25°C to ensure compliance. All input signals are specified with tr = tf = 5 ns (10% to 90% of V_{DD}) and timed from a voltage level of 1.6 Volts. See Figure 2.

[2]Mark/Space ratio for the SCLK input is 40/60 to 60/40.

[3]Measured with the load circuit of Figure 1 and defined as the time required for the output to cross 0.8 V or 2.0 V.

[4]t_9 is derived form the measured time taken by the data outputs to change 0.5 V when loaded with the circuit of Figure 1. The measured number is then extrapolated back to remove the effects of charging or discharging the 50 pF capacitor. This means that the time, t_9, quoted in the timing characteristics is the true bus relinquish time of the part and is independent of the bus loading.

Specifications subject to change without notice.

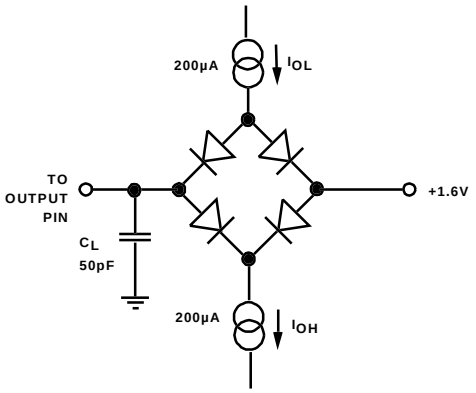
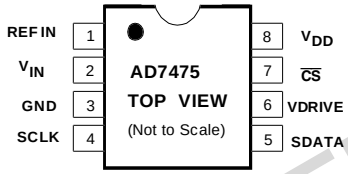
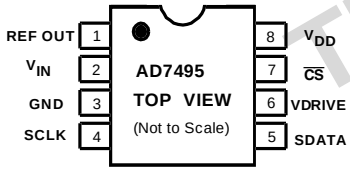


Figure 1. Load Circuit for Digital Output Timing Specifications

AD7475 PINCONFIGURATION SOIC/ µSOIC



AD7495 PINCONFIGURATION SOIC/ µSOIC



ABSOLUTE MAXIMUM RATINGS[1]

(T_A = +25°C unless otherwise noted)

V_{DD} to GND	–0.3 V to 7 V
VDRIVE to GND	–0.3 V to V_{DD} + 0.3 V
Analog Input Voltage to GND	–0.3 V to V_{DD} + 0.3 V
Digital Input Voltage to GND	–0.3 V to VDRIVE + 0.3 V
Digital Output Voltage to GND	–0.3 V to VDRIVE + 0.3 V
REF IN to GND	–0.3 V to V_{DD} + 0.3 V
Input Current to Any Pin Except Supplies[2]	±10 mA
Operating Temperature Range	
Commercial (A Version)	–40°C to +85°C
Storage Temperature Range	–65°C to +150°C
Junction Temperature	+150°C
SOIC, µSOIC Package, Power Dissipation	450 mW
θ_{JA} Thermal Impedance	157°C/W (SOIC)
	205.9°C/W (µSOIC)
θ_{JC} Thermal Impedance	56°C/W (SOIC)
	43.74°C/W (µSOIC)
Lead Temperature, Soldering	
Vapor Phase (60 secs)	+215°C
Infared (15 secs)	+220°C

NOTES

[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2]Transient currents of up to 100 mA will not cause SCR latch up.

ORDERING GUIDE

Model	Range	Linearity Error (LSB)[1]	Package Option[2]	Branding
AD7495AR	-40°C to +85°C	±2	SO-8	AD7495AR
AD7495BR	-40°C to +85°C	±1	SO-8	AD7495BR
AD7495ARM	-40°C to +85°C	±2	RM-8	CCA
AD7475AR	-40°C to +85°C	±2	SO-8	AD7475AR
AD7475BR	-40°C to +85°C	±1	SO-8	AD7475BR
AD7475ARM	-40°C to +85°C	±2	RM-8	C9A
EVAL-AD7495CB[3]	Evaluation Board			
EVAL-AD7475CB[3]	Evaluation Board			
EVAL-CONTROL BOARD[4]	Controller Board			

NOTES

[2]R = SOIC; RM = µSOIC.

[3]This can be used as a stand-alone evaluation board or in conjunction with the EVAL-CONTROL BOARD for evaluation/demonstration purposes.

[4]This board is a complete unit allowing a PC to control and communicate with all Analog Devices evaluation boards ending in the CB designators.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD7475/AD7495 feature proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN FUNCTION DESCRIPTION

Pin No.	Pin Mnemonic	Function
7	$\overline{CS}$	Chip Select. Active low logic input. This input provides the dual function of initiating conversions on the AD7475/AD7495 and also frames the serial data transfer.
1	REF IN	Reference Input for the AD7475. An external reference must be applied to this input. The voltage range for the external reference is 2.5V±1% for specified performance.
	REF OUT	Reference Output for the AD7495. A 100nF capacitor is required from this pin to AGND. The internal reference can be taken from this pin but buffering is required before it is applied elsewhere in a system.
8	V_{DD}	Power Supply Input. The V_{DD} range for the AD7475/AD7495 is from +2.7V to +5.25V.
3	GND	Analog Ground. Ground reference point for all circuitry on the AD7475/AD7495. All analog input signals and any external reference signal should be referred to this GND voltage. Both of these pins should connect to the AGND plane of a system.
2	VIN	Analog Input. Single-ended analog input channel. The input range is 0 to REFIN.
6	VDRIVE	Logic Power Supply Input. The voltage supplied at this pin determines what voltage the interface of the AD7475/AD7495 will operate at.
5	SDATA	Data Out. Logic Output. The conversion result from the AD7475/AD7495 is provided on this output as a serial data stream. The bits are clocked out on the falling edge of the SCLK input. The data stream consists of four leading zeros followed by the 12 bits of conversion data which is provided MSB first.
4	SCLK	Serial Clock. Logic input. SCLK provides the serial clock for accessing data from the part. This clock input is also used as the clock source for the AD7475/AD7495's conversion process.

TERMINOLOGY

Integral Nonlinearity
This is the maximum deviation from a straight line passing through the endpoints of the ADC transfer function. The endpoints of the transfer function are zero scale, a point 1/2 LSB below the first code transition, and full scale, a point 1/2 LSB above the last code transition.

Differential Nonlinearity
This is the difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

Offset Error
This is the deviation of the first code transition (00 . . . 000) to (00 . . . 001) from the ideal, i.e AGND + 1LSB

Gain Error
This is the deviation of the last code transition (111 . . . 110) to (111 . . . 111) from the ideal (i.e., V_{REF} – 1 LSB) after the offset error has been adjusted out.

Track/Hold Acquisition Time
The track/hold amplifier returns into track mode and the end of conversion. Track/Hold acquisition time is the time required for the output of the track/hold amplifier to reach its final value, within ±1 LSB, after the end of conversion.

Signal to (Noise + Distortion) Ratio
This is the measured ratio of signal to (noise + distortion) at the output of the A/D converter. The signal is the rms amplitude of the fundamental. Noise is the sum of all nonfundamental signals up to half the sampling frequency ($f_S/2$), excluding dc. The ratio is dependent on the number of quantization levels in the digitization process; the more levels, the smaller the quantization noise. The theoretical signal to (noise + distortion) ratio for an ideal N-bit converter with a sine wave input is given by:

Signal to (*Noise* + *Distortion*) = (6.02 *N* + 1.76) *dB*

Thus for a 12-bit converter, this is 74 dB.

Total Harmonic Distortion
Total harmonic distortion (THD) is the ratio of the rms sum of harmonics to the fundamental. For the AD7475/ AD7495, it is defined as:

$$THD\ (dB) = 20 \log \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2}}{V_1}$$

where V_1 is the rms amplitude of the fundamental and V_2, V_3, V_4, V_5 and V_6 are the rms amplitudes of the second through the sixth harmonics.

Peak Harmonic or Spurious Noise
Peak harmonic or spurious noise is defined as the ratio of the rms value of the next largest component in the ADC output spectrum (up to $f_S/2$ and excluding dc) to the rms value of the fundamental. Normally, the value of this specification is determined by the largest harmonic in the spectrum, but for ADCs where the harmonics are buried in the noise floor, it will be a noise peak.

Intermodulation Distortion
With inputs consisting of sine waves at two frequencies, fa and fb, any active device with nonlinearities will create distortion products at sum and difference frequencies of mfa ± nfb where m, n = 0, 1, 2, 3, etc. Intermodulation distortion terms are those for which neither m nor n are equal to zero. For example, the second order terms include (fa + fb) and (fa – fb), while the third order terms include (2fa + fb), (2fa – fb), (fa + 2fb) and (fa – 2fb).

The AD7475/AD7495 are tested using the CCIF standard where two input frequencies near the top end of the input bandwidth are used. In this case, the second order terms are usually distanced in frequency from the original sine waves while the third order terms are usually at a frequency close to the input frequencies. As a result, the second and third order terms are specified separately. The calculation of the intermodulation distortion is as per the THD specification where it is the ratio of the rms sum of the individual distortion products to the rms amplitude of the sum of the fundamentals expressed in dBs.

PSR (Power Supply Rejection)
Variations in power supply will affect the full-scale transition, but not the conveter's linearity. Power Supply Rejection is the maximum change in the full-scale transition point due to a change in power-supply voltage from the nominal value.

MODES OF OPERATION

The mode of operation of the AD7475/AD7495 is selected by controlling the (logic) state of the $\overline{CS}$ signal during a conversion. There are three possible modes of operation, Normal Mode, Partial Power-Down Mode and Full Power-Down Mode. The point at which $\overline{CS}$ is pulled high after the conversion has been initiated will determine which power-down mode, if any, that the device will enter. Similarly, if already in a power-down mode then $\overline{CS}$ can control whether the device will return to Normal operation or remain in power-down. These modes of operation are designed to provide flexible power management options. These options can be chosen to optimize the power dissipation/throughput rate ratio for differing application requirements.

Normal Mode

This mode is intended for fastest throughput rate performance as the user does not have to worry about any power-up times with the AD7475/AD7495 remaining fully-powered all the time. Figure 2 shows the general diagram of the operation of the AD7475/AD7495 in this mode.

The conversion is iniated on the falling edge of $\overline{CS}$ as described in the Serial Interface section. To ensure the part remains fully powered up at all times $\overline{CS}$ must remain low until at least 10 SCLK falling edges have elapsed after the falling edge of $\overline{CS}$. If $\overline{CS}$ is brought high any time after the 10th SCLK falling edge but before the 16th SCLK falling edge the part will remain powered up but the conversion will be terminated and SDATA will go back into tri-state. Sixteen serial clock cycles are required to complete the conversion and access the conversion result. $\overline{CS}$ may idle high until the next conversion or may idle low until sometime prior to the next conversion, (effectively idling $\overline{CS}$ low).

Once a data transfer is complete (SDATA has returned to tri-state), another conversion can be initiated after the quiet time, t_{quiet}, has elapsed by bringing $\overline{CS}$ low again.

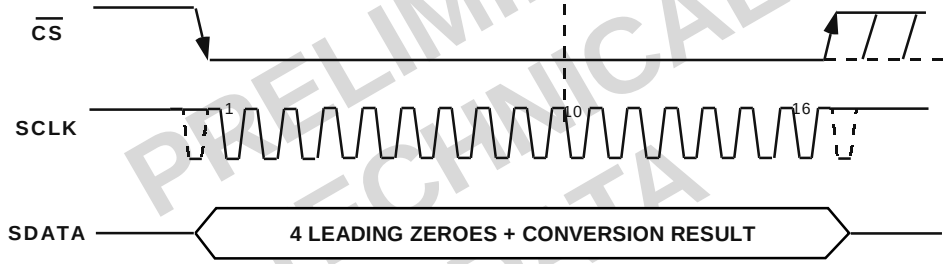


Figure 2. Normal Mode Operation

Partial Power-Down Mode

This mode is intended for use in applications where slower throughput rates are required; either the ADC is powered down between each conversion, or a series of conversions may be performed at a high throughput rate and then the ADC is powered down for a relatively long duration between these bursts of several conversions. When the AD7475 is in partial power down, all analog circuitry is powered down except for the bias current generator and in the case of the AD7495 all analog circuitry is powered down except for the on-chip reference and reference buffer.

To enter Partial Power-Down, the conversion process must be interrupted by bringing $\overline{CS}$ high anywhere after the second falling edge of SCLK and before the tenth falling edge of SCLK as shown in Figure 3. Once $\overline{CS}$ has been brought high in this window of SCLKs, then the part will enter partial power down and the conversion that was intiated by the falling edge of $\overline{CS}$ will be terminated and SDATA will go back into tri-state. If $\overline{CS}$ is brought high before the second SCLK falling edge, then the part will remain in Normal Mode and will not power-down. This will avoid accidental powerdown due to glitches on the $\overline{CS}$ line.

In order to exit this mode of operation and power the AD7475/AD7495 up again, a dummy conversion is performed. On the falling edge of $\overline{CS}$ the device will begin to power up, and will continue to power up as long as $\overline{CS}$ is held low until after the falling edge of the tenth SCLK. The device will be fully powered up once 16 SCLKs have

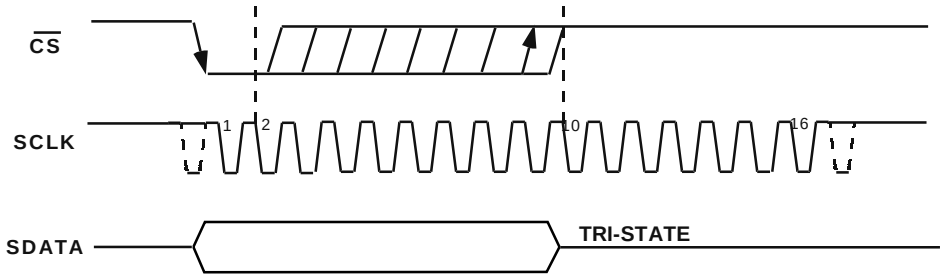


Figure 3. Entering Partial Power-Down Mode

elapsed and valid data will result from the next conversion as shown in figure 4. If $\overline{CS}$ is brought high before the second falling edge of SCLK, then the AD7475/AD7495 will go back into partial power down again. This avoids accidental power up due to glitches on the $\overline{CS}$ line, as although the device may begin to power up on the falling edge of $\overline{CS}$, it will power down again on the rising edge of $\overline{CS}$. If in Partial Power-Down and CS is brought high between the second and tenth falling edges of SCLK then the device will enter Full Power Down Mode.

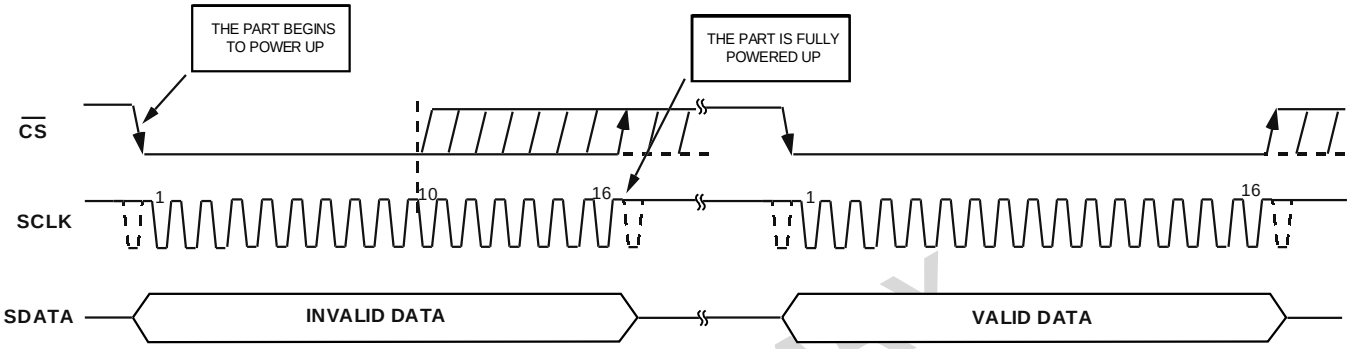


Figure 4. Exiting Partial Power-Down Mode

Full Power-Down Mode

This mode is intended for use in applications where slower throughput rates are required than that in the Partial Power Down Mode, as power up from a full power down would not be complete in just one dummy conversion. This mode is more suited to applications where a series of conversions performed at a relatively high throughput rate would be followed by a long period of inactivity and hence power down. When the AD7475/ AD7495 is in full power down, all analog circuitry is powered down. See Power-up Times section.

Full Power-Down is entered in a similar way as partial power down except the timing sequence shown in Figure 3 must be executed twice.The conversion process must be interrupted in a similar fashion by bringing $\overline{CS}$ high anywhere after the second falling edge of SCLK and before the tenth falling edge of SCLK. The device will enter partial power down at this point. To reach full power down, the next conversion cycle must be interrupted in the same way as shown in Figure 5. Once $\overline{CS}$ has been brought high in this window of SCLKs, then the part will power down completely.

NOTE: It is not necessary to complete the 16 SCLKs once $\overline{CS}$ has been brought high to enter a power down mode.

To exit Full Power Down, and power the AD7475/ AD7495 up again, a dummy conversion is performed as when powering up from partial power down. On the falling edge of $\overline{CS}$ the device will begin to power up, and will continue to power up as long as $\overline{CS}$ is held low until after the falling edge of the tenth SCLK. The power up time is longer than one dummy conversion cycle however and this time must elapse before a conversion can be initaited as shown in Figure 6. See Power-up Times section for the power up times associated with the AD7475 and the AD7495.

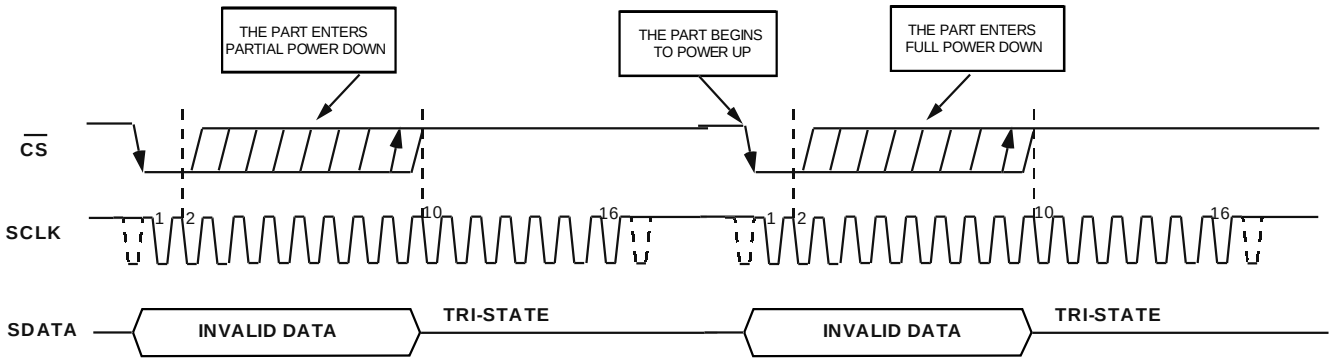


Figure 5. Entering Full Power-Down Mode

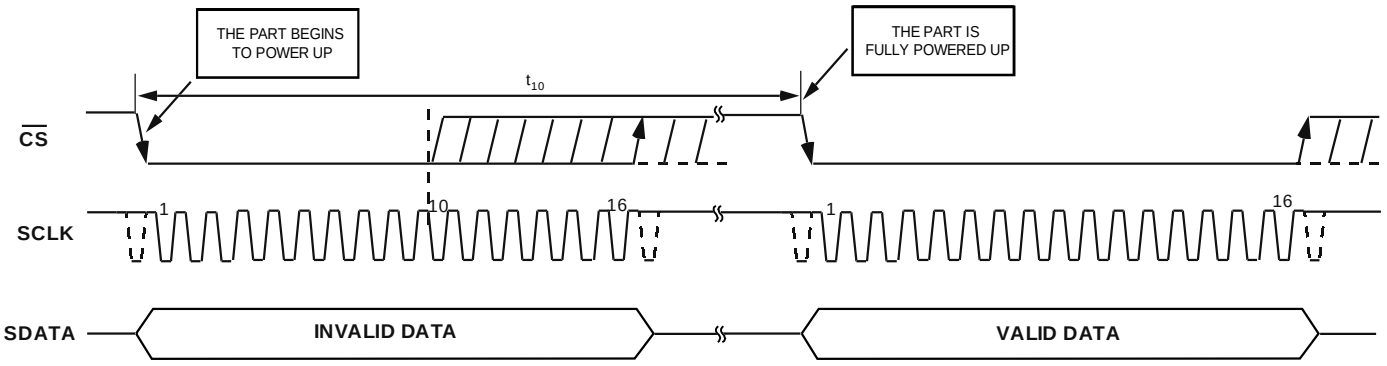


Figure 6. Exiting Full Power-Down Mode

SERIAL INTERFACE

Figure 7 shows the detailed timing diagram for serial interfacing to the AD7475/AD7495. The serial clock provides the conversion clock and also controls the transfer of information from the AD7475/AD7495 during conversion.

$\overline{CS}$ initiates the data transfer and conversion process. The falling edge of $\overline{CS}$ puts the track and hold into hold mode, takes the bus out of tristate and the analog input is sampled at this point. The conversion is also initiated at this point and will require 16 SCLK cycles to complete. On the 16th SCLK falling edge the SDATA line will go back into tristate. If the rising edge of $\overline{CS}$ occurs before 16 SCLKs have elapsed, then the conversion will be terminated and the SDATA line will go back into tri-state, otherwise SDATA returns to tristate on the 16th SCLK falling edge as shown in figure 7.

Sixteen serial clock cycles are required to perform the conversion process and to access data from the AD7475/95. $\overline{CS}$ going low provides the first leading zero to be read in by the microcontroller or DSP. The remaining data is then clocked out by subsequent SCLK falling edges beginning with the 2nd leading zero, thus the first falling clock edge on the serial clock has the second leading zero provided. The final bit in the data transfer is valid on the sixteenth falling edge, having being clocked out on the previous (15th) falling edge. In applications with a slower SCLK, it may be possible to read in data on each SCLK rising edge, i.e. the first rising edge of SCLK after the $\overline{CS}$ falling edge would provide the first leading zero and the 15th rising SCLK edge would provide DB0.

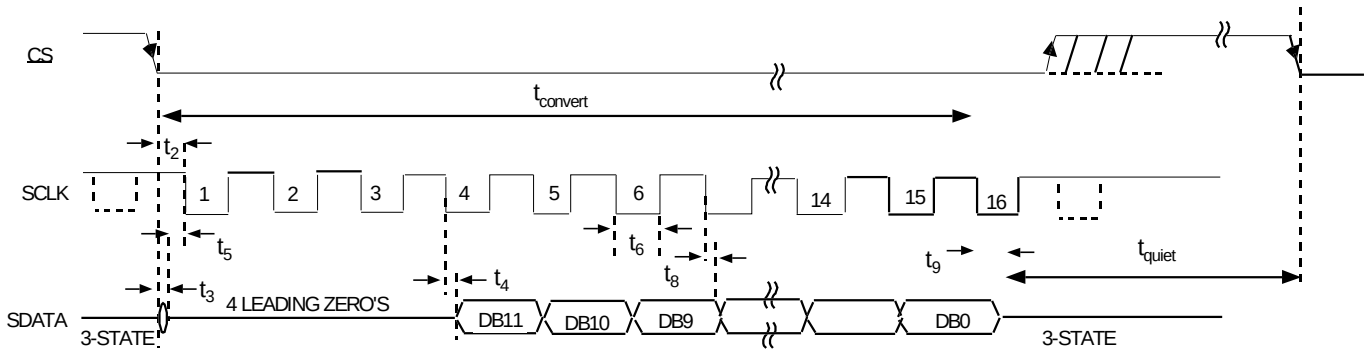
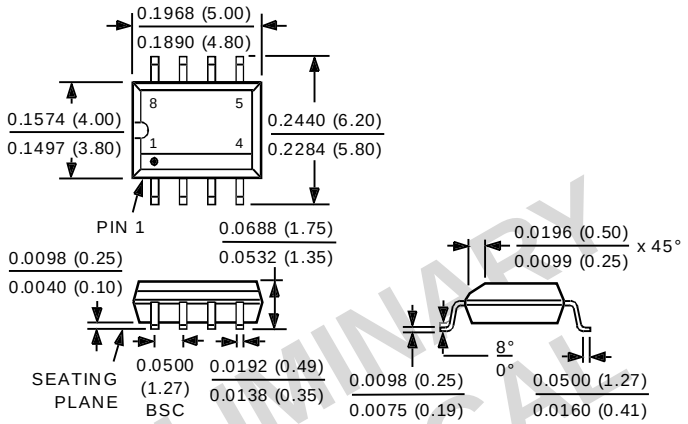


Figure 7. Serial Interface Timing Diagram

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

8-lead SOIC (SO-8)



8-lead microSOIC (RM-8)