6.5 A 128x128 CMOS Imager with 4x128 Bit-Serial Column-Parallel PE Array

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A column parallel processing architecture in CMOS imagers is advantageous over the alternative System-On-Imager solutions, because both simple pixel structure and wide bandwidth between the imager and processor are maintained in the architecture. A conventional column parallel processing architecture either leaves insufficient processing speed or requires sophisticated data path to meet the required image processing speed [1], [2]. In this work, a 4x128 fine-grained bit-serial processing element (PE) array is incorporated into 128x128 pixel CMOS imager columns as shown in Figure 6.5.1 to meet the processing speed requirement and the demand for versatile processing system. Four column parallel SIMD processors are configured as a MIMD architecture to share image-processing tasks. A fully-programmable PE structure and this re-configurable processor array architecture allow a highly flexible processing system. The prototype imager chip potentially affords pixel-rate color-processing tasks such as color interpolation, color correction, aperture correction, and color-coding, for 8b 640x480 images at 30frame/s by performing ~220 operations/pixel with a 20MHz clock. The column-parallel processing imager chip is fabricated with a standard triple metal 0.6mm CMOS technology.

All the data paths in the imager chip shown in Figure 6.5.1 are implemented at imager column level. Correlated double sampling (CDS) circuitry is arranged per column to reduce a pixel-to-pixel fixed pattern noise (FPN). Sampled signals are digitized with a column parallel cyclic analog-to-digital converter (ADC) [3]. One ADC is implemented per 4 imager columns, and four pixel data in the same imager row are digitized successively in one row period. The layout pitch of both the CDS and the ADC are exactly four times the pixel column pitch. The PEs are physically laid out as 4x128 two-dimensional array pitch-matched to imager pixels to minimize silicon area, whereas the PE array is functionally configured with four 1x128 column parallel SIMD processors. The PEs in the same PE row share a single stream of instruction and work as a SIMD processor. Each PE row receives respective instruction streams. This processing architecture can be considered as a combination of SIMD processors with a MIMD processing scheme. The column pitch of 18mm is not dominated by the size of a PE but by that of Op-Amps used both in CDS and in ADC circuits. The expected minimum PE column pitch with 0.6μm technology is estimated as ~7μm. Since the cyclic converter produces outputs bit by bit, no output register for the ADC is required between the ADC and the next stage bit-serial PE arrays. The cyclic ADC and the bit-serial PE architecture allow flexible signal word length, because there is no specific bit-wide data path in this architecture.

Figure 6.5.2 shows the functional representation of the PE. The PE comprises a logic unit and a 128b DRAM column. A bit-serial Boolean function generator pitch-matched to the DRAM column is implemented in the logic [4]. Three latches (A, B, and C) provide inputs to the function generator. The function generator can produce all the 256 three-input Boolean functions, which are selected with eight control signals (f7-0). Dynamic logic is used in the function generator to reduce the logic silicon area to 18x500μm^2 [4]. The PE has two kinds of inter-PE communication paths. One is the path connecting two neighboring PEs in a row direction (right, left). The other is a 1b bus connecting PEs on the same column of the PE array for communication among four SIMD processors. A portion of a block of PE array with the inter-PE communication paths is shown in Figure 6.5.3. A 1b bus is arranged per column for inter-SIMD communication. The column bus is hooked by four PEs on a column and DMUX at the ADC output, and is connected to output MUX. One of the four PEs or DMUX drives the column bus, and any of the PEs and output MUX can receive bus data at a time.

The combination of SIMD/MIMD processing architecture allows variety of processing schem to meet various application tasks. One of the examples of processing schemes with this processing architecture for typical 3x3 kernel filtering is shown in Figure 6.5.4. A column of 4 SIMD processors performing two 3x3-kernel filtering is shown in this example. Each SIMD processor receives three rows of imager data row-by-row. A column bus transfers the result of the first 3x3-kernel filtering in a SIMD processor to two SIMD processors processing consecutive imager row data at a time. The second 3x3-kernel filtering starts right after a SIMD processor produces the result of the first 3x3-kernel filtering. As shown in Figure 6.5.4, four SIMD processors exactly share the total processing task for one frame image, since a processing task for one pixel is performed with one SIMD processor. By employing this processing scheme, the total processor silicon area becomes scalable with the increase of number of pixels. A processing scheme can be altered by changing the control signals for the SIMD processors. For example, a 4-stage pipeline scheme can be employed with this processor architecture. The versatile processor architecture meets the demand for use in a variety of image processing applications.

Figure 6.5.5 shows both the captured raw image and the Sobel filtered image to demonstrate imager performance. The imager chip affords ~220 operations per pixel for an 8b VGA image for typical two-input one-output operation like addition with 20MHz clock. A die micrograph is shown in Figure 6.5.6. Since the number of pixels in this experimental chip (128x128) is much lower than VGA resolution (640x480), the chip aspect ratio appears high. However, the required silicon area occupied with this column parallel digital processor implemented as a full VGA chip is estimated as only ~60% of pixel array silicon area. The chip overview is shown in Table 6.5.1.

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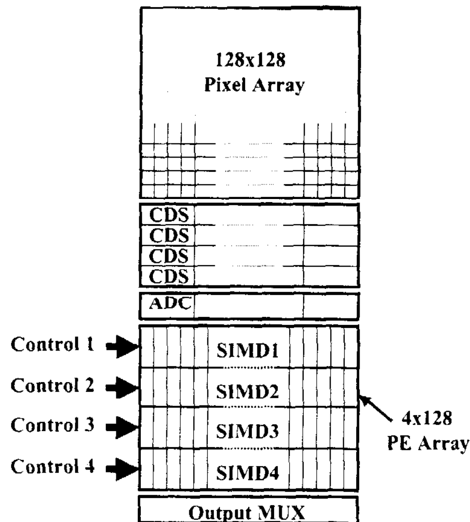


Figure 6.5.1: Imager chip configuration.

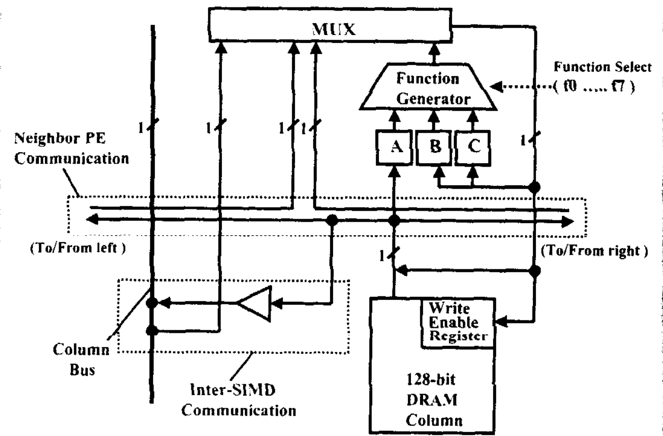


Figure 6.5.2: Functional representation of processing element (PE).

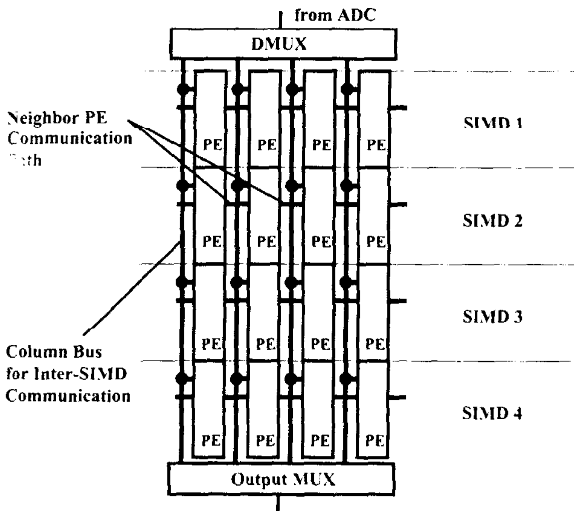


Figure 6.5.3: Inter-PE communication path.

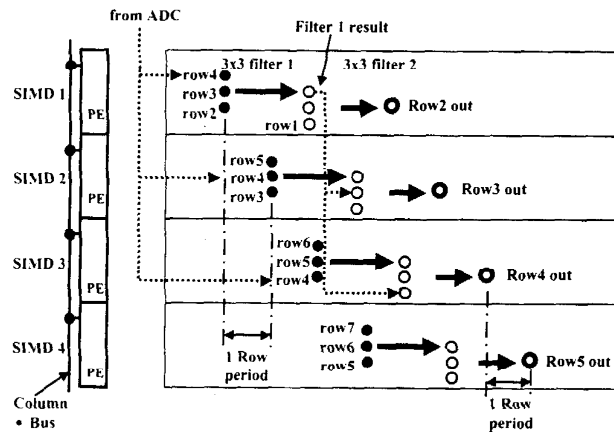
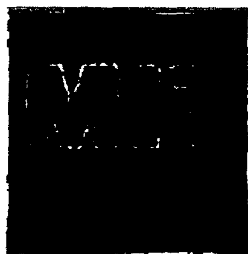


Figure 6.5.4: Processing scheme example.

(a) Raw image



(b) Sobel filtered image

Figure 6.5.5: Reproduced images from the imager chip. Raw image (a), and edge image with Sobel filtering (b).

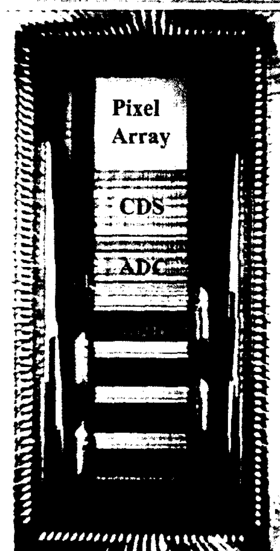


Figure 6.5.6: Imager die micrograph.

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