Application Note AN2xxx

A Neutral Grounding Resistor Monitor

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Summary
A Neutral Grounding Resistor (NGR) limits ground fault currents in local power distribution systems. This application packs a PSoC with functions to protect against an unhealthy NGR and too high fault currents. 'Dynamic Configuration Adaptation' combines modules in one analog column sharing the comparator bus. Separate configurations do self-calibration and graceful power-down handling.

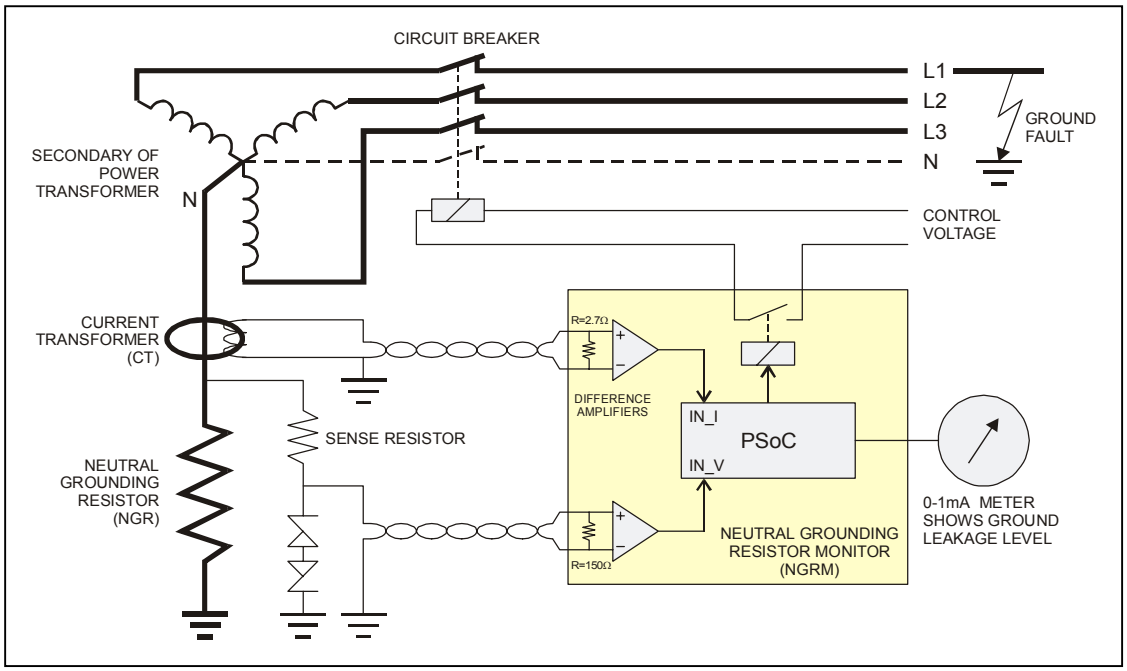

Figure 1: Power distribution system

Introduction

Figure 1 shows a three phase power distribution system with phase conductors L1, L2 and L3. A neutral conductor N may or may not be included. A power transformer with its secondary windings connected in star feeds the loads (not drawn). The scene could be laid for example in a factory or mine. Line to line voltage (V_{sys}) could be from 480V up to 11kV, 50 or 60Hz.

The star point of the transformer's secondary is connected to ground through a so called Neutral Grounding Resistor (NGR), the focal point of this Application Note. By the way, 'ground' in this respect means: all conductive parts that users can touch. The NGR's function is to limit fault currents in case a phase makes some form of contact with ground.

Maximum current flows through the NGR when the fault is a dead short. It is called the Let Through Current I_{lt}. I_{lt} is a design parameter that one chooses when laying out the distribution system. When I_{lt} flows, the voltage across the NGR is $V_{sys}/\sqrt{3}$, the system's line to neutral voltage.

The advantage of having fault currents limited is that it is not necessary to trip the circuit breaker instantaneously in case of a ground fault. Some time may elapse, normally in the order of 0.5 to 3 seconds. In that time the fault may prove to clear itself, and no activity was ever interrupted. The properties of power cabling and the power handling capability of the NGR will determine how long a fault can be tolerated before the circuit breaker must eventually be operated.

Resistive grounding works only as long as the NGR remains in good condition. A bad low-resistance NGR could cause burnt out cabling in case of a fault. Too high a resistance could let a ground fault go unnoticed. A next fault could then mean a short between phases. The NGR Monitor (NGRM) described in this Application Note protects against these horrors by continuously measuring the NGR's resistance. It trips the circuit breaker should an abnormal value be detected. As a bonus it also trips in case a ground fault does not clear itself in time.

Design requirements

The NGRM was to be based on an existing instrument, designed around an 8051 microcontroller derivative. It contained around 220 components on three printed circuit boards, and was relatively difficult to build. The PSoC approach was selected to innovate the product and improve on all these factors. The final result was a new, much lower cost product, having about 90 components on just one board. Production started end of February 2004.

Here is a list of the technical requirements for the design. Please refer to figure 1.

1. System voltages V_{sys} are standard values. Per V_{sys} there is a separate sense resistor version that cooperates with the NGRM's input resistor to scale down the measured voltage to one value. (The sense resistor contains back to back zeners to limit output voltage when the NGRM is not connected).
2. Let Through Currents I_{lt} to be covered are 5 to 400A in several steps, all using the same 1000:1 CT.
3. To be able to measure resistance, one has to have some current. Fortunately there is always a certain minimum amount of leakage current flowing through the NGR due to capacitive coupling of L1, L2 and L3 to ground. The NGRM has to be able to use exactly that current to measure resistance reliably, down to approximately 1% of full range; that is 1% of I_{lt} for current, and 1% of $V_{sys}/\sqrt{3}$ for voltage. Together with requirement no. 2, this means a dynamic range for reliable current measurement of 0.01x5A to 1.00x400A, or 1:8000 !
4. Safety regulations require that the user must be able to ground the CT's secondary.
5. When the power transformer is switched on, high transient voltages may develop even across parts of the ground grid. The NGRM has to be able to withstand these.
6. Ground Fault trip levels should be from 5 to 50% of I_{lt} in several steps, and trip delays from 60ms to 2s in several steps.
7. Resistor Fault trip levels (i.e. % deviation from nominal value) do not have to be precise; a value around 50% will be sufficient. Trip delay can be fixed at 1.5s.
8. The measured actual value of ground leakage should be shown on a 0-1mA DC current output.
9. The trip relay should power up in the last known state (i.e. the state it had before power went down).
10. Operating temperature range from –25 to +60°C.
11. Power consumption should be minimal to allow for a low cost wide input range AC/DC supply.

Design considerations

PSoC changes the life of a designer. Where every additional function had to be paid for in the past, one is now challenged to get them for free by utilizing the onboard resources to the max. In an attempt to master the art of efficiently assigning functions to PSoC blocks, one will go through trial and error cycles. Many decisions will be taken and undone. A PSoC block may be instructed to do x today and y tomorrow. But eventually everything will freeze into one or several configurations.

In able to learn from this design experience it is helpful to write down the major considerations that led to the final solution. For the NGRM the list below was compiled.

- The CT load resistance has to remain below about 3Ω to achieve good linearity over the full dynamic range. So we have to be able to deal with very low input voltages: 1% of 5A through the CT generates only 0.14mV across 2.7Ω. Signals will therefore be distorted and noisy, especially in these harsh environments. So we need high gains and good filtering.
- To achieve high gains in the PSoC, we will have to combine the gains of an input amplifier (PGA) and a filter.
- High gains mean DC offsets, limiting dynamic range. A PGA at gain=48 may generate 0.5V offset, and an LPF2 may generate 0.4V, together limiting dynamic range by 70%. The solution to avoid this without using external components is: a band pass filter (BPF2) rather than a low pass filter.
- The BPF2 has to work at a relatively low center frequency (50-60Hz). To avoid problems with internal PSoC leakage currents, Cypress advises to maximize the clock frequency by setting C2=C3=1. The Filter Design Spreadsheet shows that with C4=16 and an Over Sampling Ratio of 200 we get a Q of almost 2 and a gain of precisely 2xC1. The latter is a very attractive feature, since for different I_{lt} settings we need to be able to set different gains. Also, since measuring accurately down to 1% of full scale is required, it will prove helpful to dynamically switch to a higher gain for low input levels. The BPF2 is the ideal candidate to do this gain switching, since it can precisely switch to a gain that is a power of 2 higher (e.g. 2 and 8, or 6 and 24). That makes software processing that much easier.
- CT and NGR are grounded and high transients between grounded parts are possible. Some AC ground differentials may be expected under steady state conditions as well. At the same time the input signal may be very low as shown before. All this means that we need differential input amplifiers with excellent CMRR together with high common mode voltage withstand capability, a matter that cannot be left to the PSoC. Fortunately high grade difference amplifiers with integrated precision resistors withstanding several hundred volts common mode can be found on the marketplace.
- To avoid multiplexing and routing issues, the DUALADC module was selected. The two A/D converter blocks can be placed such that they can pick up their signals where necessary, and they can achieve a sample time of say 1ms at good resolution. Such a sample time would be adequate to meet the 60ms Ground Fault trip delay requirement.
- The user needs a settable I_{lt}. For a given I_{lt} one would like to scale the current signal such that the top of the sine just hits the A/D converter's Vref. But given the discrete set of possible input gains (i.e. PGA + BPF2 gains), one cannot do better than select gains such that the top of the sine (Vtop) is as high as possible without exceeding Vref. Now, setting α=Vtop/Vref, one has to live with the fact that α varies per I_{lt} setting. What is needed here is a means of deducting from a given value of I_{lt} what the optimum values for PGA gain and BPF2 gain are, and of calculating what the resulting value of α is. An Excel spreadsheet was developed that does exactly that. It comes as a separate file Ngrm.xls. The spreadsheet contains a lot of explanation, and can be modified for comparable situations.
- For very low values of voltage and current, it becomes increasingly difficult to establish the resistance of the NGR. This is because noise sources such as common mode errors, AC supply feedthrough and filter noise (PSoC's filters are especially noisy in the low frequency domain) become more and more influential. (DC offset errors stemming from filter and A/D converter do not have to play a predominant role, since they can be filtered out in software). The conclusion is, that when both voltage and current measurements fall below a certain limit, it will be necessary to refrain from tripping, no matter what the exact measured values are. The NGR is simply not being monitored then. The existence of an 'NGR not monitored' mode does not limit the usefulness of the system. First of all capacitive leakage currents are normally large enough to prevent the system from dwelling there. Otherwise, the NGR being good or bad, any significant ground fault will immediately cause a voltage and/or current large enough to leave this mode of operation, thereby restoring supervision of the NGR when it becomes necessary.

- A test signal can elegantly be generated without any additional hardware by pulling the voltage input IN_V (on the PSoC) up and down in a rhythm close to 50 and 60 Hz by means of the input pin's pull-up and pull-down resistors. This presumes that the input is driven via some resistance, but that is desirable anyway since a resistor with an added capacitor make up a nice pre-sampling filter for the BPF2 (which is, after all, a sampling structure). With the test signal active as a result of the user pressing the test button, the system should trip on Resistor Fault, seeing an unbalanced voltage and current. This is considered sufficient proof for correct operation: the trip circuit works, the voltage channel works, and when subsequently the system monitors the NGR and does not trip, the current channel cannot but work correctly as well.
- To minimize power consumption, a latched type output relay was selected. Such a relay is controlled by a 10ms pulse when changed over only, so power consumption is virtually nil. However, the relay must be left reliably in a known state when supply voltage is lost, so it calls for a Power Fail recognition mechanism. The power supply's buffer capacitor must be able to still trigger the relay's coil when the supply is lost.
- The routine that handles shutdown after Power Fail is the ideal place to write the relay status (not tripped or tripped, plus reason of trip) to flash emulated e2prom. This way the available number of flash write cycles is preserved as much as possible, especially if the status is only written when different. The stored status is used at the next power up to restore the relay. Since ambient temperature can be well below 0°C, the temperature sensor is needed when writing to flash. A separate configuration 'Shutdown' will be loaded containing just the FlashTemp module.
- The current source output can be made with a PGA and a few resistors plus a capacitor, controlled from a PWM signal with varying duty cycle. Unlike other signals in the system, the accuracy of the PWM signal will depend on the accuracy of the supply voltage Vcc. Therefore a separate configuration 'Calibrate' was made that automatically calibrates the current output during power up, using the accuracy of Vref. Not a single extra external component is necessary.

The hardware

Dipswitches are used for user settings of I_{lt}, Ground Fault trip level and Ground Fault trip delay. Two pushbuttons perform trip reset and test functions.

LEDs show

- Whether the PSoC is running (flashing 1s on, 1s off)
- What the trip cause is (Ground Fault or Resistor fault or both)
- Whether the NGR is being monitored or not; if both current and voltage are lower than approximately 1% of full scale, a resistance value cannot be determined, and the LED is on

Except for the differential input buffers and a relay driver chip, all functionality was packed inside the PSoC.

PSoC configuration and software

The NGRM's base configuration 'ngrm' is shown in figure 2, and the auxiliary configurations 'Calibrate' and 'Shutdown' are shown in figures 3 and 4 respectively.

In the base configuration, not all modules necessary to fulfill all tasks would fit, because of resource conflicts. In particular, the Power Ok/Fail comparator and one of the DUALADC's blocks both needed the comparator bus. A technique baptized 'Dynamic Configuration Adaptation' was used to enable the blocks to share the bus and coexist in the same column. This is detailed in the next section.

The DUALADC's interrupt routine can elegantly be used to create the approximately 1ms real time clock: the module's clock is set at 4800kHz, and then the CALCTIME parameter is calculated using the datasheet to arrive at the selected time. The adcint.asm interrupt file is modified to call a C-function clock(). This is the only place where the Library Source is modified. clock() then handles all the high speed processing: Power Ok/Fail handling (through Dynamic Configuration Adaptation), signal rectification and filtering, switch debouncing, test signal generation, ground fault tripping and dynamic amplification switching.

The main program main() can do the low speed processing in a background loop: Resistor Fault recognition and controlling the 1mA current output. Main() can also harbor the i, j and α values from the ngrm.xls spreadsheet in lists of defines and then the program can be written such that any constant needed (derived from i, j and α) is calculated automatically (by the C-compiler).

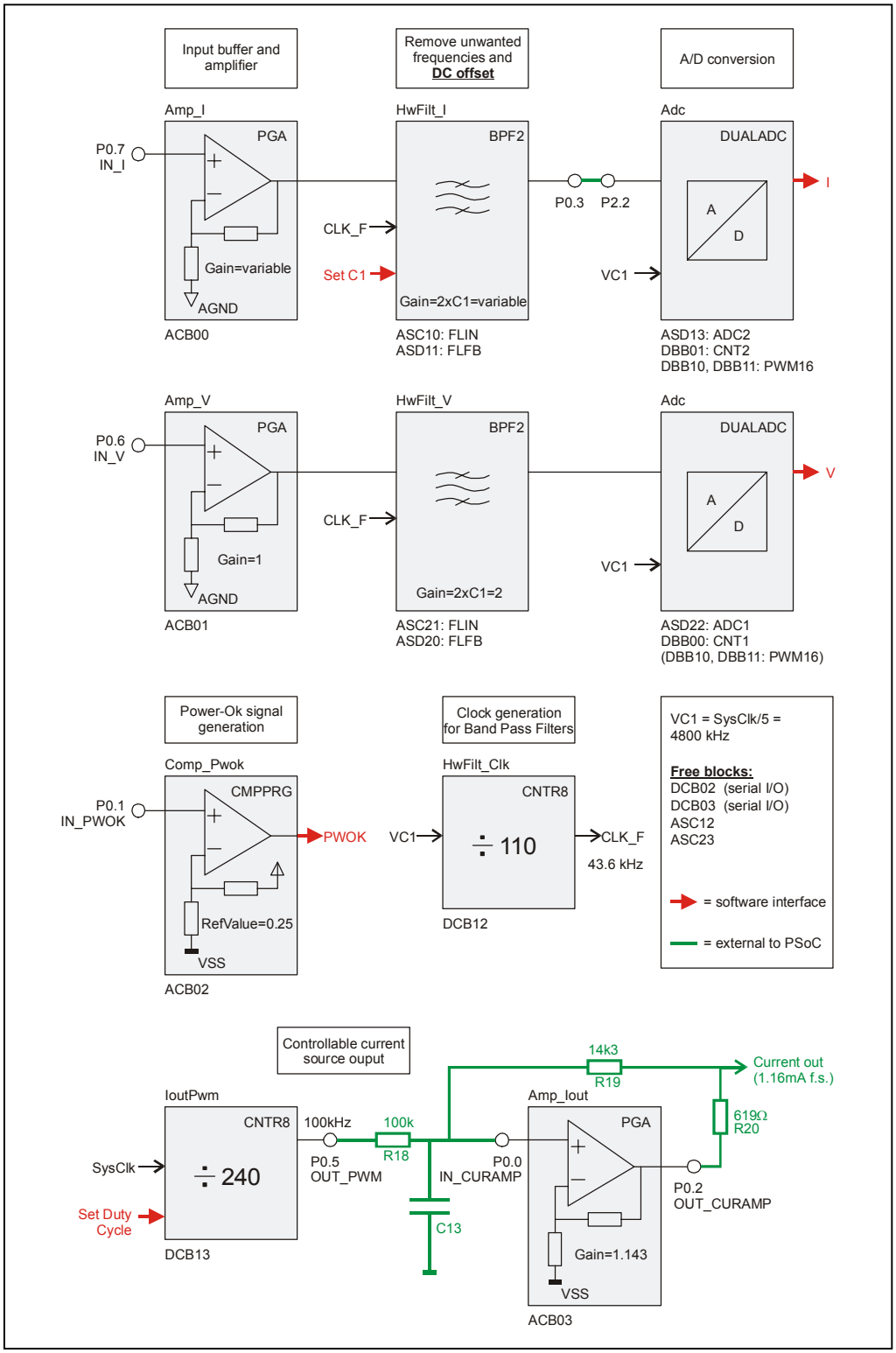

Figure 2: Base configuration

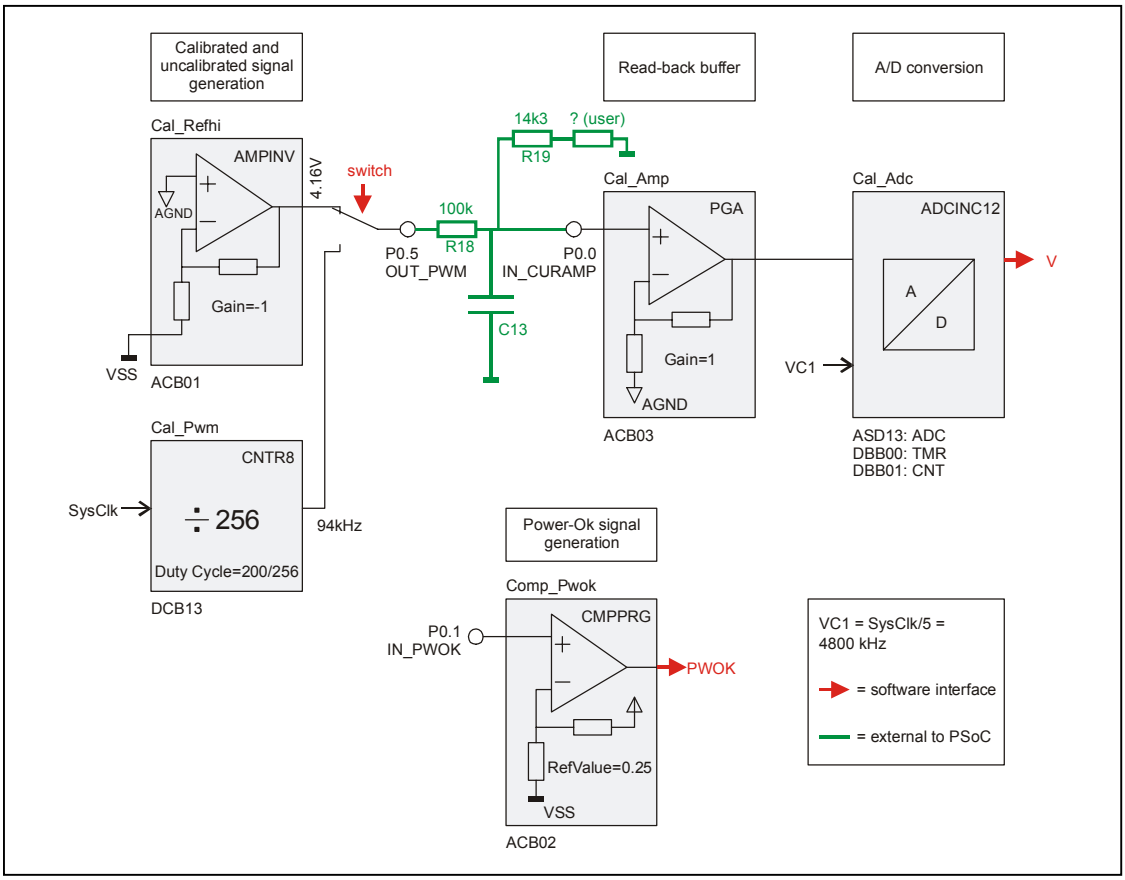

Figure 3: 'Calibrate' configuration

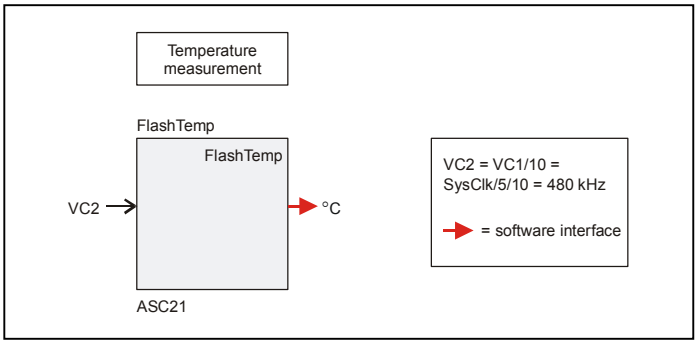

Figure 4: 'Shutdown' configuration

Dynamic Configuration Adaptation

It may happen that a configuration has unused analog PSoC blocks that cannot be assigned to a function as intended because of conflicting resource allocations. Sometimes a reorganization of blocks may help, and in other cases the problem can be solved by introducing an auxiliary dynamic configuration. But if the loading of a different configuration destroys a currently important status, that is just not possible. As a further option, the existing configuration may be adaptable 'on the fly' to make the impossible possible.

In the NGRM's design, the two ADC blocks of the DUALADC module use the comparator buses of columns 2 and 3 to control their respective CNTR blocks in the digital array. The Power Ok/Fail CMPPRG module still had to find a place in one of these columns, but for the microcontroller to be able to read the output of the comparator (interrupt driven or not), the comparator has to be connected to the same bus. Now, since the DUALADC is used to generate the real time clock (of approximately 1ms), one cannot afford to replace the configuration with a different one; that would destroy the contents of the timer that does the actual timekeeping.

The way out here is that during the 'CALCTIME period' the DUALADC holds its counters disabled through the very comparator bus. This opens the possibility to disconnect the ADC block from the bus, connect the CMPPRG block to it, read its state, disconnect again and reconnect the ADC. Some precautions are necessary not to corrupt the ADC's counter. The exact coding in clock() is presented below . Sampling the Power Ok/Fail signal once every millisec is fast enough.

The software operated switch in the 'Calibrate' configuration (figure 3) could be regarded as a form of Dynamic Configuration Adaptation. However, the objective here could also be achieved with standard Dynamic Reconfiguration.

Epilogue

Although the PSoC is packed with functions, care was taken to keep two digital blocks free that can be used to add serial I/O facilities. Many other additions could be made: an alarm relay, alarm and trip levels on Ground Fault currents, more dipswitches, selectable failsafe relay behavior (trip at loss of power supply), etc. etc.

```
void clock (void)
{
  //************************* DYNAMIC CONFIGURATION ADAPTATION *************************
  // Sample the Power OK status by removing Adc's comparator output from the column 2
  // comparator bus, then enabling Comp_Pwok's output to that bus and reading it; this can be
  // safely done, because Adc's counters are disabled by it's PWM, see the DUALADC datasheet
  DBB00CR0 &= ~0b1;          // Disable DUALADC's counter 1
  DBB01CR0 &= ~0b1;          // Disable DUALADC's counter 2
  ASD22CR2 &= ~(0b1<<6);     // Disable Adc comparator output
  ACB02CR1 |= (0b1<<6);      // Enable Comp_Pwok output
  DEC_CR0 &= ~(0b1<<4+2);    // Disable the incremental gate (2=column no.); this enables
                             // the gate to the column's LUT and thus the uC (and the
                             // DUALADC counter's enable input!)
  pwok = FALSE;
  for (k=0; k<5; k++)        // Noise filtering: only fail if all samples fail
  {
    WAIT(10);                // Wait 10 usec for latch updates and for filtering purposes
    if (CMP_CR0 & CMP_CR0_COMP2)
    {
      pwok = TRUE;
      pwok_int_ena = TRUE;  // Enable the shutdown 'interrupt' as soon as power becomes ok
      break;
    }
  };
  DEC_CR0 |= (0b1<<4+2);     // Re-enable the incremental gate (2=column no.); this disables
                             // the gate to the column's LUT and thus the DUALADC's counter,
                             // since the PWM still outputs a zero here, being within CalcTime
  ACB02CR1 &= ~(0b1<<6);     // Disable Comp_Pwok output
  ASD22CR2 |= (0b1<<6);      // Re-enable Adc comparator output
  DBB00CR0 |= 0b1;           // Re-enable DUALADC's counter 1
  DBB01CR0 |= 0b1;           // Re-enable DUALADC's counter 2
  //********************** END OF DYNAMIC CONFIGURATION ADAPTATION ***********************

  if (!pwok && pwok_int_ena) shutdown();   // Loads Shutdown configuration; never returns

  // <high speed processing is done here>
}
```

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