FM209 and FM214
9600/14400 bps MONOFAX® Modem Family

Designer's Guide

Order No. 1175
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NOTICE

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1. INTRODUCTION

The Rockwell FM209 and FM214 MONOFAX® facsimile modem family offers 9600 bps and 14400 bps half-duplex capability with options supporting voice and audio codecs, full-duplex and half-duplex speakerphone, speaker independent and speaker dependent automatic speech recognition, Type I and Type II Caller ID, and V.23 full duplex modes. The modem models are identified in Table 1-1.

These functions are supplied in a single device. The Rockwell FM209 and FM214 MONOFAX facsimile modem family is packaged in a 128-pin TQFP containing a Digital Signal Processor (DSP), a Primary Integrated Analog (PIA) codec, and a optional Secondary Integrated Analog (SIA) codec (-S option).

This device family enables cost-effective development of a common facsimile machine design featuring digital answering machine, full-duplex speakerphone and automatic speech recognition functionality.

1.1 FACSIMILE MODEM

The modem can operate at 14400, 12000 (FM214 family only), 9600, 7200, 4800, 2400, or 300 bps, and can perform HDLC framing per T.30 at all rates. A programmable DTMF detector, three programmable tone detectors, V.21 Channel 2 FSK 7E flag detector, Caller ID demodulator and ring detector are provided.

1.2 VOICE AND AUDIO CODECS (-V OPTION)

The voice coder/decoder (codec) compresses voice at an average rate of 2.9 kbps which provides 24 minutes of stored voice messages in 4 Mbits of memory. This voice codec allows the host controller to efficiently store and playback digital incoming messages (ICMs), outgoing messages (OGMs) and conversations (-VS option).

The ADPCM audio codec compresses audio signals (music/voice) at 32 kbps or 24 kbps and the PCM audio codec records audio signals at 128 kbps or 64 kbps for highest fidelity coding and reproduction.

Selectable error correction coding allows storage in audio grade RAMs (ARAMs). Echo cancellation techniques employed during playback allow DTMF, tone and Type II Caller ID CAS detection during voice/audio codec operation to support user selectable features. The coder can record messages from the PIA or SIA. The decoder can play back messages to the PIA or both the PIA and SIA. Dual/single tone transmission is available when the decoder is disabled.

1.3 SPEAKERPHONE (-S OPTION)

The full-duplex speakerphone provides hands-free telephone voice communication employing acoustic echo cancellation and line echo cancellation. It also supports full-duplex intercom voice communication employing dual acoustic echo cancellation techniques. The half-duplex speakerphone provides hands-free telephone/intercom voice communication with exceptionally high gain.

Conversation recording and message playback are supported during speakerphone operation (-VS option). Also supported are DTMF detector, tone detectors, and Caller ID Type II CAS detection.

The speakerphone algorithm constantly adjusts its parameters to deliver the best performance during real-time conditions, allowing automatic fallback from full-duplex to pseudo-duplex. The host controller can easily set up the speaker mute, microphone mute, automatic gain control (AGC) enable/disable, microphone level, line level, speaker volume, tone transmit, and handset functions.

1.4 AUTOMATIC SPEECH RECOGNITION (-R OPTION)

The Automatic Speech Recognition (ASR) consists of the following:

- Speaker Independent (SI) North American English isolated word recognition for a predefined 69-word vocabulary list.
- Speaker Dependent (SD) isolated word training.
- SD isolated word recognition functions.

More information on ASR features is available in an Application Note. Contact your sales representative.

1.5 V.23 FULL-DUPLEX MODEM AND CALLER ID

Both full-duplex transmit and receive (with asymmetric 1200/75 bps connection) and half-duplex (1200 bps) asynchronous V.23 are supported, as well as both serial and parallel interfaces to the modem. The V.23 algorithm includes an optional, programmable, receive compromise equalizer which is active in both V.23 and Caller ID (V.23 Receive only) modes.

Common applications for V.23 include France's Minitel and Japan's Lowest Cost Routing.

Table 1-1. Modem Models and Supported Features

Modem	Max. Data Rate	Voice and Audio Codecs (-V)	FDX/HDX Digital Speakerphone (-S)	Automatic Speech Recognition (-R)
FM214-VSR	14.4 kbps	●	●	●
FM214-VS	14.4 kbps	●	●	–
FM214-V	14.4 kbps	●	–	–
FM214	14.4 kbps	–	–	–
FM209-VSR	9.6 kbps	●	●	●
FM209-VS	9.6 kbps	●	●	–
FM209-V	9.6 kbps	●	–	–
FM209	9.6 kbps	–	–	–

1.6 FEATURES

- Group 3 facsimile transmission/reception
  - ITU-T V.17 and V.33 (FM214 models)
  - ITU-T V.29, V.27 ter, T.30, V.21 Channel 2, T.4
  - ITU-T V.17 and V.27 ter short train
  - HDLC framing at all speeds
  - Receive dynamic range: 0 dBm to –43 dBm
  - Automatic adaptive equalization
  - Fixed and programmable digital compromise equalization
  - DTMF detect and tone detect
  - ITU-T V.21 Channel 2 FSK 7E Flag Detect
  - Ring detector
  - Programmable transmits level
  - Programmable single/dual tone transmission
- Voice codec (-V Option)
  - 24 minutes of voice storage per 4 Mbit memory
  - Near toll quality voice recording and playback
  - Programmable AGCs
  - Programmable line/microphone input and line/speaker output filters
  - Error correction coding allows ARAM usage
  - DTMF detect, tone detect, and tone transmit
  - Type II Caller ID CAS detection
  - Pitch synchronized fast and slow playback
  - Near-end echo cancellation
- ADPCM Audio codec (-V Option)
  - High fidelity recording and playback of audio signals
  - 32 kbps and 24 kbps
  - Programmable AGCs
  - Programmable line/microphone input and line/speaker output filters
  - DTMF detect, tone detect, and tone transmit
  - Type II Caller ID CAS detection
  - Near-end echo cancellation
- PCM audio codec
  - 128 kbps and 64 kbps
  - DTMF detect and tone detect
  - Type II Caller ID CAS detection
  - Near end echo cancellation
- Full-duplex speakerphone (-S Option)
  - Acoustic echo cancellation
  - Line echo cancellation or secondary acoustic echo cancellation
  - Programmable microphone and speaker AGCs
  - Programmable line and speaker output filters
  - Microphone and speaker volume control and muting
  - Auto fallback toward pseudo-duplex operation under poor operating conditions
  - Programmable handset echo simulation in handset operation
  - High gain half-duplex mode
  - Intercom support
  - DTMF detect and 3 tone detectors
  - Type II Caller ID CAS detection
  - Two dual tone transmitters
  - Conversation recording and message playback with Voice or ADPCM Audio codec (-VS option)

- Automatic Speech Recognition (-R Option). More information is provided in an Application Note. Contact your sales representative.
  - Speaker Dependent (SD) and Speaker Independent (SI) isolated word recognition
  - SI Vocabulary (English) for hands-free voice control of dialing, telephone answering machine and fax functions
  - Active word list for recognition selected by host controller
  - Supports input from microphone, local handset, and telephone line
  - SI word models trained off-line and stored in DSP ROM
  - SD word models trained in real-time, stored in (off-chip) NVRAM and downloaded to DSP RAM
  - Supports 30 Active simultaneous SD words
  - SD training - single utterance or multiple utterances
  - 2.5 second maximum speech length for SD training
  - Rejection capability provided for SI mode
- Room Monitor
  - DTMF detect, tone detect and tone transmit
  - Type II Caller ID CAS detection
  - Near end echo cancellation
  - Monitor recording and message playback with Voice or Audio Codec (-V option)
- V.23 and Type I Caller ID
  - Full-duplex modes:
    TX = 75 bps, RX = 1200 bps
    TX = 1200 bps, RX = 75 bps
  - Half-duplex mode:
    TX = RX = 1200 bps
  - Serial and parallel data modes
  - Programmable parallel data mode
  - 5, 6, 7, or 8 data bits
  - 1 or 2 Stop bits
  - Mark, Space, Even, or Odd Parity
  - Break function
  - Transmitter squelch
  - Compromise equalizer
- Programmable interface memory interrupt
- Eight General Purpose Input (GPI) and eight General Purpose Output (GPO) pins for host assignment
- DTE interface: two alternate ports
  - Selectable microprocessor bus (6500 or 8085)
  - ITU-T V.24 (EIA/TIA-232-E compatible) interface
- TTL and CMOS compatible
- 3.3V/5V operation
- Power consumption (see Table 2-5):
  - Operating Mode: 200 mW (Basic), 275 mW (-V option), 300 mW (-VS option)
  - Sleep Mode: 1 ma (Basic, -V option, and -VS option)
- Packaging
  - 128-pin TQFP (thin quad flat pack)

1.7 TECHNICAL SPECIFICATIONS

1.7.1 Modem

Function	Description
Configurations, Signaling Rates and Data Rates	The selectable modem configurations, along with the corresponding symbol (baud) rates and data rates, are listed in Table 1-3.
Scrambler/Descrambler	The modem incorporates a self-synchronizing scrambler/descrambler in accordance with ITU-T V.17 (FM214 models), V.33 (FM214 models), V.29, and V.27 ter recommendations, depending on the selected configuration.
Data Encoding	Data encoding conforms to ITU-T recommendations V.17 ter (FM214 models), V.33 (FM214 models), V.29, V.27 ter, V.21 Channel 2, V.23 and CID receive.
Fixed Digital Cable Compromise Equalizer	Compromise equalization can improve performance when operating over low quality lines. The modem has a selectable fixed digital compromise cable equalizer in the high speed receive and transmit data paths. The modem includes an optional host programmable Receive Compromise Equalizer for V.23 1200 bps reception and Caller ID mode.
Transmitted Data Spectrum	Transmitted data spectrum is shaped in the baseband by an excess bandwidth finite impulse response filter (FIR) with the following characteristics: When operating at 2400 baud, the transmitted spectrum is shaped by a square root of 20% raised cosine filter. When operating at 1600 baud, the transmitted spectrum is shaped by a square root of 50% raised cosine filter. When operating at 1200 baud, the transmitted spectrum is shaped by a square root of 90% raised cosine filter. The out-of-band transmitter energy levels in the 4 kHz – 50 kHz frequency range is below –55.0 dBm.
Transmit Level	The transmitter output (TXA) level is programmable in the DSP RAM from 0 dBm to –15.0 dBm. The modem adjusts the output level by digitally scaling the output to the transmitter's digital-to-analog converter.
Turn-on Sequence	Transmitter turn-on sequence times are shown in Table 1-4.
Receive Dynamic Range	The receiver satisfies PSTN performance requirements for received line signal levels from 0 dBm to –43 dBm measured at the Receiver Analog Input (RXA) input. An external input buffer with 6 db loss recommended must be supplied between RXA and RIN. The default values of the programmable Received Line Signal Detector (RLSD#) turn-on and turn-off threshold levels are –43 dBm and –48 dBm, respectively. The RLSD# threshold levels can be programmed over the following range: Turn on: –10 dBm to –47 dBm Turn off: –10 dBm to –52 dBm

Function	Description
Automatic Adaptive Equalizer	An adaptive equalizer in ITU-T V.17 (FM214 models), V.33 (FM214 models), V.29 and V.27 ter modes compensates for transmission line amplitude and group delay distortion.
Receiver Timing	The timing recovery circuit can track a ±0.01% frequency error in the associated transmit timing source.
Carrier Recovery	The carrier recovery circuit can track a ±7 Hz frequency offset in the received carrier.
Turn-off Sequence	Transmitter turn-off sequence times are shown in Table 1-5
Clamping	Received Data (RXD) is clamped to a constant mark whenever RLSD# is off.
V.23 Modem	The modem can transmit and detect Break signals (continuous Space). The Mark and Space frequencies are 1300 and 2100 Hz, respectively, for 1200 bps, and 390 and 450 Hz, respectively, for 75 bps. The modem transmitter output can be forced to zero. The modem includes an optional host programmable Receive Compromise Equalizer for V.23 1200 bps reception and Caller ID Mode. Default transmitter turn-on sequence time is shown in Table 1-2. See Section 4 for programming information.

Table 1-2. V.23 Default Turn-On and Turn-Off Sequences

Configuration	RTS On to CTS On	RTS Off to CTS Off
V.23 FDX	10.5 ms	2.2 ms

1.7.2 Tone Detectors and Generators

The tone detector signal path is separate from the main received signal path thus enabling tone detection to be independent of the receiver status. The tone detectors operate in all modes. The filter coefficients of each filter are host programmable in RAM.

The modem can generate voice-band single or dual tones from 0 Hz to 4800 Hz with a resolution of 0.15 Hz and an accuracy of 0.01%. Tones over 3400 Hz are attenuated. Dual tone generation allows the modem to operate as a programmable DTMF dialer.

Table 1-3. Configurations, Signaling Rates, and Data Rates

Configuration	Modulation[1]	Carrier Frequency (Hz) ±0.01%	Data Rate (bps) ±0.01%	Baud (Symbols/Sec.)	Bits /Symbol	Constellation Points
V.17/V.33 14400 [2]	TCM	1700 or 1800	14400	2400	6	128
V.17/V.33 12000 [2]	TCM	1700 or 1800	12000	2400	5	64
V.17 9600 [2]	TCM	1700 or 1800	9600	2400	4	32
V.17 7200 [2]	TCM	1700 or 1800	7200	2400	3	16
V.29 9600	QAM	1700	9600	2400	4	16
V.29 7200	QAM	1700	7200	2400	3	8
V.29 4800	QAM	1700	4800	2400	2	4
V.27 ter 4800	DPSK	1800	4800	1600	3	8
V.27 ter 2400	DPSK	1800	2400	1200	2	4
V.21 Channel 2 300	FSK	1650, 1850	300	300	1	–
V.23 receive HDX	FSK	1300, 2100	1200	1200	1	–
V.23 1200/75	FSK	1300, 2100, 390, 450	1200/75	1200/75	1	–
Type I Caller ID	FSK	1200, 2200	1200	1200	1	–

Notes:

1. Modulation legend:
   - QAM: Quadrature Amplitude Modulation
   - DPSK: Differential Phase Shift Keying
   - FSK: Frequency Shift Keying
   - TCM: Trellis-Coded Modulation
2. FM214 models only.

Table 1-4. Turn-On Sequence Times

Configuration	RTS# On to CTS# On	
	Echo Protector Tone Disabled	Echo Protector Tone Enabled
V.17/V.33	1395 ms	1602 ms
V.17 Short Train	144 ms	351 ms
V.29 Long Train	255 ms	443 ms
V.27 ter 4800 bps Long Train	710 ms	917 ms
V.27 ter 4800 bps Short Train	52 ms	259 ms
V.27 ter 2400 bps Long Train	945 ms	1152 ms
V.27 ter 2400 bps Short Train	69 ms	276 ms
V.21 Channel 2 300 bps	≤ 14 ms	≤ 14 ms

Table 1-5. Turn-Off Sequence Times

Configuration	Data and Scrambled Ones	No Transmitted Energy	Total
V.17 Long and Short Train/V.33	13.3 ms	20 ms	33.3 ms
V.29 Long Train	5 ms	20 ms	25 ms
V.27 ter 4800 bps Long and Short Train	7 ms	20 ms	27 ms
V.27 ter 2400 bps Long and Short Train	10 ms	20 ms	30 ms
V.21 Channel 2 300 bps	7 ms	0 ms	7 ms

Notes:

1. In parallel data mode, the turn-off sequence may be extended by 8 bit times.
2. In HDLC mode, the turn-off sequence may be extended by more than 8 bit times.

1.7.3 Voice Codec Mode (-V Option)

In the Voice Codec Mode, the modem can compress a voice message at an average rate of 2.9 kbps or at a fixed rate of 4.7 kbps and decompress a voice message at various pitch synchronized playback speeds. Optional error correction coding is available for use with ARAMs.

DTMF detect, tone detect, Type II Caller ID CAS detection and tone transmit functions are supported.

1.7.4 ADPCM Audio Codec Mode (-V Option)

The ADPCM Audio Codec Mode enables the host to record and playback audio (music/voice) with highest fidelity. The modem can compress an audio signal to 32 kbps or 24 kbps.

DTMF detect, tone detect, Type II Caller ID CAS detection and tone transmit functions are supported.

1.7.5 PCM Audio Codec Mode

The PCM Audio Codec Mode enables the host to transmit and receive 8-bit or 16-bit audio signals. In this mode, the host can access the analog-to-digital (A/D) converter (ADC) and the digital-to-analog (D/A) converter (DAC). Incoming analog audio signals can then be converted to digital format and digital signals can be converted to analog audio output.

DTMF detect, tone detect, Type II Caller ID CAS detection and tone transmit are supported.

1.7.6 Speakerphone Mode (-S Option)

The speakerphone Mode provides hands-free full-duplex or half-duplex telephone operation and intercom operation under host control. The host can separately control volume, muting, AGC, and tone generation in microphone and speaker channels. The speakerphone automatically recalculates loop control parameters to maintain duplexity and stability.

Conversation recording and message playback with voice codec or ADPCM audio codec are supported (-V option). DTMF detect, tone detect and Type II Caller ID CAS detection are also supported.

1.7.7 Automatic Speech Recognition (-R Option)

The Automatic Speech Recognition (-R option) performs of the following:

- Speaker Independent (SI) North American English isolated word recognition for a predefined 69-word vocabulary list
- Speaker Dependent (SD) isolated word training
- SD isolated word recognition functions

More information on ASR is available in an Application Note. Contact your sales representative.

1.7.8 Room Monitor Mode

The Room Monitor Mode allows the remote-end user to monitor the local room activity by listening to audio captured by the microphone connected to the microphone input of IA. Room monitor operation is supported in Voice Codec Mode and ADPCM Audio Codec Mode for room monitor recording and OGM playback.

DTMF detect, tone detect, Type II Caller ID CAS detection and tone transmit are supported.

2. HARDWARE INTERFACE SIGNALS

Any point that is active when exhibiting the relatively more negative voltage of a two-voltage system (0 VDC for TTL or –12 VDC for EIA/TIA-232-E) is called active low and is represented by a small circle at the signal point. Active low signals are indicated by a pound symbol (#). For example: RESET#. Edge-triggered clocks are indicated by a small triangle (DCLK). Open-collector (open-source or open-drain) outputs are denoted by a small half circle (signal IRQ1#).

A clock intended to activate logic on its rising edge (low-to-high transition) is called active high, while a clock intended to activate logic on its falling edge (high-to-low transition) is called active low. When a clock input is associated with a small circle, the input activates on a falling edge. If no circle is shown, the input activates on a rising edge.

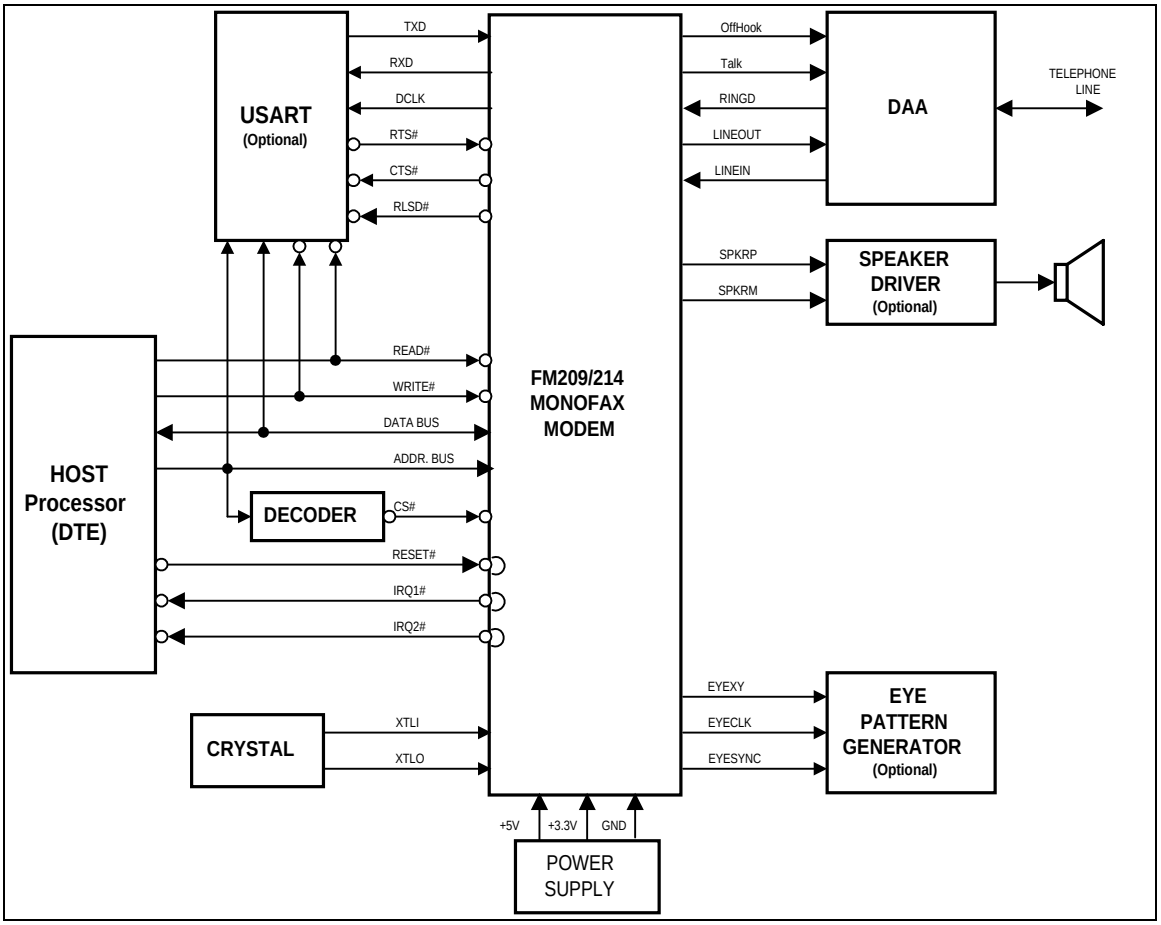


Figure 2-1. Modem Functional Interconnect Diagram (Fax)

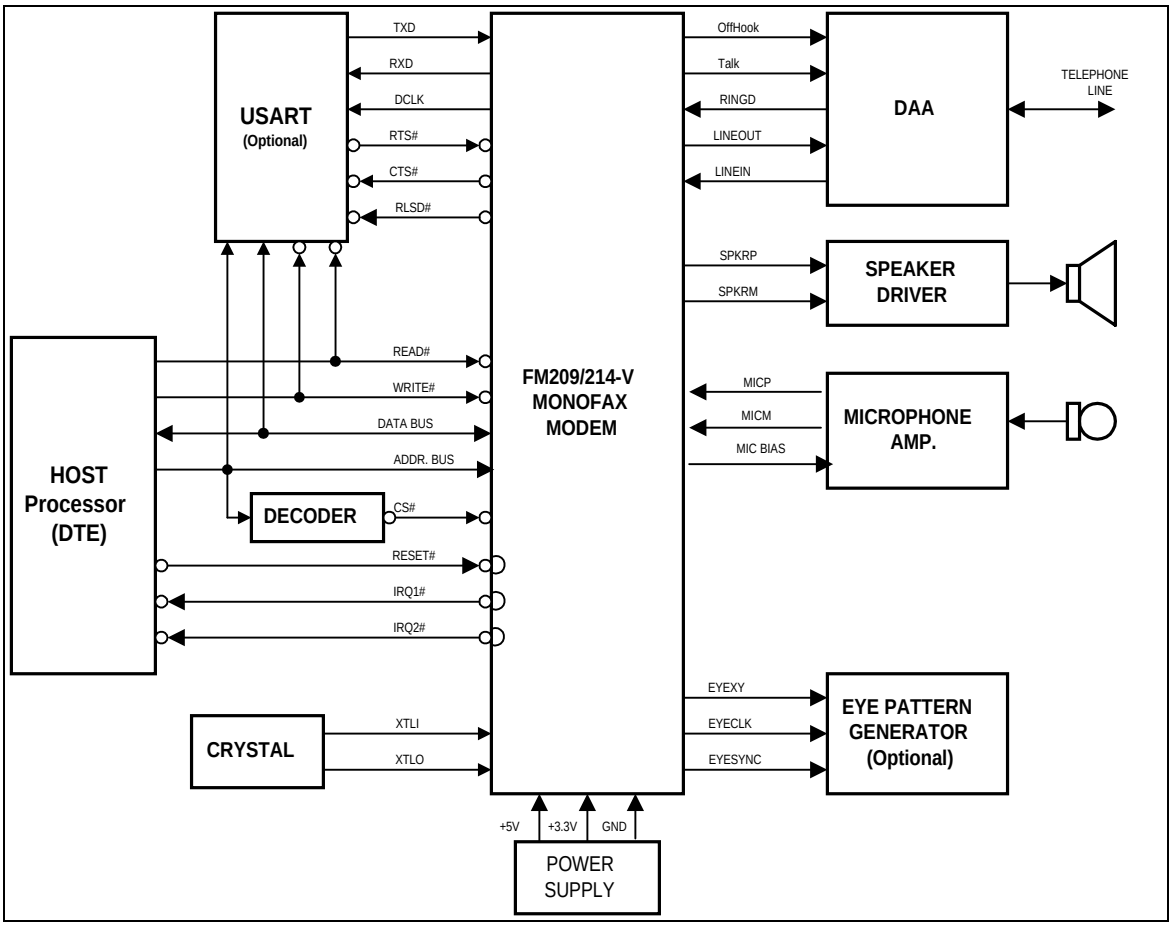


Figure 2-2. Modem Functional Interconnect Diagram (Fax and DTAM)

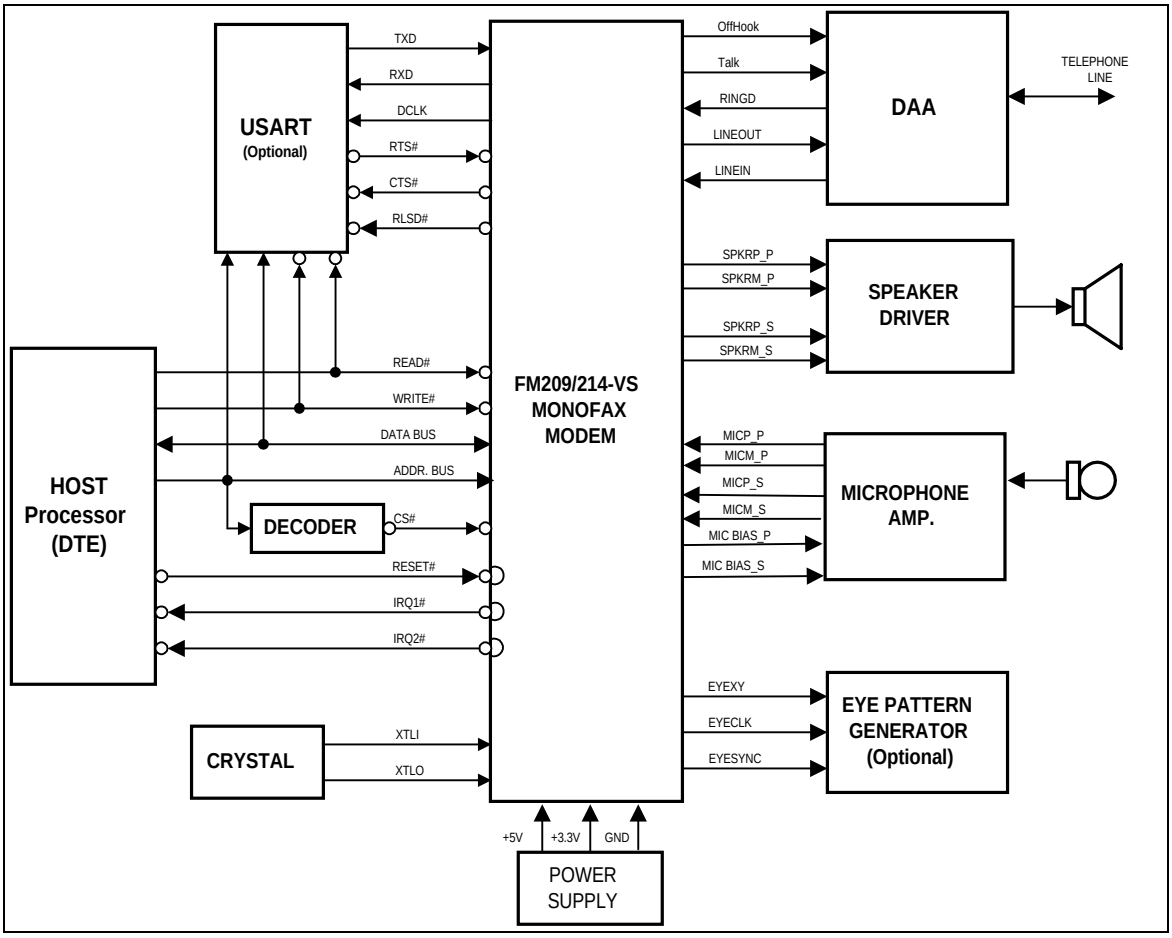


Figure 2-3. Modem Functional Interconnect Diagram (Fax, DTAM, and Speakerphone)

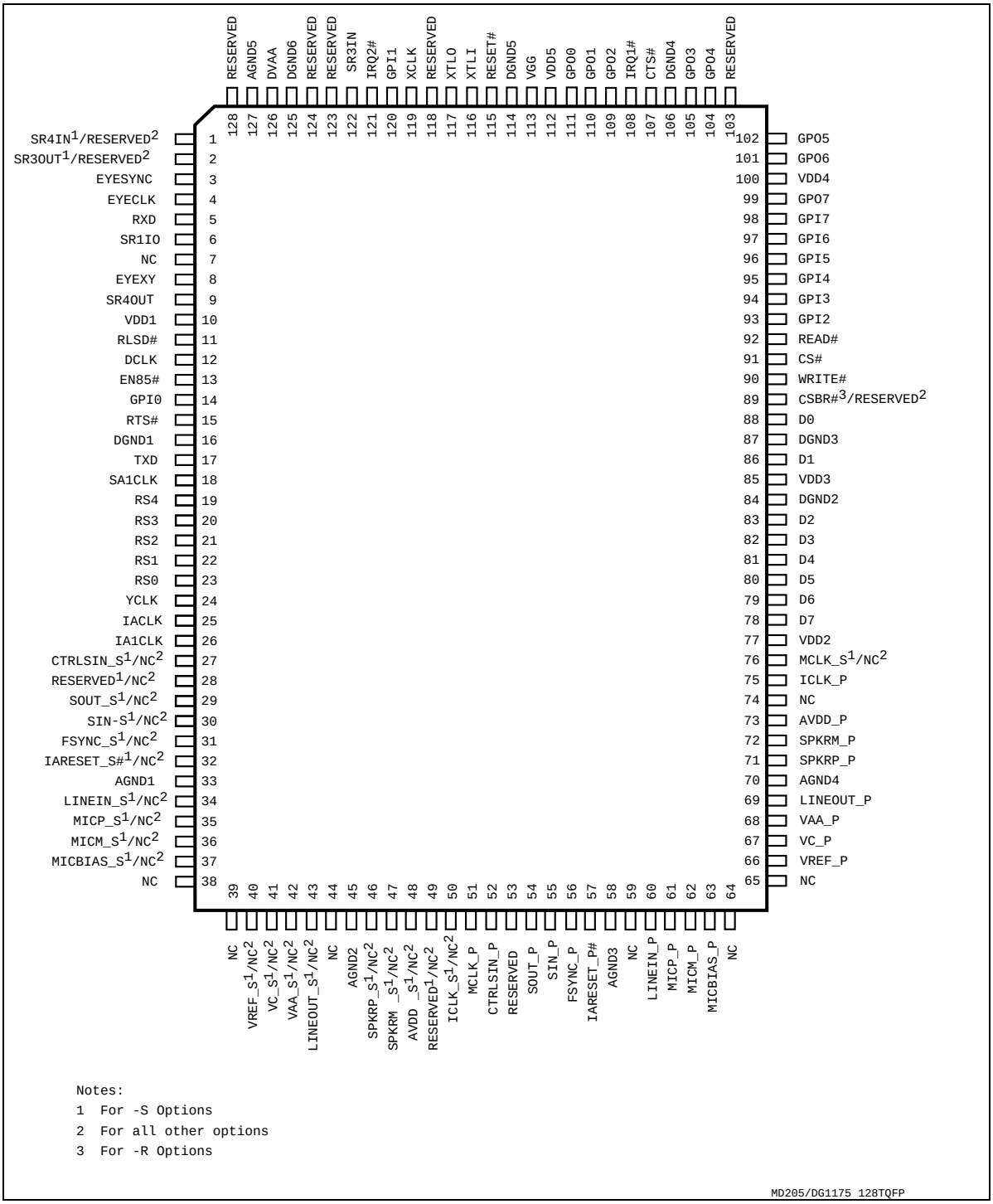


Figure 2-4. Modem Pin Signals - 128-Pin TQFP

Table 2-1. FM209/214 Modem Pin Signals - 128-Pin TQFP

Pin	Signal Label	I/O Type	Interface	Pin	Signal Label	I/O Type	Interface
1	SR4IN/RESERVED	MI	Modem Interconnect	51	MCLK_P	MI	Modem Interconnect
2	SR3OUT/RESERVED	MI	Modem Interconnect	52	CTRLSIN_P	MI	Modem Interconnect
3	EYESYNC	OA	Eye Pattern Circuit	53	RESERVED	MI	Modem Interconnect
4	EYECLK	OA	Eye Pattern Circuit	54	SOUT_P	MI	Modem Interconnect
5	RXD	OA	DTE serial interface	55	SIN_P	MI	Modem Interconnect
6	SR1IO	MI	Modem Interconnect	56	FSYNC_P	MI	Modem Interconnect
7	NC	-	No Connection	57	IARESET_P#	MI	Modem Interconnect
8	EYEXY	OA	Eye Pattern Circuit	58	AGND3	GND	IA Analog Ground
9	SR4OUT	MI	Modem Interconnect	59	NC	-	No Connection
10	VDD1	PWR	3.3V Digital Supply for DSP	60	LINEIN_P	I	Line Interface
11	RLSD#	OB	DTE Serial Interface	61	MICP_P	I	Microphone Input
12	DCLK	OB	DTE Serial Interface	62	MICM_P	I	Microphone Input
13	EN85#	IA	Host Parallel Interface	63	MICBIAS_P	O	Microphone Bias Output
14	GPI0	IA	Host Parallel Interface	64	NC	-	No Connection
15	RTS#	IA	DTE Serial Interface	65	NC	NC	No Connection
16	DGND1	GND	DSP Digital Ground	66	VREF_P	MI	Modem Interconnect
17	TXD	IA	DTE Serial Interface	67	VC_P	MI	Modem Interconnect
18	SA1CLK	MI	Modem Interconnect	68	VAA_P	PWR	5V Analog Supply for IA
19	RS4	IB	Host Parallel Interface	69	LINEOUT_P	O	Line Interface
20	RS3	IB	Host Parallel Interface	70	AGND4	GND	IA Analog Ground
21	RS2	IB	Host Parallel Interface	71	SPKRP_P	O	Speaker Interface Output
22	RS1	IB	Host Parallel Interface	72	SPKRM_P	O	Speaker Interface Output
23	RS0	IB	Host Parallel Interface	73	AVDD_P	PWR	5V Digital power for IA
24	YCLK	I		74	NC	-	No Connection
25	IACLK	MI	Modem Interconnect	75	ICLK_P	MI	Modem Interconnect
26	IA1CLK	MI	Modem Interconnect	76	MCLK_S/NC	MI	Modem Interconnect
27	CTRLSIN_S/NC	MI	Modem Interconnect	77	VDD2	PWR	3.3V Digital Supply for DSP
28	RESERVED/NC	MI	Modem Interconnect	78	D7	IB/OC	Host Parallel Interface
29	SOUT_S/NC	MI	Modem Interconnect	79	D6	IB/OC	Host Parallel Interface
30	SIN_S/NC	MI	Modem Interconnect	80	D5	IB/OC	Host Parallel Interface
31	FSYNC_S/NC	MI	Modem Interconnect	81	D4	IB/OC	Host Parallel Interface
32	IARESET_S#/NC	MI	Modem Interconnect	82	D3	IB/OC	Host Parallel Interface
33	AGND1	GND	IA Analog Ground	83	D2	IB/OC	Host Parallel Interface
34	LINEIN_S/NC	I	Line Interface	84	DGND2	GND	DSP Digital Ground
35	MICP_S/NC	I	Microphone Input	85	VDD3	PWR	3.3V Digital Supply for DSP
36	MICM_S/NC	I	Microphone Input	86	D1	IB/OC	Host Parallel Interface
37	MICBIAS_S/NC	O	Microphone Bias Output	87	DGND3	GND	DSP Digital Ground
38	NC	-	No Connection	88	D0	IB/OC	Host Parallel Interface
39	NC	-	No Connection	89	CSBR#	IB	Host Parallel Interface
40	VREF_S/NC	MI	Modem Interconnect	90	WRITE#	IB	Host Parallel Interface
41	VC_S/NC	MI	Modem Interconnect	91	CS#	IB	Host Parallel Interface
42	VAA_S/NC	PWR	5V IA Analog power	92	READ#	IB	Host Parallel Interface
43	LINEOUT_S/NC	O	Line Interface	93	GPI2	IA	General purpose input
44	NC	-	No Connection	94	GPI3	IA	General purpose input
45	AGND2	GND	IA Analog Ground	95	GPI4	IA	General purpose input
46	SPKRP_S/NC	O	Speaker Interface Output	96	GPI5	IA	General purpose input
47	SPKRM_S/NC	O	Speaker Interface Output	97	GPI6	IA	General purpose input
48	AVDD_S/NC	PWR	5V IA Digital power	98	GPI7	IA	General purpose input
49	RESERVED/NC	MI	Modem Interconnect	99	GPO7	OC	General purpose output
50	ICLK_S/NC	MI	Modem Interconnect	100	VDD4	PWR	3.3V DSP Digital Power

Table 2-1. FM209/214 Modem Pin Signals - 128-Pin TQFP (Cont'd)

Pin	Signal Label	I/O Type	Interface	Pin	Signal Label	I/O Type	Interface
101	GPO6	OC	General purpose output	115	RESET#	IB	External reset
102	GPO5	OC	General purpose output	116	XTALI	I	Crystal in
103	RESERVED	MI	Modem Interconnect	117	XTALO	O	Crystal Out
104	GPO4	OC	General purpose output	118	RESERVED	MI	Modem Interconnect
105	GPO3	OC	General purpose output	119	XCLK	OB	X clock output
106	DGND4	GND	DSP Digital Ground	120	GPI1	IA	General purpose input
107	CTS#	OB	DTE Serial Interface	121	IRQ2#	OA	Interrupt request
108	IRQ1#	OB	Interrupt request	122	SR3IN	MI	Modem Interconnect
109	GPO2	OC	General purpose output	123	RESERVED	MI	Modem Interconnect
110	GPO1	OC	General purpose output	124	RESERVED	MI	Modem Interconnect
111	GPO0	OC	GPO0 (IAreset)	125	DGND6	GND	DSP Digital Ground
112	VDD5	PWR	3.3V DSP Digital Power	126	DVAA	PWR	3.3V DSP analog power
113	VGG	PWR	5V DSP Digital	127	AGND5	GND	DSP Analog Ground
114	DGND5	GND	DSP Digital Ground	128	RESERVED	MI	Modem Interconnect

Notes:

I/O types:

MI = Modem interconnect.

IA, IB, = digital input (see Table 2-3).

OA, OB, OC = digital output (see Table 2-3).

I = analog input (see Table 2-4).

O = analog output (see Table 2-4).

_P Signals: Primary IA

_S Signals: Secondary IA

Reserved = No external connection allowed.

Table 2-2. Modem Hardware Interface Signal Definitions

Label	I/O Type	Interface Signal Definition
OVERHEAD SIGNALS		
XTLI, XTLO	I/O	**Crystal In and Crystal Out.** The modem must be connected to an external crystal circuit consisting of a 32.256 MHz crystal.
RESET#	IB	**Reset.** After application of +5V power to the modem, RESET# must be held low for at least 15 ms after the +5V power reaches operating range. The modem is ready to use 25 ms after the low-to-high transition of RESET#. The reset sequence initializes the modem interface memory (Table 3-1) to default values.
VGG	PWR	**5V Supply Voltage for DSP Digital Circuits.**
AVDD_P, AVDD_S	PWR	**3.3V Supply Voltage for IA Digital Circuits.** Connect to VCC through decoupling circuit.
VAA_P, VAA_S	PWR	**5V Supply Voltage for IA Analog Circuits.** Connect to VCC through decoupling circuit.
VDDn	PWR	**3.3V Supply Voltage for DSP Digital Circuits.**
DVAA	PWR	**3.3V Supply Voltage for DSP Analog Circuits.**
DGNDn	GND	**Ground for Digital Circuits.** Connect to digital ground.
AGNDn	GND	**Ground for Analog Circuits.** Connect to analog ground.
MICROPROCESSOR BUS INTERFACE		
Address, data, control, and interrupt hardware interface signals allow modem connection to an 8085 or 6500 bus compatible microprocessor. With the addition of external logic, the interface can be made compatible with a wide variety of other microprocessors, such as the 8080 or 68000. The microprocessor interface allows a microprocessor to change modem configuration, read or write channel and diagnostic data, and supervise modem operation by writing control bits and reading status bits. **Note:** The modem should not be continuously selected for read operation. Also, read or write operations should be delayed by at least 2 XCLK cycles from a preceding write cycle.		
D0–D7	IB/OC	**Data Lines.** Eight bi-directional data lines (D0–D7) provide parallel transfer of data between the host and the modem. The most significant bit is D7. Data direction is controlled by the Read Enable (READ#-ø2) and Write Enable (WRITE#-R/W#) signals. During a read cycle, data from the DSP interface memory register is gated onto the data bus via three-state drivers in the DSP. These drivers force the data lines high for a one bit, or low for a zero bit. When not read, the three-state drivers assume their high-impedance (off) state. During a write cycle, data from the data bus is copied into the selected DSP interface memory register, with high and low bus levels representing one and zero bit states, respectively.
RS0–RS4	IB	**Register Select Lines.** Five active high Register Select inputs (RS0–RS4) address interface memory registers within the DSP when CS# is low. These lines are typically connected to address lines A0-A4. When selected by CS# low, the DSP decodes RS0 through RS4 to address one of 32 8-bit internal interface memory registers (00-1F). The most significant address bit is RS4 while the least significant address bit is RS0. The selected register can be read from, or written into, via the 8-bit parallel data bus (D0–D7).
CS#	IB	**Chip Select.** The active low CS# input selects and enables the modem DSP for parallel data transfer between the DSP and the host over the microprocessor bus.
CSBR#	IB	**Chip Select Buffer RAM.** Active low chip select used when CS# is active to select Interface Memory (CSBR# high) or Buffer RAM (CSBR# low).

Table 2-2. Modem Hardware Interface Signal Definitions (Cont'd)

<table>
<tr><th>Label</th><th>I/O Type</th><th>Interface Signal Definition</th></tr>
<tr><td>READ#</td><td>IB</td><td>Read Enable. When EN85# is low (8085 bus selected), reading is controlled by the host pulsing READ# input low during the microprocessor bus access cycle. The read timing is:

<table>
<tr><th>Parameter</th><th>Symbol</th><th>Min.</th><th>Max.</th><th>Units</th></tr>
<tr><td>CS# Setup Time</td><td>TCS</td><td>0</td><td>–</td><td>ns</td></tr>
<tr><td>RSi Setup Time</td><td>TRS</td><td>10</td><td>–</td><td>ns</td></tr>
<tr><td>Data Access Time</td><td>TDA</td><td>–</td><td>45</td><td>ns</td></tr>
<tr><td>Data Hold Time</td><td>TDHR</td><td>10</td><td>–</td><td>ns</td></tr>
<tr><td>Control Hold Time</td><td>THC</td><td>10</td><td>–</td><td>ns</td></tr>
</table>

Notes:
1. CS# and READ# must not both be continuously active.
2. A read or write operation following a read operation must be delayed by at least 2 XCLK cycle.</td></tr>
<tr><td>WRITE#–R/W#</td><td>IB</td><td>Write Enable–R/W#. When EN85# is low (8085 bus selected), writing is controlled by the host pulsing WRITE# input low during the microprocessor bus access cycle. The write timing is:

<table>
<tr><th>Parameter</th><th>Symbol</th><th>Min.</th><th>Max.</th><th>Units</th></tr>
<tr><td>CS# Setup Time</td><td>TCS</td><td>0</td><td>–</td><td>ns</td></tr>
<tr><td>RSi Setup Time</td><td>TRS</td><td>10</td><td>–</td><td>ns</td></tr>
<tr><td>Control Hold Time</td><td>THC</td><td>10</td><td>–</td><td>ns</td></tr>
<tr><td>Write Data Setup Time</td><td>TWDS</td><td>20</td><td>–</td><td>ns</td></tr>
<tr><td>Write Data Hold Time</td><td>TDHW</td><td>10</td><td>–</td><td>ns</td></tr>
</table>

Note:
1. A read or write operation following a write operation must be delayed by at least 4 XCLK cycles.</td></tr>
<tr><td>IRQ1#,
IRQ2#</td><td>OB,
OA</td><td>Interrupt Request. IRQ1# and IRQ2# interrupt request outputs may be connected to the host processor interrupt request input in order to interrupt host program execution for immediate modem service. (The term, "IRQ#," refers to both the IRQ1# and IRQ2# output lines in the following discussion.) The IRQ# output can be enabled in DSP interface memory to indicate immediate change of conditions in the modem. The use of IRQ# is optional depending upon modem application.

The IRQ# output structure is an open-drain field-effect-transistor (FET). The IRQ# output can be wire-ORed with other IRQ# lines in the application system. Any of these sources can drive the host interrupt input low, and the host interrupt servicing process normally continues until all interrupt requests have been serviced (all IRQ# lines have returned high). IRQ2# is active high and is driven at all times other that during Reset.

Because of the open-drain structure of IRQ#, an external pull-up resistor to +3.3V is required at some point on the IRQ# line. The resistor value should be small enough to pull the IRQ# line high when all IRQ# drivers are off (it must overcome the leakage currents). The resistor value should be large enough to limit the driver sink current to a level acceptable to each driver. If only the modem IRQ# output is used, a resistor value of 5.6K ohms, 20%, 0.25 W, is sufficient.</td></tr>
</table>

Table 2-2. Modem Hardware Interface Signal Definitions (Cont'd)

Label	I/O Type	Interface Signal Definition
V.24 SERIAL INTERFACE		
These pins provide timing, data, and control signals for implementing a ITU-T Recommendation V.24 compatible serial interface. These signals are TTL compatible in order to drive the short wire lengths and circuits normally found within stand-alone modem enclosures or equipment cabinets. For driving longer cables, these signals can be converted to EIA/TIA-232-E voltage levels.		
TXD	IA	**Transmit Data.** The modem obtains serial data to be transmitted from the local DTE on the Transmit Data (TXD) input in serial data mode (PDM bit = 0), or from the interface memory Transmit Data Register (DBUFF) in parallel data mode (PDM bit = 1).
RXD	OA	**Received Data.** The modem presents received serial data to the local DTE on the Received Data (RXD) output and to the interface memory Receive Data Register (DBUFF) in parallel data mode.
RTS#	IA	**Request to Send.** The active low RTS# input allows the modem to transmit data present at TXD in the serial data mode (PDM bit = 0), or in DBUFF in the parallel data mode (PDM bit = 1), when CTS# becomes active. The RTS# hardware control input is logically ORed with the RTSP bit (Table 3-1) by the modem to form the resultant control signal.
CTS#	OB	**Clear To Send.** CTS# active indicates to the local DTE that the training sequence has been completed and any data present at the TXD input in the serial data mode or in DBUFF in the parallel data mode will be transmitted. CTS# response times from RTS# on are shown in Table 1-4. The CTS# hardware status output parallels the operation of the CTSP bit (Table 3-1).
RLSD#	OB	**Received Line Signal Detector.** For V.17, V.33, V.29, and V.27 ter; RLSD# goes active at the end of the training sequence. If energy is above the turn-on threshold and training is not detected, the RLSD# off-to-on response time is 816 baud times for V.17/V.33, V.29, and V.27 ter long train; 492 baud times for V.17/V.33; and 486 baud times for V.27 ter short train. The RLSD# on-to-off time is 40 ± 5 ms for V.17/V.33, 35 ± 5 ms for V.29 or 11.6 ± 5 ms for V.27 ter. The RLSD# on-to-off time ensures that all valid data bits have appeared on RXD. The RLSD# programmable threshold levels default to –43 dBm for off-to-on and to –48 dBm for on-to-off. A minimum hysteresis of 2 dBm exists between the actual off-to-on and on-to-off transition levels. The threshold level and hysteresis are measured with an unmodulated 2100 Hz tone applied to the Receiver Analog (RXA) input. **Note:** Performance may be degraded when the received signal level is less than –43 dBm.
DCLK	OB	**Data Clock.** The modem outputs a synchronous Data Clock (DCLK) for USRT timing. The DCLK frequency is the data rate (±0.01%) with a duty cycle of 50 ±1%. The DCLK low-to-high transitions coincide with the center of the data bits. Transmit Data (TXD) must be stable during the one microsecond period immediately preceding the rising edge of DCLK and following the rising edge of DCLK.
AUXILIARY SIGNALS		
EN85#	IA	**Enable 85 Bus.** The EN85# input selects the modem microprocessor bus compatibility. When EN85# is low, the modem can interface directly to an 8085 compatible microprocessor bus using READ# and WRITE#. When EN85# is high, the modem can interface directly to a 6500 compatible microprocessor.
XCLK	OB	**XCLK Output.** XCLK is a 32.256 MHz clock.
YCLK	IA	**YCLK.** YCLK pin is reserved as a test input.

Table 2-2. Modem Hardware Interface Signal Definitions (Cont'd)

Label	I/O Type	Interface Signal Definition
		TELEPHONE/AUDIO INTERFACE
LINEOUT_P	O	**Primary IA Line Out.** The output characteristics are the same as a 1458 type op amp.
SPKRP_P, SPKRM_P	O	**Primary IA Speaker Plus and Speaker Minus.** The SPKRP_P and SPKRM_P outputs are a differential outputs 180 degrees out of phase with each other. The speaker driver can drive, full scale, loads as low as 120 ohms.
LINEIN_P	I	**Primary IA Line In.** LINEIN_P is a single-ended receive data input from the telephone line interface or an optional external hybrid circuit. The input impedance is > 150k ohms.
MICBIAS_P	O	**Primary IA MIC. Bias Output.**
MICP_P, MICM_P	I	**Primary IA MIC differential Inputs.** MICP_P and MICM_P are a differential microphone input from the microphone amplifier circuit. The input impedance is > 38k ohms.
LINEOUT_S	O	**Secondary IA Line Out.** The output characteristics are the same as a 1458 type op amp.
SPKRP_S, SPKRM_S	O	**Secondary IA Speaker Plus and Speaker Minus.** The SPKRP_S and SPKRM_S outputs are a differential outputs 180 degrees out of phase with each other. The speaker driver can drive, full scale, loads as low as 120 ohms.
LINEIN_S	I	**Secondary IA Line In.** LINEIN_S The input impedance is > 150k ohms.
MICBIAS_S	O	**Secondary IA MIC. Bias Output.**
MICP_S, MICM_S	I	**Secondary IA MIC differential Inputs.** MICP_S and MICM_S are a differential microphone input from the microphone amplifier circuit. The input impedance is > 38k ohms.
		GENERAL PURPOSE INPUT/OUTPUT LINES
GPI0-GPI7	IA	**General Purpose Inputs.** Eight general purpose input (GPI) pins are available to the host for programming via the modem interface memory.
RINGD (GPI7)	IA	**Ring Frequency Detected.** The RINGD signal from the DAA, when connected to the GPI7 input, is monitored for pulses in the range of 15 Hz to 68 Hz (with an 8000 Hz sample rate). The frequency detection range may be changed by the host in DSP RAM. The circuit driving RINGD should be a 4N35 optoisolator or equivalent. The circuit driving RINGD should not respond to momentary bursts of ringing less than 125 ms in duration, or less than 40 VRMS (15 Hz to 68 Hz) across TIP and RING. The RI status bit in the interface memory reflects the logic level on the GPI7 pin.
GPO0-GPO7	OC	**General Purpose Outputs.** Eight general purpose output (GPO) pins are available to the host for programming via the modem interface memory. GPO0 is used to reset the PIA and SIA. Connect the GPO0 output to IARESET_P# and IARESET_S#.
		EYE DIAGNOSTIC INTERFACE
Three signals provide the timing and data necessary to create an oscilloscope quadrature eye pattern. The eye pattern is simply a display of the received baseband constellation. By observing this constellation, common line disturbances can usually be identified.		
EYEXY	OA	**Serial Eye Pattern X/Y Output. Serial Eye Pattern X/Y Output.** EYEXY is a serial output containing two 16-bit diagnostic words (EYEX and EYEY) for display on an oscilloscope. EYEX data is the first 16 bits, MSB first, that are shifted out on the high portion of the EYESYNC clock. EYEX is a serial bit stream that is the equivalent of modem interface memory register XDAM1 followed by XDAL1. EYEY data is the second 16 bits, MSB first, that are shifted out on the low portion of the EYESYNC clock. EYEY is a serial bit stream that is the equivalent of modem interface memory register YDAM1 followed by YDAL1.
EYECLK	OA	**Serial Eye Pattern Clock.** EYECLK is a 345.6 kHz clock. Since the EYEXY data is shifted out on the rising edge of EYECLK, any eye pattern generator circuitry should sample EYEXY on the falling edge of EYECLK.
EYESYNC	OA	**Serial Eye Pattern Strobe.** EYESYNC is a strobe that indicates whether the EYEX or EYEY portion of EYEXY is shifted. The EYESYNC frequency is equal to the sample rate of the modem configuration.

Table 2-2. Modem Hardware Interface Signal Definitions (Cont'd)

Label	I/O Type	Interface Signal Definition
REFERENCE SIGNALS AND MODEM INTERCONNECT		
GPO0	OC	**GPO0.** Connect to IARESET_P# (57) & IARESET_S# (32)
IARESET#_P	MI	**IARESET_P#.** Connect to IARESET_S# (32) & GPO0 (111)
IARESET#_S	MI	**IARESET_S#.** Connect to IARESET_P# (57) & GPO0 (111)
ICLK_P	MI	**ICLK_P.** Connect to ICLK_S (50) & IA1CLK (26)
ICLK_S	MI	**ICLK_S.** Connect to ICLK_P (75) & IA1CLK (26)
IA1CLK	MI	**IA1CLK.** Connect to ICLK_P (75) & ICLK_S (50)
IACLK	MI	**IACLK.** Connect to MCLK_P (51) & MCLK_S (76)
MCLK_P	MI	**MCLK_P.** Connect to MCLK_S (76) & IACLK (25)
MCLK_S	MI	**MCLK_S.** Connect to MCLK_P (51) & IACLK (25)
SA1CLK	MI	**SA1CLK.** Connect to FSYNC_P(56) & FSYNC_S(31)
FSYNC_P	MI	**FSYNC_P.** Connect to FSYNC_S (31) & SA1CLK (18)
FSYNC_S	MI	**FSYNC_S.** Connect to FSYNC_P (56) & SA1CLK (18)
SIN_S	MI	**SIN_S.** Connect to SR3OUT (2)
SOUT_S	MI	**SOUT_S**. Connect to SR4IN (1)
CTRLSIN_P	MI	**CTRLSIN_P.** Connect to CTRLSIN_S(27) & SR1IO (6)
CTRLSIN_S	MI	**CTRLSIN_P.** Connect to CTRLSIN_P(52) & SR1IO (6)
SR1IO	MI	**SR1IO.** Connect to CTRLSIN_P(52) & CTRLSIN_S(27)
SOUT_P	MI	**SOUT_P.** Connect to SR3IN (122)
SR3IN	MI	**SR3IN.** Connect to SOUT_P(54)
SR3OUT	MI	**SR3OUT.** Connect to SIN_S (30)
SR4IN	MI	**SR4IN**. Connect to SOUT_S (29)
SIN_P	MI	**SIN_P.** Connect to SR4OUT (9)
SR4OUT	MI	**SR4OUT.** Connect to SIN_P (55)
VC_P	MI	**Low Voltage Reference.** Connect to analog ground through 10 µF (polarized, + terminal to VC) and 0.1 µF (ceramic) in parallel.
VREF_P	MI	**High Voltage Reference.** Connect to VC through 10 µF (polarized, + terminal to VREF) and 0.1 µF (ceramic) in parallel.
VC_S	MI	**Low Voltage Reference.** Connect to analog ground through 10 µF and 0.1 µF (ceramic) in parallel.
VREF_S	MI	**High Voltage Reference.** Connect to VC through 10 µF and 0.1 µF (ceramic) in parallel.

Notes:

1. I/O types:
   MI = Modem interconnect.
   IA, IB, = digital input (see Table 2-3).
   OA, OB, OC = digital output (see Table 2-3).
   I = analog input (see Table 2-4).
   O = analog output (see Table 2-4).
   PWR = Power
   GND = Ground

Table 2-3. Digital Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Input High Voltage	V_{IH}				VDC	
Type IA		2.0	–	5.25		
Type IB		0.7 V_{DD}	–	5.25		
Input High Current	I_{IH}				µA	V_{DD} = 3.6fV, V_{IN}= 3.6 V
Type IA		–	–	40		
Type IB		–	–	40		
Input Low Voltage	V_{IL}				VDC	
Type IA		0	–	0.8		
Type IB		0	–	0.8		
Input Low Current	I_{IL}				µA	V_{DD} = 3.6 V
Type IA and IB		–	–	–400		
Input Leakage Current	I_{IN}		–		µADC	
Types IA and IB				±2.5		
Output High Voltage	V_{OH}		–	–	VDC	
Type OA, OB		2.4	–	–		I_{LOAD} = 2 ma
Type OC		2.4	–	–		I_{LOAD} = 4 ma
Output Low Voltage	V_{OL}				VDC	
Type OA, OB		–	–	0.4		I_{LOAD} = -2 ma
Type OC		–	–	0.4		I_{LOAD} = 4 ma
Output Leakage Current	I_{LO}			±10	µADC	
Types OA and OB						
Capacitive Load	C_L				pF	
Types IA, IB			–	10		
Capacitive Drive	C_D				pF	
Types OA, OB, and OC			–	10		
Circuit Type						
Type IA						TTL
Type IB						Schmitt trigger input
Types OA and OB						TTL
Type OC						TTL with 3-state

Note:

1. Test Conditions: VDD =±5%, TA = 0 C to 70 C, (unless otherwise stated)
   Output Load Conditions: Data bus (D0-D7), address bus (RS0-RS4), chip selects, READ#, and WRITE# loads = 70 pF + one TTL load.
   Other = 50 pF + one TTL load.

Table 2-4. Analog Electrical Characteristics

Name	Type	Characteristic	Value
LINEIN_P, LINEIN_S	I	Input Impedance Maximum AC Input Voltage Reference Voltage*	> 150K Ω 3.2 VP-P +2.5 VDC
LINEOUT_P, LINEOUT_S	O	Minimum Load Maximum Capacitive Load Output Impedance Maximum AC Output Voltage Reference Voltage* DC Offset Voltage	350 Ω 0.12 µF 2.05 Ω 3.6 VP-P +2.5 VDC ± 200 mV
MICP_P and MICM_P, MICP_S and MICM_S	I	Input Impedance Maximum AC Input Voltage Reference Voltage*	> 38K Ω 3.2 VPd +2.5 VDC
MICBIAS_P MICBIAS_S	O	Out Voltage Output Current	2.2V Typical 1 ma typical 2 ma Max
SPKRP_P and SPKRM_P, SPKRP_S and SPKRM_S,	O	Minimum Load Maximum Capacitive Load Output Impedance Maximum AC Output Voltage Reference Voltage* DC Offset Voltage	120 Ω 0.1 µF < 4.1 Ω 3.6 VP-P +2.5 VDC ± 200 mV
* Reference voltage provided internal to the device.			

Table 2-5. Current and Power Requirements

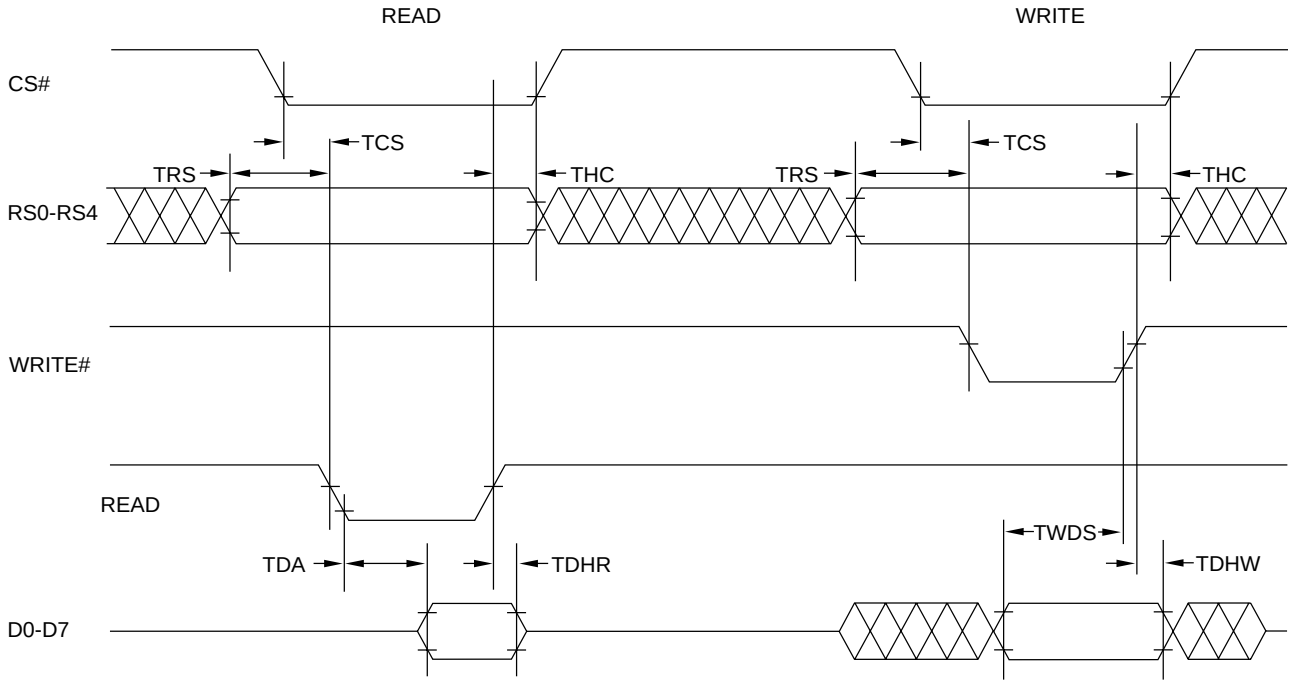
Mode	Current (ID) Typical @ 25° (ma)		Power (PD) Typical @ 25°C (mW)	Maximum @ 0°C (mW)	Maximum @ -40°C (mW)
FM209/214	@ 3.3V	52.5	200	250	270
Normal mode	@5V	5.75			
FM209/214-V	@ 3.3V	74.5	275	345	370
Normal mode	@5V	5.85			
FM209/214-VS	@ 3.3V	82.5	300	375	405
Normal mode	@5V	5.85			
FM209/214	@ 3.3V	2	7.6	9.5	10.3
Sleep Mode	@5V	0.2			

Notes:

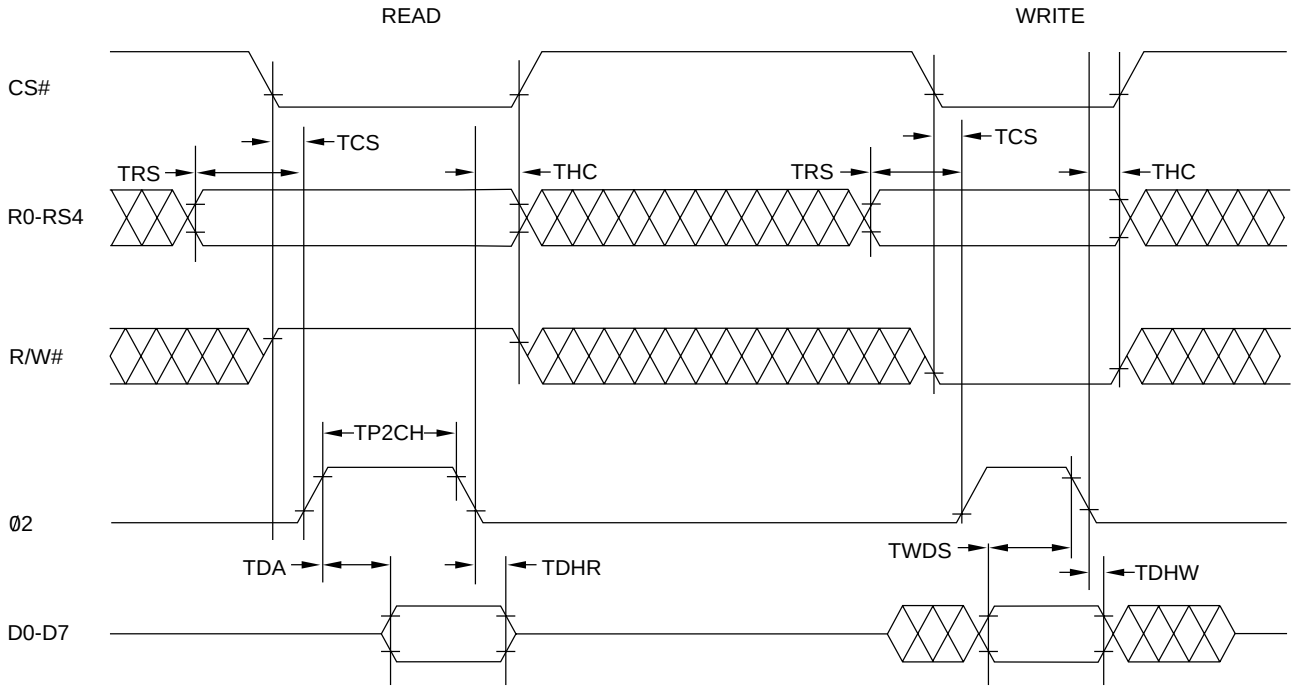
1. Maximum power @ -40°C specified only for extended temperature range parts.
2. Test conditions: VCC = 3.3 VDC for typical values; VCC = 3.6 VDC for maximum values.
3. Input Ripple less than 0.1 Vpeak-peak.
4. Data based on 32.256 MHz crystal frequency.

Table 2-6. Absolute Maximum Ratings

Parameter	Symbol	Limits	Units
Supply Voltage	V_{DD}	-0.5 to +3.6	V
Input Voltage	V_{IN}	-0.5 to (+5VD +0.5)	V
Analog Inputs	V_{IN}	-0.3 to (+5VA + 0.3)	V
Voltage Applied to Outputs in High Impedance (Off) State	V_{HZ}	-0.5 to (+5VD + 0.5)	V
DC Input Clamp Current	I_{IK}	±20	ma
DC Output Clamp Current	I_{OK}	±20	ma
Static Discharge Voltage (25°C)	V_{ESD}	±2500	V
Latch-up Current (25°C)	I_{TRIG}	±200	ma
Operating Temperature Range	T_A		°C
Commercial		0 to +70	
Extended		-40 to +85	
Storage Temperature Range	T_{STG}	-55 to +125	°C
ESD Bus Voltage	V_{GG}	-0.5 to (+5VD +0.5)	V



a. 8085 Bus Compatible (EN85# = L)



b. 6500 Bus Compatible (EN85# = H)

1175F2-5

Figure 2-5. Microprocessor Interface Waveforms

Table 2-7. Microprocessor Interface Timing

Parameter	Symbol	Min.	Max.	Units
CS# Setup Time	TCS	0	-	ns
RSi Setup Time	TRS	10	-	ns
Data Access Time	TDA	-	45	ns
Data Hold Time	TDHR	10	-	ns
Control Hold Time	THC	10	-	ns
Write Data Setup Time	TWDS	20	-	ns
Write Data Hold Time	TDHW	10	-	ns
Phase 2 (ø2) Clock High	TP2CH	70	-	ns

Notes:

1. CS# and READ# must not both be active continuously.
2. A read or write operation following a write operation must be delayed by at least 4 XCLK cycles.
3. A read or write operation following a read operation must be delayed by at least 2 XCLK cycle.

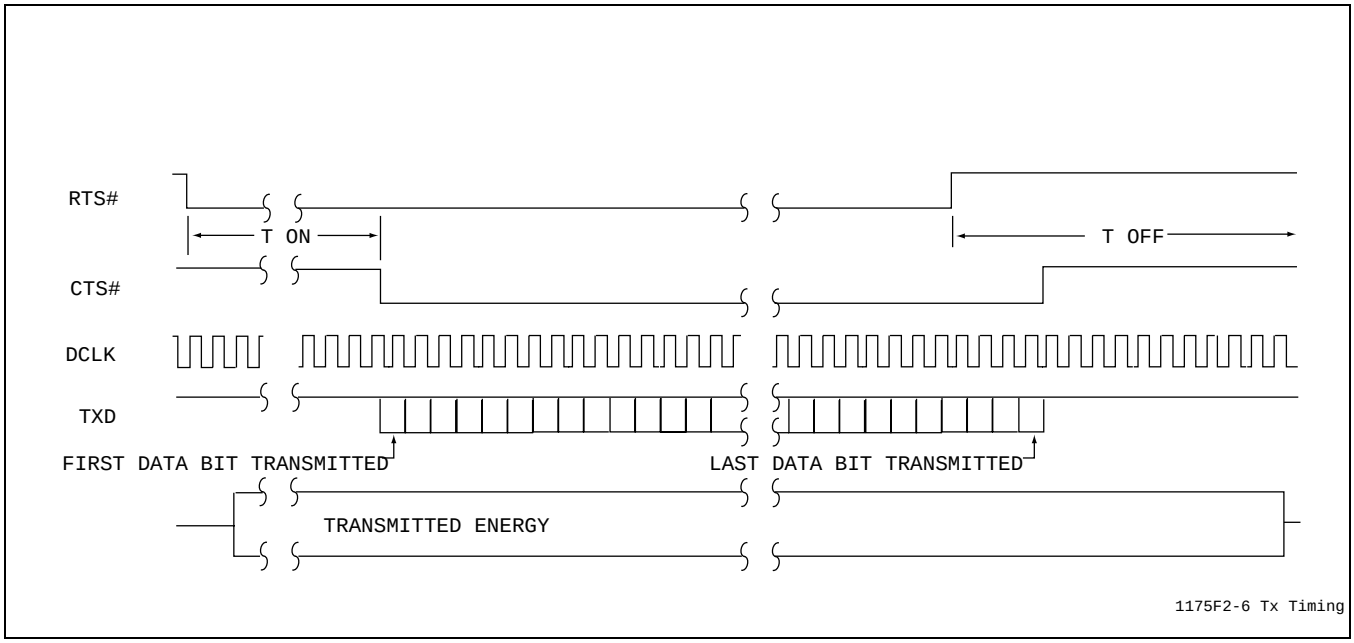


Figure 2-6. Transmitter Signal Timing

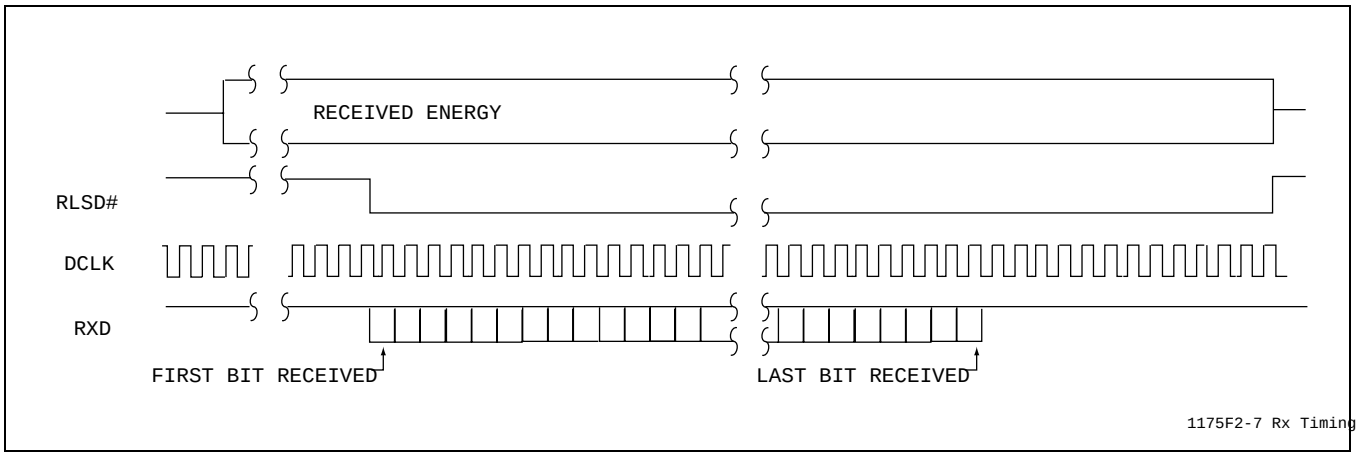


Figure 2-7. Receiver Signal Timing

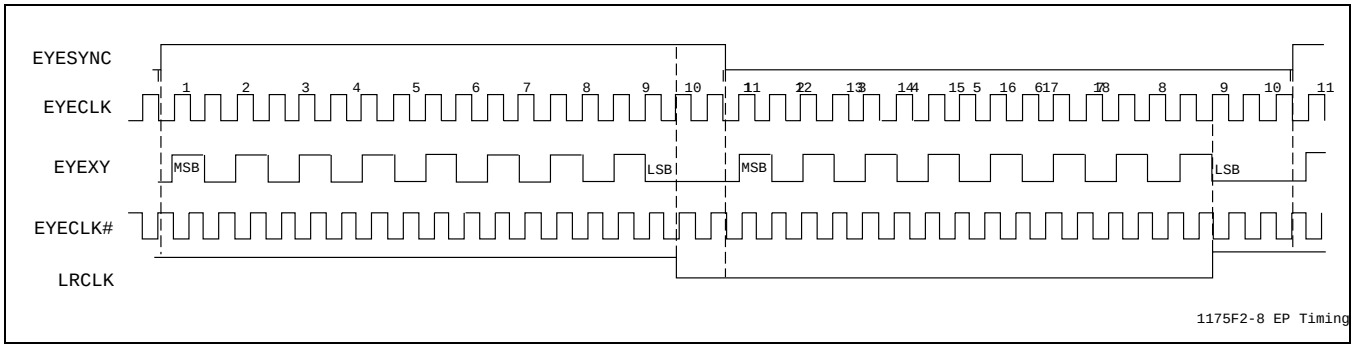


Figure 2-8. Eye Pattern Timing

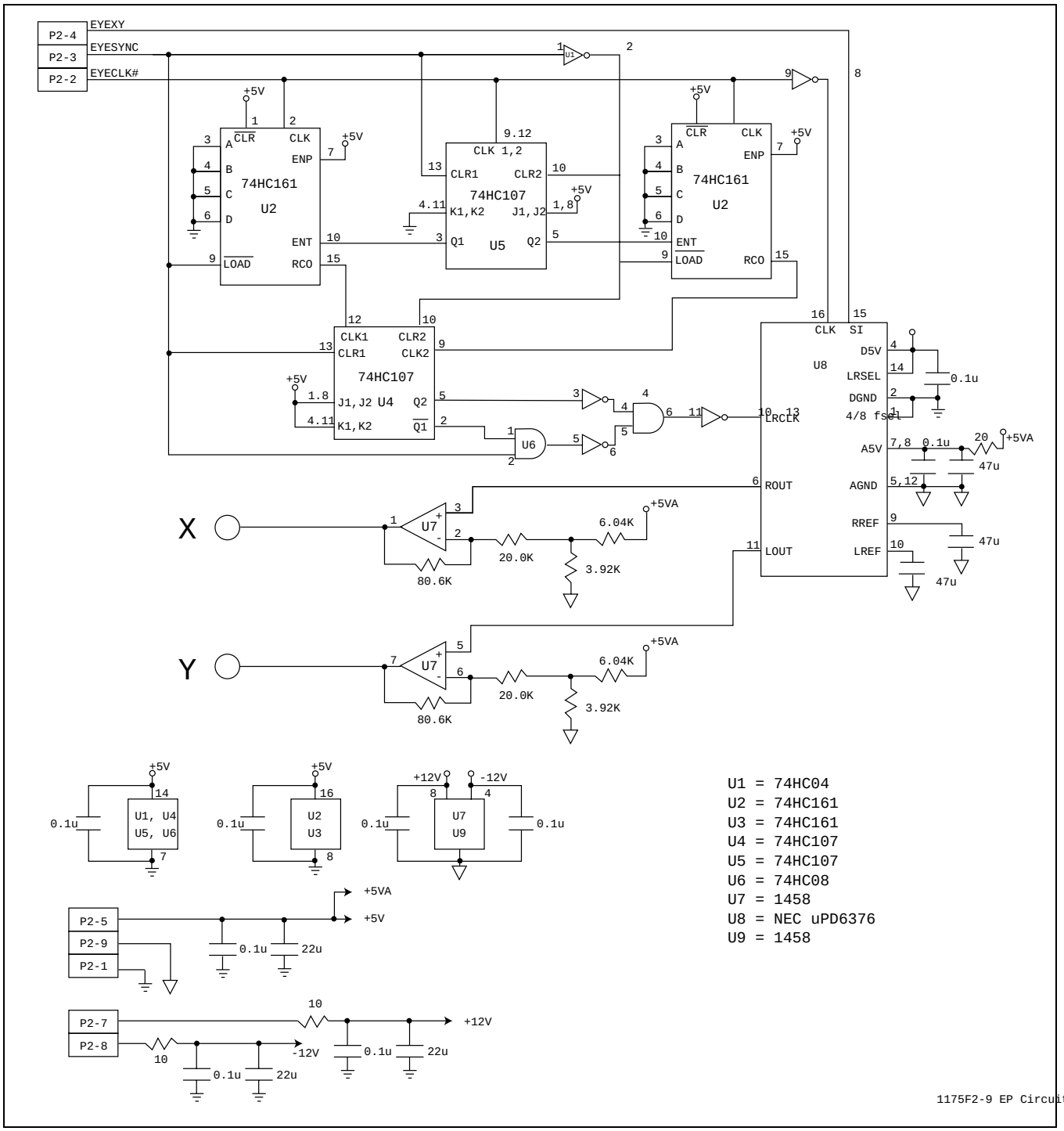


Figure 2-9. Eye Pattern Circuit

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3. SOFTWARE INTERFACE

Modem functions are implemented in firmware executing in the FM209/214 modem's digital signal processor.

3.1 INTERFACE MEMORY

The DSP communicates with the host processor by means of a dual-port, interface memory. The interface memory in the DSP contains thirty-two 8-bit registers, labeled register 00 through 1F (Figure 3-1). Each register can be read from, or written into, by both the host and the DSP.

The host can control modem operation by writing control bits to DSP interface memory and writing parameter values to DSP RAM through interface memory. The host monitors modem operation by reading status bits from DSP interface memory and reading parameter values from DSP RAM through interface memory.

Writing parameter values to DSP RAM and reading parameter values from DSP RAM is described in Section 4.

3.1.1 Interface Memory Map

A memory map of the 32 addressable registers in the modem is shown in Figure 3-1. These 8-bit registers may be read or written during any host read or write cycle. In order to operate on a single bit or a group of bits in a register, the host must read a register and then mask out unwanted data. When writing a single bit or group of bits in a register, the host must perform a read-modify-write operation. The entire register (8-bits) must first be read, the necessary bits must be set or reset without altering the other register bits, then the byte (8-bits) containing both the unaltered and modified bits must be written back into the interface memory.

3.1.2 Interface Memory Bit Definitions

The interface memory bits are defined in Table 3-1. The interface memory bits are referred to using the format Z:Q. The register number is designated by Z (00 through 1F), and the bit number by Q (0 through 7, 0 = least significant bit).

Register Function	Reg. Addr.	Bit 7	6	5	4	3	2	1	0	Default
Interrupt Handling	**1F**	PIA	—	—	PIE	PIREQ	—	—	SETUP	**-XX0-XX0**
	1E	B2IA	B1IA	B2I1E	B2I2E	B2A	B1I1E	B1I2E	B1A	**--00-00-**
High Speed Control & Status	**1D**	SHPR*	ASPEED*	PR*	PRDET*	—	—	—	—	**0000XXXX**
DTMF Status	**1C**	EDET	DTDET	OTS	DTMFD	DTMF				**--------**
General Purpose Outputs	**1B**	GPO7	GPO6	GPO5	GPO4	GPO3	GPO2	GPO1	GPO0	**00000001**
RAM Access/Voice Control	**1A**	SBRAM2	SBRAM1	DCDEN	CDEN	VOXREC	AGCDIS	CASDIS	RNGDIS	**00000000**
Speakerphone,	**19**	—	TONEPE	TONESE	VOXLO	VOXHI	AGCEN	RXBQ	TXBQ	**X00--000**
Voice/Audio Codec Control	**18**	HDSPK	SIAHND	TXSEN	TXH	RXH	INTRCM	LNLVL	LNLVL	**000--000**
V.23 Control	**18**	—	—	—	—	—	—	TDBE	—	**XXXXXX1X**
Voice/Audio Codec Status	**17**	EDETC	DTDETC	OTSC	DTMFDC	VOX	RI	FRx	VOVUN	**--------**
General Purpose Inputs	**16**	GPI7	GPI6	GPI5	GPI4	GPI3	GPI2	GPI1	GPI0	**--------**
RAM Access 2, V.23, and HDLC Control	**15**	ACC2	AREX2	AEOF	DR2	IO2/ CEQ	BR2/ ANS	WRT2	CR2/ V23HDX	**00000000**
V.23 Control	**14**	TXSQ	BRKS	PARSL		PEN	STB	WDSZ		**00000000**
Voice/Audio Codec Control	**14**	—	AGCSEL	DCVOX/ ENUPDT	0	FAST50	FAST33	SLOW	NORM	**-0000001**
RAM Access 2 Address/Data	**14**	RAM ADDRESS 2 (ADD2)								**00000000**
	13	X RAM DATA 2 MSB (XDAM2)/SINGLE BANK RAM ADDRESS 2 MSB (SBAD2M)								**--------**
	12	X RAM DATA 2 LSB (XDAL2)/SINGLE BANK RAM ADDRESS 2 LSB (SBAD2L)/TBUFFER								**--------**
	11	Y RAM DATA 2 MSB (YDAM2)								**--------**
	10	Y RAM DATA 2 LSB (YDAL2)/DATA BUFFER (DBUFF)								**--------**
Speakerphone,	**0F**	—	—	—	AGCPE	AGCSE	—	ECHOAT		**---11-00**
Voice/Audio Codec Control	**0E**	TTONEE	VOLUP	VOLDWN	SP/HS	MUTEP	MUTES	MICLVL		**-0010101**
High Speed Status	**0F**	FED		—	—	—	—	CTSP	CDET	**--XXXX--**
	0E	FSKFLS	—	—	—	—	—	—	—	**-XXXXXXX**
	0D	RX	PNDET	—	—	—	HPFEN	—	—	**--XXX0XX**
	0C	—	—	DATA	SCR1	PN	P2	P1	—	**XX-----X**
Programmable Interrupt	**0B**	ITBMSK								**00000000**
Control	**0A**	TRIG		ANDOR	ITADRS					**00000000**
High Speed Control, V.23, and HDLC Control & Status	**09**	OVRUN/ OE	EQSV	EQFZ	ZEROC	ABIDL	EOF BRKD	CRC/ FE	FLAG/ PE	**-000----**
Tone Detect, V.23, & High Speed Control & Status	**08**	FR3	FR2	FR1	12^{TH}	PNSUC/ CASD/UE	FSK7E	DCABLE	PDEQZ	**0000-000**
Mode Control**	**07**	RTSP	TDIS/ CODECS	PDM/ RMM	SHTR	EPT	SQEXT	SKIP	HDLC	**00001000**
	06	CONF								**00010100**
RAM Access 1 Control and Programmable Interrupt Control	**05**	ACC1	AREX1	PIDR	DR1	IO1	BR1	WRT1	CR1	**10000101**
RAM Access 1 Address/Data	**04**	RAM ADDRESS 1 (ADD1)								**00010111**
	03	X RAM DATA 1 MSB (XDAM1)/SINGLE BANK RAM ADDRESS 1 MSB (SBAD1M)								**--------**
	02	X RAM DATA 1 LSB (XDAL1)/SINGLE BANK RAM ADDRESS 1 LSB (SBAD1L)								**--------**
	01	Y RAM DATA 1 MSB (YDAM1)								**--------**
	00	Y RAM DATA 1 LSB (YDAL1)								**--------**

Notes:

* FM214 only.

* * A changed value in these registers (except RTSP and TDIS) require the setting of SETUP to become active.

— This symbol in the "Bit" columns indicates that the bit is reserved for modem use only (do not alter X value in "Default Value" column).

- This symbol in the "Default Value" column indicates that the value is determined by operating conditions.

Figure 3-1. Interface Memory Map

Table 3-1. Interface Memory Bit Definitions

Mnemonic	Location	Default	Name/Description
12^{TH}	08:4	0	**Select 12^{th} Order.** When control bit 12^{TH} is a 1, the tone detectors operate as one 12^{th} order filter (uses FR3).When 12^{TH} is a 0, the tone detectors operate as three parallel independent 4^{th} order filters (FR1, FR2, FR3).The 12^{th} bit is valid in all reception modes.
ABIDL	09:3	–	**Abort/Idle.** In HDLC mode, when the modem is configured as a transmitter and control/status bit ABIDL is a 1, the modem will finish sending the current DBUFF byte. The modem will then send continuous ones if ZEROC is a 0, or continuous zeros if ZEROC is a 1. When ABIDL is a 0, the modem will not send continuous ones or zeros. If ABIDL is reset one DCLK cycle after being set, the modem will transmit eight continuous ones if ZEROC is a 0, or eight continuous zeros if ZEROC is a 1. ABIDL is also set by the modem when the underrun condition occurs (bit OVRUN is a 1) and the modem will send at least eight continuous ones (if ZEROC is a 0) or eight continuous zeros (if ZEROC is a 1).To stop continuous ones or zeros transmission, ABIDL must be reset by the host. In HDLC mode, when the modem is configured as a receiver and status bit ABIDL is a 1, the modem has received a minimum of seven consecutive ones. To recognize further occurrences of this abort condition, ABIDL must be reset by the host.
ACC1	05:7	1	**RAM Access 1.** When control bit ACC1 is a 1, the modem accesses the RAM associated with the address in ADD1, and the AREX1 and CR1 bits. WRT1 determines if a read or write is performed.
ACC2	15:7	0	**RAM Access 2.** When control bit ACC2 is a 1, the modem accesses the RAM associated with the address in ADD2, and the AREX2 and CR2 bits. WRT2 determines if a read or write is performed.
ADD1	04:0-7	17	**RAM Address 1.** ADD1, in conjunction with AREX1, contains the RAM address used to access the modem's X and Y Data RAM (CR1 = 0) or X and Y Coefficient RAM (CR1 = 1) via the X RAM Data 1 least significant byte (LSB) and most significant byte (MSB) words (02:0-7 and 03:0-7, respectively) and the Y RAM Data 1 LSB and MSB words (00:0-7 and 01:0-7, respectively).
ADD2	14:0-7	00	**RAM Address 2.** ADD2, in conjunction with AREX2, contains the RAM address used to access the modem's X and Y Data RAM (CR2 = 0) or X and Y Coefficient RAM (CR2 = 1) via the X RAM Data 2 LSB and MSB words (12:0-7 and 13:0-7, respectively) and the Y RAM Data 2 LSB and MSB words (10:0-7 and 11:0-7, respectively).
AEOF	15:5	0	**Automatic End of Frame.** When the modem is configured as an HDLC transmitter and AEOF control bit is a 1, the modem interprets an underrun condition as an end of frame and outputs the FCS and at least one ending flag. (HDLC mode.)
AGCDIS	1A:2	0	**AGC Disable.** In Voice Codec Mode or Audio Codec Mode, the AGCDIS control bit disables (AGCDIS = 1) or enables (AGCDIS = 0) AGC in the voice/audio coder.
AGCEN	19:2	0	**Sample Rate AGC Enable.** When control bit AGCEN is a 1, the Sample Rate AGC is enabled to operate prior to Voice or ADPCM Audio coder. When AGCEN is a 0 the Sample Rate AGC is disabled.
AGCPE	0F:4	1	**AGC in PIA ADC Enable.** In speakerphone mode, the AGC associated with the PIA ADC sample is enabled when control bit AGCPE is a 1; the AGC gain is programmable when AGCPE is a 0.
AGCSE	0F:3	1	**AGC in SIA ADC Enable.** In speakerphone mode, the AGC associated with the SIA ADC sample is enabled when control bit AGCSE is a 1; the AGC gain is programmable when AGCSE is a 0.
AGCSEL	14:6	0	**AGC Select.** When control bit AGCSEL is a 0, the voice/audio coder Energy AGC is selected. When AGCSEL is a 1, the voice coder Classifier AGC is selected. (Voice Codec Mode and Audio Codec Mode)
ANDOR	0A:5	0	**AND/OR Bit Mask Function.** When control bit ANDOR is a 1 and the programmable interrupt is enabled (PIE bit = 1), the modem will assert IRQ1# if all the bits in the register specified by ITADRS and masked by ITBMSK trigger the interrupt and control bit PIREQ has been previously reset by the host. When ANDOR is a 0 and the programmable interrupt is enabled, the modem will assert IRQ1# if any one of the bits in the register specified by ITADRS and masked by ITBMSK trigger the interrupt and control bit PIREQ has been previously reset by the host.
ANS	15:2	0	**Answer.** When configuration bit ANS is set, the modem is in answer mode; when reset, the modem is in originate mode. If the modem is in Answer Mode (ANS= 1), then the transmit data rate is 1200 bps, and the receive data rate is 75 bps. If the modem is in Originate mode, the transmit data rate is normally 75 bps, and the receive data rate is 1200 bps. (V.23). When V.23 Half Duplex mode is selected (V23HDX = 1), ANS should be set to 0 to configure 1200 bps transmit and receive data rates. Since this is a configuration bit, the SETUP bit (1F:0) must be set after any change in the ANS bit.

Table 3-1. Interface Memory Bit Definitions (Cont'd)

Mnemonic	Location	Default	Name/Description
AREX1	05:6	0	**RAM Access 1 Code Extension Select.** When control bit AREX1 is a 1, the upper part (80h-FFh) of the RAM is selected. When AREX1 is a 0, the lower part (0-7Fh) is selected.
AREX2	15:6	0	**RAM Access 2 Code Extension Select.** When control bit AREX2 is a 1, the upper part (80h-FFh) of the RAM is selected. When AREX2 is a 0, the lower part (0-7Fh) is selected.
ASPEED	1D:6	0	**Auto Speed Change Enable.** When control bit ASPEED is a 0, the modem transmitter sends the default V.17 rate sequence. The modem receiver stores the rate sequence in RAM. (V.17 modes.) **ASPEED** / **Data Rate** / **Rate Sequence Pattern** 0 / V.17, all rates / 0111h 1 / 14400 bps / 0171h 1 / 12000 bps / 01B1h 1 / 9600 bps / 01F1h 1 / 7200 bps / 0331h When set to a 1, the modem transmitter sends a different rate sequence depending on the selected TCM configuration. When receiving in a TCM configuration, the modem reconfigures to the received rate sequence. The new configuration is reflected in the receiver CONF register.
B1A	1E:0	–	**Buffer 1 Available.** When set to a 1, status bit B1A signifies that the modem has either written diagnostic data to, or read diagnostic data from, the Y RAM DATA 1 LSB (YDAL1) register (00:0-7). This condition can also cause IRQ1# or IRQ2# to be asserted. The host writing to or reading from register 00 resets the B1A and B1IA bits to 0. (See B1I1E, B1I2E, and B1IA.)
B1I1E	1E:2	0	**Buffer 1 Interrupt 1 Enable.** When control bit B1I1E is a 1, IRQ1# is enabled for Buffer 1, the modem will assert IRQ1# and set B1IA to a 1 when B1A is set to 1 by the modem. When B1I1E is a 0, B1A has no effect on IRQ1# and B1IA. (See B1A and B1IA.)
B1I2E	1E:1	0	**Buffer 1 Interrupt 2 Enable.** When control bit B1I2E is a 1, IRQ2# is enabled for Buffer 1, the modem will assert IRQ2# when B1A is set to 1 by the modem. When B1I2E is a 0, B1A has no effect on IRQ2#. (See B1A.)
B1IA	1E:6	–	**Buffer 1 Interrupt Active.** When Buffer 1 interrupt is enabled (B1I1E is a 1) and B1A is set to a 1 by the modem, the modem asserts IRQ1# and sets status bit B1IA to a 1 to indicate that B1A caused the interrupt. The host writing to or reading from register 00 resets B1IA to a 0. (See B1I1E and B1A.)
B2A	1E:3	–	**Buffer 2 Available.** When set to a 1, status bit B2A signifies that, when the modem is in the parallel data mode (with or without HDLC selected), it has read register 10:0-7 (DBUFF) when transmitting (buffer becomes empty), or it has written register 10:0-7 (DBUFF) when receiving (buffer becomes full). When the modem is not in parallel data mode, the setting of B2A to a 1 by the modem signifies that the modem has either written diagnostic data to, or read diagnostic data from, the Y RAM DATA 2 LSB (YDAL2) register (10:0-7). In Voice Codec Mode or Audio Codec Mode, the modem sets B2A to indicate that the modem has loaded encoder output data into DBUFF (coder enabled, CDEN = 1 and DCDEN = 0) or that the modem has read decoder input data from DBUFF (decoder enabled, DCDEN = 1 and CDEN = 0). The modem setting B2A can also cause IRQ1# or IRQ2# to be asserted. The host writing to or reading from register 10h resets the B2A and B2IA bits to 0. (See B2I1E, B2I2E, and B2IA.)
B2I1E	1E:5	0	**Buffer 2 Interrupt 1 Enable.** When control bit B2I1E is a 1, IRQ1# is enabled for Buffer 2, the modem will assert IRQ1# and set B2IA to a 1 when B2A is set to a 1 by the modem. When B2I1E is a 0, B2A has no effect on IRQ1# and B2IA. (See B2A and B2IA.)

Table 3-1. Interface Memory Bit Definitions (Cont'd)

Mnemonic	Location	Default	Name/Description
B2I2E	1E:4	0	**Buffer 2 Interrupt 2 Enable.** When control bit B2I2E is a 1, IRQ2# is enabled for Buffer 2, the modem will assert IRQ2# when B2A is set to a 1 by the modem. When B2I2E is a 0, B2A has no effect on IRQ2#. (See B2A.)
B2IA	1E:7	–	**Buffer 2 Interrupt Active.** When Buffer 2 interrupt is enabled (B2I1E is a 1) and B2A is set to a 1 by the modem, the modem asserts IRQ1# and sets status bit B2IA to a 1 to indicate that B2A caused the interrupt. The host writing to or reading from register 10 resets B2IA to a 0. (See B2I1E and B2A.)
BR1	05:2	1	**Baud Rate 1.** In high-speed modem modes, when control bit BR1 is a 1, RAM access for ADD1 occurs at the baud rate regardless of the state of DR1. When BR1 is a 0, RAM access occurs at the sample rate or data rate (See DR1). The BR1 bit must be reset to 0 for tone, Voice Codec, Audio Codec, audio, or speakerphone modes.
BR2	15:2	0	**Baud Rate 2.** In high speed modem modes, when control bit BR2 is a 1, RAM access for ADD2 occurs at the baud rate regardless of the state of DR2. When BR2 is a 0, RAM access occurs at the sample rate or data rate (See DR2). The BR2 bit must be reset to a 0 for tone, audio, or speakerphone mode.
BRKD	09:2	–	**Break Detect (Parallel Mode).** When set, status bit BRKD indicates that the V.23 receiver has detected a Break sequence (continuous Space). (V.23)
BRKS	14:6	0	**Break Send (Parallel Mode).** When control bit BRKS is set in parallel mode, the modem will send continuous Space. When BRKS is reset, the modem will transmit parallel data from the TBUFFER. (V.23)
CASD	08:3	0	**CAS Detected.** In Speakerphone, Voice Codec, and Audio codec modes when status bit CASD is a 1, the Type II Caller ID CAS signal has been detected. When CASD is a 0 Type II Caller ID CAS signal has not been detected. The host must reset CASD after each detection.
CASDIS	1A:1	0	**CAS Disable.** When control bit CASDIS is a 1, Type II Caller ID CAS detection is disabled. When CASDIS is a 0 Type II Caller ID CAS detection is enabled. Type II Caller ID CAS detector is available in Speakerphone, Voice Codec, and ADPCM Audio Codec modes.
CDEN	1A:4	0	**Coder Enable.** In Voice Codec Mode or Audio Codec Mode, the modem performs voice/audio coding when control bit CDEN is a 1. The coder output is placed into DBUFF. Status bit B2A will be set by the modem when the coder output buffer becomes full (DBUFF). ACC2 must be reset. DCDEN must be a 0 when CDEN is a 1.
CDET	0F:0	–	**Carrier Detected.** When status bit CDET is a 1, the receiver has finished receiving the training sequence, or has turned on due to detecting energy above threshold, and is receiving data. When CDET is a 0, the receiver is in the idle state or is in the process of training.
CEQ	15:3	0	**Receive Compromise Equalizer Enable (1200 bps only).** When control bit CEQ is set, the receiver's digital compromise equalizer is inserted into the receive path (1200 bps receive only). The compromise equalizer taps are programmable through RAM. (V.23)
CODECS	07:6	0	**Codec Select.** In Voice Codec Mode and Audio Codec Modes the CODECS control bit selects data input source and output destination. When CODECS is a 1, the SIA ADC signal is recoded and the transmit signal is sent to both the PIA and SIA DACs. When CODECS is a 0, the PIA ADC signal is recoded and the transmit signal is sent to the PIA DAC. The setting of the CODECS bit must be followed by the setting of the SETUP bit to become active.

Table 3-1. Interface Memory Bit Definitions (Cont'd)

Mnemonic	Location	Default	Name/Description
CONF	06:0-7	14	**Configuration.** The CONF control bits select one of the following configurations: **CONF (Hex) — Configuration** 31 — V.17/V.33 14400 bps. (FM214.)* 32 — V.17/V.33 12000 bps. (FM214.)* 34 — V.17 9600 bps. (FM214.)* 38 — V.17 7200 bps. (FM214.)* 71 — 14400 bps with 1700 Hz carrier (non-standard TCM). (FM214.)* 72 — 12000 bps with 1700 Hz carrier (non-standard TCM). (FM214.)* 74 — 9600 bps with 1700 Hz carrier (non-standard TCM). (FM214.)* 78 — 7200 bps with 1700 Hz carrier (non-standard TCM). (FM214.)* 14 — V.29 9600 bps. * 12 — V.29 7200 bps. * 11 — V.29 4800 bps. * 0A — V.27 ter 4800 bps. * 09 — V.27 ter 2400 bps. * 20 — RTS on: V.21 Ch. 2 300 bps FSK transmit. * RTS off: V.21 Ch. 2 300 bps FSK receive and tone detect. * 21 — RTS on: V.21 Ch. 2 300 bps FSK transmit. * RTS off: V.21 Ch. 2 300 bps FSK receive, tone detect, and DTMF detect.* 24 — V.23, tone detect.* 22 — V.23 receive 1200 bps (Caller ID), tone detect. * 80 — RTS on: Dual/single tone transmit. * RTS off: Tone detect. * 82 — RTS on: 8-bit PCM Audio Codec transmit, DTMF detect, and tone detect. ** RTS off: 8-bit PCM Audio Codec receive , DTMF detect and tone detect.** 86 — RTS on: 16-bit PCM Audio Codec transmit, DTMF detect, and tone detect. ** RTS off: 16-bit PCM Audio Codec receive, DTMF detect and tone detect.** 90 — Voice Codec (-V option) Mode with Room Monitor** 91 — Speakerphone (-S option) with Voice Codec Mode (-V option). 92 — ADPCM Audio Codec (24 kbps, -V option) Mode with Room Monitor. ** 93 — Speakerphone (-S option) with ADPCM Audio Codec (24 kbps, -V option) Modes.** 94 — ADPCM Audio Codec (32 kbps, -V option) Mode with Room Monitor. ** 95 — Speakerphone (-S option) with ADPCM Audio Codec (32 kbps, -V option) Modes.** 98 — Voice Codec (4.7 kbps, -V option) Mode with Room Monitor. ** 99 — Speakerphone (-S option) with Voice Codec (4.7 kbps, -V option) Modes.** * Sample rate is 9600 Hz. ** Sample rate is 8000 Hz.

Table 3-1. Interface Memory Bit Definitions (Cont'd)

Mnemonic	Location	Default	Name/Description
			Configuration Definitions: (Cont'd) **V.17.** The modem operates as specified in ITU-T Recommendation V.17. **V.33.** The modem operates as specified in ITU-T Recommendation V.33. **V.29.** The modem operates as specified in ITU-T Recommendation V.29. **V.27 ter.** The modem operates as specified in ITU-T Recommendation V.27 ter. **V.23.** The modem operates as specified in ITU-T Recommendation V.23. **V.23 Receive.** The modem operates as specified in ITU-T Recommendation V.23. **V.21 Channel 2.** The modem operates as specified in ITU-T Recommendation V.21 Channel 2. **High Speed Modes.** The 2400 bps through 14400 bps modes. **DTMF Detect.** The modem detects DTMF transmissions. **Tone Transmit.** The modem transmits single or dual frequency tones in response to the RTS input pin or RTSP bit. Tone frequencies and amplitudes are programmable in the DSP RAM. **Tone Detect.** When the Tone Detect configuration is selected and 12^{TH} is a 1, the three 4^{th} order tone detect filters are combined into a single 12^{th} order tone detect filter (FR3). If 12^{TH} is not set to a 1, the three tone detect filters are placed in parallel and are independent (FR1, FR2, and FR3). All tone detect filters are programmable. **Voice Codec Mode.** Voice coder and decoder with optional error correction coding (CDEN, DCDEN, HDLC). DTMF detect, Type II Caller ID CAS detection and three tone detectors with a local echo canceller during decoder operation. Dual/single tone transmission when decoder disabled (RTSP). Continuously selectable pitch synchronized decoder playback speeds of 50% faster, 33% faster, or 50% slower than normal speed (FAST50, FAST33, SLOW, NORM). Selectable SIA and PIA recording source and playback destination (CODECS). **ADPCM Audio Codec Mode.** 24 kbps or 32 kbps audio coder and decoder (CDEN, DCDEN). DTMF detect, Type II Caller ID CAS detection and three tone detectors are available. Dual/single tone transmission is available when the decoder is disabled (RTSP). During the decoder operation, a local echo canceller is used to improve DTMF and tone detector operation. Selectable SIA and PIA recording source and playback destination (CODECS). **PCM Audio Codec Mode.** 16-bit or 8-bit PCM audio coder and decoder. DTMF detect, Type II Caller ID CAS detection and three tone detectors are available. A local echo canceller is used to improve DTMF and tone detector operation. Selectable SIA and PIA recording source and playback destination (CODECS). **Room Monitor**. Room monitor routes the PIA ADC input signal to the PIA DAC output, or routes the SIA ADC input signal to the PIA DAC output (RMM). **Speakerphone Mode.** Full-duplex telephone voice communication, full-duplex intercom (INTRCM) voice communication and high gain half-duplex (HDSPK) telephone/intercom voice communications operations are supported. Full-duplex auto fallback to pseudo-duplex under poor operating conditions. Conversation recording, stored message playback, PIA and SIA single/dual tone transmission, DTMF detect, Type II Caller ID CAS detection and tone detect are provided. Speakerphone options include microphone and speaker AGCs, muting, and volume control. A speakerphone/handset switch supports private communication (SP/HS).

Table 3-1. Interface Memory Bit Definitions (Cont'd)

Mnemonic	Location	Default	Name/Description
CR1	05:0	1	**Coefficient RAM 1 Select.** When control bit CR1 is a 1, AREX1 and ADD1 address Coefficient RAM. When CR1 is a 0, AREX1 and ADD1 address Data RAM. This bit must be set according to the desired RAM address (Table 4-1).
CR2	15:0	0	**Coefficient RAM 2 Select.** When control bit CR2 is a 1, AREX2 and ADD2 address Coefficient RAM. When CR2 is a 0, AREX2 and ADD2 address Data RAM. This bit must be set according to the desired RAM address (Table 4-1).
CRC	09:1	–	**Cyclic Redundancy Check Error.** In HDLC mode, when status bit CRC is a 1 and status bit EOF is a 1, the received frame is in error. When CRC is a 0 and EOF is a 1, the received frame is correct. CRC changes immediately before EOF is set to a 1. In Caller ID mode (CONF = 22h), the modem sets the CRC bit if the stop bit is detected to be a 1.
CTSP	0F:1	–	**Clear To Send Parallel.** When set to a 1, status bit CTSP indicates to the DTE that the training sequence has been completed and any data present at TXD (PDM = 0) or DBUFF (PDM = 1) will be transmitted. CTSP parallels the operation of the CTS# pin.
DATA	0C:5	–	**Data Mode.** When status bit DATA is a 1, the high speed transmitter/receiver is in the data mode.
DBUFF	10:0-7	–	**Data Buffer.** In the parallel data mode (PDM bit = 1), the host obtains received data from the modem by reading a data byte from DBUFF; the host sends data to the modem to be transmitted by writing a data byte to DBUFF. The data is received and transmitted bit 0 first. The modem reading (taking data) or writing (sending data) to this register sets the B2A bit. The host reading (taking data) or writing (sending data) to this register resets the B2A bit. By setting B2IxE (x=1 or 2), the host can enable the assertion of IRQ#x upon the setting of B2A. Bit 0 of DBUFF is the first bit of the 8-bit input or output. In the V.23 configuration (CONF = $24), in parallel data mode (PDM bit = 1), the host obtains received data from the modem by reading a data byte from DBUFF. The modem writing (sending data) to this register sets the B2A bit (1E:3). The host reading (taking data) from this register resets the B2A bit (1E:3). In voice/audio codec modes, DBUFF is the 8-bit voice/audio decoder input buffer (DCDEN = 1 and CDEN = 0) or voice/audio coder output buffer (CDEN = 1 and DCDEN = 0).
DCABLE	08:1	0	**Digital Cable Equalizer Enable.** Control bit DCABLE enables (1) or disables (0) insertion of the digital cable equalizer into the receive and transmit paths.
DCDEN	1A:5	0	**Decoder Enable.** When control bit DCDEN is a 1 and bit CDEN is a 0, the modem performs voice/audio decoding on the DBUFF input. Status bit B2A is set by the modem when the decoder's input buffer is empty. CDEN must be reset when DCDEN is a 1. ACC2 must be reset. (Voice/audio codec modes.)
DCVOX	14:5	0	**Decouple VOX.** When the voice coder Energy AGC is enabled (AGCSEL = 0) and control bit DCVOX is a 0 , the AGC gain is applied to the input signal when the AGC is enabled (AGCDIS = 0) and the VOX bit is a 1. When AGCSEL = 0 and DCVOX is a 1, the AGC gain is applied signal when the AGC is enabled (AGCDIS = 0) regardless of the VOX bit state. (Voice/audio codec modes.)
DR1	05:4	0	**Data Rate 1.** In high speed, FSK/DTMF, or FSK modes, when control bit DR1 is a 1, RAM access associated with ADD1 occurs at the modem data rate if BR1 = 0. When DR1 is a 0, RAM access occurs at the modem sample rate (9600 Hz) or baud rate depending on the state of BR1.
DR2	15:4	0	**Data Rate 2.** In high speed, FSK/DTMF, or FSK modes, when control bit DR2 is a 1, RAM access associated with ADD2 occurs at the modem data rate if BR2 = 0. When DR2 is a 0, RAM access occurs at the modem sample rate (9600 Hz) or baud rate depending on the state of BR2.

Table 3-1. Interface Memory Bit Definitions (Cont'd)

Mnemonic	Location	Default	Name/Description
DTDET	1C:6	–	**Dual Tone Detected.** When configured as an DTMF receiver, the modem sets status bit DTDET to a 1 when a signal is received that satisfies all DTMF criteria except on-time, off-time, and cycle-time. The encoded DTMF Output Word (1C:0-3) value is available when DTDET is a 1. If the received signal is a valid DTMF signal, then DTDET will be set to a 1 approximately 11 ms following EDET setting to a 1. The DTDET bit is reset by the modem after DTMFD is set to a 1 or if the received signal fails to satisfy any subsequent DTMF criteria.
DTDETC	17:6	–	**Dual Tone Detected Copy.** In DTMF modes, DTDETC is a copy of the DTDET bit for programmable interrupt control.
DTMF	1C:0-3	–	**DTMF Output Word.** When configured as an DTMF receiver and a DTMF signal is present such that status bit DTDET is set by the modem, the encoded DTMF output is written to 1C:0-3. The DTMF symbol codes are: **DTMF Symbol / Encoded Output (Hex) / DTMF Symbol / Encoded Output (Hex)** 1 0 3 8 4 1 6 9 7 2 9 A * 3 # B 2 4 A C 5 5 B D 8 6 C E 0 7 D F
DTMFD	1C:4	–	**DTMF Signal Detected.** When configured as an DTMF receiver, the modem sets status bit DTMFD to a 1 when a DTMF signal has been detected that satisfies all specified DTMF detect criteria. The host must reset this bit after reading the DTMF Output Word (1C:0-7), otherwise the same symbol may be missed by the host.
DTMFDC	17:4	–	**DTMF Detected Copy.** In DTMF modes, DTMFDC is a copy of the DTMFD bit for programmable interrupt control.
ECHOAT	0F:0-1	00	**Handset Echo Attenuation.** In speakerphone mode, ECHOAT bits control the level of the simulated echo for handset operation when the SP/HS bit is a 0. The signal entering the SIA ADC is attenuated and retransmitted to the SIA DAC as follows: **Bit 1 / Bit 0 / Attenuation** 0 0 ∞ dB 0 1 18 dB 1 0 12 dB 1 1 6 dB
EDET	1C:7	–	**DTMF Early Detection.** When configured as an DTMF receiver, the modem sets status bit EDET to a 1 approximately 20 ms after the DTMF signal energy is detected to indicate that the received signal is probably a DTMF signal. This bit is reset by the modem after DTMFD is set to a 1 or if the received signal fails to satisfy any subsequent DTMF criteria.
EDETC	17:7	–	**Early Detection Copy.** In DTMF modes, EDETC is a copy of the EDET bit for programmable interrupt control.
ENUPDT	14:5	0	**Energy Update.** When the Classifier AGC is enabled (AGCSEL = 1) and control bit ENUPDT is a 1 , the AGC gain will be adjusted whenever the input signal energy exceeds the AGC Gain Adaptation Threshold parameter value. (Voice/Audio Codec Mode.)

Table 3-1. Interface Memory Bit Definitions (Cont'd)

Mnemonic	Location	Default	Name/Description
EOF	09:2	–	**End of Frame.** In HDLC mode, when the modem is configured as a transmitter and bit AEOF is a 0, the EOF bit is a control bit. When AEOF is a 0, to convey to the modem that it is time to send the 16-bit FCS and ending flag of an HDLC frame, the host must set the EOF bit after the modem has taken the last byte of data (resides in DBUFF) of the frame (B2A sets again). EOF will then be reset by the modem after it has recognized the setting of EOF by the host. When the modem is configured as a transmitter and bit AEOF is a 1, EOF is a status bit. In this case, the modem will interpret the underrun condition as the end of the frame, set EOF, and will output the 16-bit FCS and at least one ending flag. EOF is reset whenever a flag is transmitted. When the modem is configured as a receiver and bit AEOF is a 1, the modem has received a frame ending flag and the CRC bit is updated. EOF must be reset by the host before receiving the ending flag of a following frame.
EPT	07:3	1	**Echo Protector Tone Enable.** When control bit EPT is a 1, an unmodulated carrier is transmitted for 187.5 ms followed by 20 ms of no transmitted energy prior to the transmission of the training sequence. When EPT is a 0, neither the echo protector tone nor the 20 ms of no energy are transmitted prior to the transmission of the training sequence except in V.29 long train which transmits 20 ms of silence at the beginning of training. (See status bit P1.) The setting of the EPT bit must be followed by the setting of the SETUP bit to become active.
EQFZ	09:5	0	**Equalizer Freeze.** When control bit EQFZ is a 1, updating of the receiver's adaptive equalizer taps is inhibited.
EQSV	09:6	0	**Equalizer Save.** When control bit EQSV is a 1, the adaptive equalizer taps are not zeroed when reconfiguring the modem or when entering the training state. Adaptive equalizer taps are also not updated during training. For short train only, this bit is used in conjunction with the SHTR bit.
FAST33	14:2	0	**Faster by 33% Playback Speed.** When control bit FAST33 is a 1 and the FAST50, SLOW, and NORM control bits are reset, playback time is 67% of normal playback time. FAST33 must be reset when another speed is selected. (Voice Codec Mode)
FAST50	14:3	0	**Faster by 50% Playback Speed.** When control bit FAST50 is a 1 and the FAST33, SLOW, and NORM control bits are reset, playback time is 50% of normal playback time. FAST50 must be reset when another speed is selected. (Voice Codec Mode)
FE	09:1	0	**Framing Error (Parallel Mode).** When set, status bit FE indicates that more than 1 in 8 characters were received without a Stop bit in asynchronous mode. When reset, no framing error is detected. (V.23)
FED	0F:7,6	–	**Fast Energy Detector.** Status bits FED indicates the level of the received signal according to the following codes: **Bit 7** **Bit 6** **Energy Level** 0 0 No energy (idle mode) 0 1 Invalid 1 0 Above Turn-off Threshold 1 1 Above Turn-on Threshold
FLAG	09:0	–	**FLAG Mode**. When the modem is configured as a transmitter and status bit FLAG is a 1, the modem is transmitting a flag sequence. When the modem is configured as a receiver and status bit FLAG is a 1, the modem has received a flag sequence. (HDLC mode.)

Table 3-1. Interface Memory Bit Definitions (Cont'd)

Mnemonic	Location	Default	Name/Description
FR1	08:5	–	**Frequency No. 1.** The modem sets status bit FR1 to a 1 when energy above tone detector 1's turn-on threshold is detected. The default detection range = 2100 Hz ± 25 Hz for 9600 Hz sample rate. The FR1 tone detector sample rate is 8000 Hz in Voice Codec Mode, Audio Codec Mode, and Speakerphone Mode. The FR1 detector must be reprogrammed for 8000 Hz.
FR2	08:6	–	**Frequency No. 2.** The modem sets status bit FR2 to a 1 when energy above tone detector 2's turn-on threshold is detected. The default detection range = 1100 Hz ± 30 Hz for 9600 Hz sample rate. The FR2 tone detector sample rate is 8000 Hz in Voice Codec Mode, Audio Codec Mode, and Speakerphone Mode. The FR2 detector must be reprogrammed for 8000 Hz.
FR3	08:7	–	**Frequency No. 3.** The modem sets status bit FR3 to a 1 when energy above tone detector 3's turn-on threshold is detected. The default detection range = 462 Hz ± 14 Hz for 9600 Hz sample rate. The FR3 tone detector sample rate is 8000 Hz in Voice Codec Mode, Audio Codec Mode, and Speakerphone Mode. The FR3 detector must be reprogrammed for 8000 Hz.
FRx	17:1	–	**Frequency No. 1, 2, or 3.** Status bit FRx is set by the modem if FR1, FR2, FR3 or CASD is set. FRx is reset by the modem if FR1, FR2, FR3 and CASD are reset.
FSK7E	08:2	–	**FSK FLAG (7E) Detected.** The modem sets status bit FSK7E to a 1 when FSK flags have been detected in a high speed receiver mode. FSK7E is valid after bit FSKFLS transitions from 1 to 0. FSK7E is not valid in V.27 ter short train modes.
FSKFLS	0E:7	0	**FSK FLAG (7E) Search.** When status bit FSKFLS is a 1, the modem is searching for FSK flags in high speed receiver modes except V.27 ter short train. This bit is reset by the modem when the FSK flag search is completed.
GPIx	16:0-7	–	**General Purpose Inputs.** The modem sets/resets bits 0 -7 in the GPIx register to represent the corresponding logic level (1 = high, 0 = low) appearing on signals GPI0 - GPI7, respectively, within 125 µs of signal transition. GPI7 is typically connected to the DAA ring detection circuitry, and bit RI in the interface memory represents a valid ring frequency if it is so connected.
GPOx	1B:0-7	00000001	**General Purpose Outputs.** Bits 0-7 in the GPOx register, set/reset by the host, are reflected by logic level outputs (1 = high, 0 = low) appearing on signals GPO0 - GPO7, respectively, within 125 µs of bit transition. Connect GPO0 to IARESETp and IARESETs.
HDLC	07:0	0	**HDLC Mode.** When control bit HDLC is a 1 and the PDM bit is a 1, the modem performs HDLC framing in parallel data mode. When the HDLC bit is a 0 or the PDM bit is a 0, the modem does not perform HDLC framing. In data modes, changing the value of the HDLC bit requires setting the SETUP bit to become active. In the Voice Codec mode, error correction is enabled (HDLC = 1) or disabled (HDLC = 0). Setting the SETUP bit is not required.
HDSPK	18:7	0	**Half-Duplex Speakerphone.** In Speakerphone mode, when control bit HDSPK is a 1, half-duplex speakerphone is enabled. When HDSPK is a 0, full-duplex speakerphone is enabled.
HPFEN	0D:2	0	**High Pass Filter Enable.** When control bit HPFEN is a 1, the Pre-AGC high pass filter is enabled in the receive path.
INTRCM	18:2	0	**Intercom.** In Speakerphone mode, when control bit INTRCM is a 1, full-duplex/half-duplex intercom is supported.
IO1	05:3	0	**Input/Output RAM 1 Select**. When control bit IO1 is a 1, ADD1 addresses IO RAM. When IO1 is a 0, ADD1 addresses either coefficient or data RAM depending on the state of the CR1 bit. This bit must be set according to the desired RAM address. (See Table 4-1).
IO2	15:3	0	**Input/Output RAM 2 Select.** When control bit IO2 is a 1, ADD2 addresses IO RAM. When IO2 is a 0, ADD2 addresses either coefficient or data RAM depending on the state of the CR2 bit. This bit must be set according to the desired RAM address. (See Table 4-1).

Table 3-1. Interface Memory Bit Definitions (Cont'd)

Mnemonic	Location	Default	Name/Description
ITADRS	0A:0-4	0	**Interrupt Address.** These 5 bits specify the register upon which the programmable interrupt and ITBMSK will take effect. The address of the byte on which the modem asserts IRQ1# on a bit or bits in that byte is: **Host Register (Hex) / ITADRS (Hex) / Host Register (Hex) / ITADRS (Hex)** 00 00 10 08 01 10 11 18 02 01 12 09 03 11 13 19 04 02 14 0A 05 12 15 1A 06 03 16 0B 07 13 17 1B 08 04 18 0C 09 14 19 1C 0A 05 1A 0D 0B 15 1B 1D 0C 06 1C 0E 0D 16 1D 1E 0E 07 1E 0F 0F 17 1F 1F
ITBMSK	0B:0-7	00	**Interrupt Bit Mask.** This byte performs a bit mask on the register specified in ITADRS for the programmable interrupt processing. A one in any position in ITBMSK will cause the modem to assert IRQ1# on the corresponding bit or bits in the register specified by ITADRS according to the ANDOR bit and the TRIG bits if PIE is set by the host and PIREQ is reset by the host.
LNLVL	18:0-1	00	**Line Volume Level.** In speakerphone mode, the LNLVL bits control the PIA ADC signal gain as follows: **Bit 1 / Bit 0 / Gain** 0 0 0 dB 0 1 6 dB 1 0 9.5 dB 1 1 12 dB
MICLVL	0E:0-1	01	**Microphone Volume Level.** In speakerphone mode, the MICLVL bits control the SIA ADC signal gain as follows: **Bit 1 / Bit 0 / Gain** 0 0 0 dB 0 1 6 dB 1 0 9.5 dB 1 1 12 dB
MUTEP	0E:3	0	**Mute PIA ADC.** In speakerphone mode, control bit MUTEP enables (MUTEP = 1) or disables (MUTEP = 0) muting of the PIA ADC signal.
MUTES	0E:2	1	**Mute SIA ADC.** In speakerphone mode, control bit MUTES enables (MUTES = 1) or disables (MUTES = 0) muting of the SIA ADC signal.
NORM	14:0	1	**Normal Playback Speed.** When control bit NORM is a 1 and the FAST50, FAST33, and SLOW control bits are reset, normal playback speed is selected. NORM must be reset when another speed is selected. (Voice Codec Mode)
OE	09:7	–	**Overrun Error (Parallel Mode).** When set, status bit OE indicates that the receive Data Buffer (DBUFF) was loaded with the new byte of received data before the host read the old data from DBUFF. When reset, DBUFF was read before new receive data was loaded into DBUFF. (V.23)

Table 3-1. Interface Memory Bit Definitions (Cont'd)

Mnemonic	Location	Default	Name/Description
OTS	1C:5	–	**On-Time Satisfied.** When configured as an DTMF receiver, the modem sets status bit OTS to 1 after the DTMF on-time criteria is satisfied. This bit is reset by the modem after DTMFD is set to a 1 or if the received signal fails to satisfy the DTMF off-time criteria.
OTSC	17:5	–	**On-Time Satisfied Copy.** In DTMF modes, OTSC is a copy of the OTS bit for programmable interrupt control.
OVRUN	09:7	–	**Overrun/Underrun.** In HDLC mode, when configured as a transmitter and control bit AEOF is a 0, the modem sets status bit OVRUN to a 1 if a transmit underrun condition occurs. If the host does not load in a new byte of data in DBUFF within eight bit times of loading the previous byte into DBUFF, OVRUN and ABIDL bits will be set. The modem will then automatically send eight continuous ones. The transmission of these ones will continue until the host resets ABIDL. The modem will then finish sending the current group of eight ones and will either start sending another frame (if B2A is a 0) or will transmit continuous flags. The modem will reset OVRUN every time it sets B2A. If AEOF is a 1, OVRUN is disabled. When configured as a receiver, the modem sets the OVRUN bit to a 1 if a receive overrun condition occurs. To detect the next overrun condition, the host must reset this bit.
P1	0C:1	–	**P1 Sequence.** When the modem is configured as a high speed transmitter, status bit P1 = 1 indicates the P1 sequence is being sent. When P1 = 0, the P1 sequence is not being sent. The P1 sequence is an echo protection tone. When the modem is configured as a receiver, the P1 bit has no meaning.
P2	0C:2	–	**P2 Sequence.** When the modem is configured as a high speed transmitter, status bit P2 = 1 indicates the P2 sequence is being sent. When P2 = 0, the P2 sequence is not being sent. When the modem is configured as a high speed receiver, status bit P2 = 1 indicates the search for the P2 to PN transition is occurring. When P2 = 0, the P2 to PN transition search is not occurring.
PARSL	14:4,5	00	**Parity Select.** In V.23 mode, control bits PARSL select the method by which parity is generated and checked during asynchronous parallel data mode. The options are: **Bit 5 / Bit 4 / Parity Selected** 0 / 0 / Mark Parity 0 / 1 / Space Parity 1 / 0 / Even Parity 1 / 1 / Odd Parity
PDEQZ	08:0	0	**Programmable Digital Equalizer.** When the host has configured the modem as a receiver or transmitter and has set control bit PDEQZ, the programmable digital equalizer is enabled. When control bit PDEQZ is a 0, the programmable digital equalizer is disabled. The programmable digital equalizer defaults to a Japanese 2 link delay equalizer. The default filter coefficients are written to RAM when the modem changes configurations from a mode having 8000 Hz sample rate to a mode having 9600 Hz sample rate.

Table 3-1. Interface Memory Bit Definitions (Cont'd)

Mnemonic	Location	Default	Name/Description
PDM	07:5	0	**Parallel Data Mode.** When control bit PDM is a 1, parallel data mode is selected. If the modem is a transmitter, data for transmission is accepted from DBUFF (10:0-7) in modes other than V.23 or TBUFFER (12:0-7) in V.23 mode (CONF = 24). If the modem is a receiver, the modem provides received data to DBUFF (10:0-7) and to the RXD output pin. The setting of the PDM bit must be followed by the setting of the SETUP bit to become active. When the PDM bit is a 0, serial data mode is selected. If the modem is a transmitter, data for transmission is accepted from the TXD input pin. When the modem is a receiver, the modem provides the received data only to the RXD output pin.
PE	09:0	0	**Parity Error (Parallel Mode).** When set, status bit PE indicates that a character with bad parity was received. When reset, a character with good parity was received. (V.23)
PEN	14:3	0	**Parity Enable (Parallel Mode).** When control bit PEN is set, parity generation and checking is enabled. When PEN is a 0, parity generation and checking is disabled. (V.23) **Note:** Parity bit is NOT masked out in the receive parallel buffer (DBUFF). The Parity bit is the MSB of the character contained in DBUFF. Start and Stop bit(s) are stripped from the data before it is written to DBUFF.
PIA	1F:7	–	**Programmable Interrupt Active.** When control bit PIE is enabled (PIE is a 1) and the interrupt condition is true as specified by ITBMSK, ITADRS, TRIG, and ANDOR, the modem asserts IRQ1# if PIREQ has been previously reset by the host (usually after servicing the previous interrupt). Status bit PIA is set by the modem when the above occurs. PIA is reset when the host resets PIREQ.
PIDR	05:5	0	**Programmable Interrupt at Data Rate.** When control bit PIDR is a 1, the programmable interrupt runs at the data rate. When PIDR is a 0, the programmable interrupt runs at the sample rate (9600 Hz). The PIDR bit is valid in all modes except tone, voice/audio codec, audio, and speakerphone.
PIE	1F:4	0	**Programmable Interrupt Enable.** When control bit PIE is enabled (PIE is a 1) and the interrupt condition is true as specified by ITBMSK, ITADRS, TRIG, and ANDOR, the modem asserts IRQ1# if PIREQ has been previously reset by the host (usually after servicing the previous interrupt). Status bit PIA is set by the modem when the above occurs. When PIE is a 0 (interrupt disabled), ITBMSK, ITADRS, TRIG, ANDOR, and PIREQ have no effect on IRQ1# and PIA.
PIREQ	1F:3	–	**Programmable Interrupt Request.** When control bit PIE is enabled (PIE is a 1) and the interrupt condition is true as specified by ITBMSK, ITADRS, TRIG, and ANDOR, the modem asserts IRQ1# if control bit PIREQ has been previously reset by the host. PIREQ is set by the modem when the programmable interrupt condition is true. The host must reset PIREQ after servicing the interrupt since the modem does not reset PIREQ. If PIREQ is not reset when the interrupt condition occurs again, the modem will not assert IRQ1#.
PN	0C:3	–	**PN Sequence.** When the modem is configured as a high speed transmitter, status bit PN = 1 signals that the PN sequence is being sent. When PN = 0, the PN sequence is not being transmitted. When the modem is configured as a high speed receiver, status bit PN = 1 indicates the PN portion of the training sequence is being received. When PN = 0, the PN portion of training is not being received.
PNDET	0D:6	–	**PN Detected.** When status bit PNDET is a 1, the receiver has detected the PN portion of the training sequence. When PNDET is a 0, PN has not been detected.
PNSUC	08:3	–	**PN Success.** When status bit PNSUC is a 1, the receiver has successfully trained at the end of the PN portion of the high speed training sequence. When PNSUC is a 0, a successful training has not occurred. PNSUC is still valid after the CDET bit is set to a 1.
PR	1D:5	–	**Rate Sequence Period.** When status bit PR is a 1 during transmit, the modem is sending the rate sequence (PR). When reset to a 0, the rate sequence (PR) is not being sent. When set to a 1 during receive, the modem is receiving the rate sequence (PR). When reset to a 0, the rate sequence (PR) is not being received. (V.17 or V.33 modes.)

Table 3-1. Interface Memory Bit Definitions (Cont'd)

Mnemonic	Location	Default	Name/Description
PRDET	1D:4	–	**Rate Sequence Detection.** When status bit PRDET is a 1, the modem receiver has detected a rate sequence pattern containing a proper synchronization bit pattern. (V.17 or V.33 modes.)
RNGDIS	1A:0	0	**Ring Detector Disable.** When control bit RNGDIS is a 1, the Ring Detector is enabled. When RNGDIS is a 0, Ring Detector is disabled. **Note:** The host may set this bit to avoid false ring detection after off-hook. The delay between activation and actual toggling of the external control line will be two sample periods.
RI	17:2	–	**Ring Indicator.** Status bit RI is set when a valid ringing signal is being detected. RI is reset when a valid ringing signal is not being detected. Ringing is selected if pulses are present on GPI7 input in the 15-68 Hz frequency range (default frequency range) for the 8000 Hz sampling rate modes. The RI bit follows the ringing signal with a 1 during the ON time and a 0 during the OFF time. The minimum and maximum valid ring frequencies are host programmable in DSP RAM.
RMM	07:5	0	**Room Monitor.** In Voice Codec and ADPCM Audio Codec modes, setting bit RMM enables the room monitor that routes the PIA Mic input signal to the PIA Line output. Setting both CODECS and RMM bits enables the room monitor that routes the SIA Mic input signal to the PIA Line output. The setting of the RMM bit must be followed by the setting of the SETUP bit to become active.
RTSP	07:7	0	**Request To Send Parallel.** The one state of control bit RTSP begins a transmit sequence. The modem will continue to transmit until RTSP is reset to a 0 (or RTS# is turned off) and the turn-off sequence has been completed. RTSP parallels the operation of the RTS# hardware input pin. These inputs are "ORed" by the modem, except in the Voice Codec and Audio Codec modes.
RX	0D:7	–	**Receive State.** In high speed modes, the modem is in the receive state when status bit RX is a 1; the modem is in the transmit state when RX is a 0.
RXBQ	19:1	0	**Receive Biquad Filter.** In Voice and ADPCM Audio Codec modes, when control bit RXBQ is a 1, the decoder output is filtered by the Receive Biquad Filter. In Speakerphone mode, the received speech is filtered by the Receive Biquad Filter. When RXBQ is 0, the Receive Biquad Filter is disabled.
RXH	18:3	–	**Receive Speech Detect.** In Speakerphone mode, when status bit RXH is a 1, receive speech is detected. When RXH is 0, receive speech is not detected.
SBAD1L	02:0-7	--	**Single Bank RAM Address 1 LSB.** When control bits ACC1 and SBRAM1 are both a 1, SBAD1L contains the LSB of the address used to access the modem's single bank RAM via the Y RAM Data 1 LSB and MSB words (00:0-7 and 01:0-7, respectively).
SBAD1M	03:0-7	--	**Single Bank RAM Address 1 MSB.** When control bits ACC1 and SBRAM1 are both a 1, SBAD1M contains the MSB of the address used to access the modem's single bank RAM via the Y RAM Data 1 LSB and MSB words (00:0-7 and 01:0-7, respectively).
SBAD2L	12:0-7	--	**Single Bank RAM Address 2 LSB.** When control bits ACC2 and SBRAM2 are both a 1, SBAD2L contains the LSB of the address used to access the modem's single bank RAM via the Y RAM Data 2 LSB and MSB words (10:0-7 and 11:0-7, respectively).
SBAD2M	13:0-7	--	**Single Bank RAM Address 2 MSB.** When control bits ACC2 and SBRAM2 are both a 1, SBAD2M contains the MSB of the address used to access the modem's single bank RAM via the Y RAM Data 2 LSB and MSB words (10:0-7 and 11:0-7, respectively).
SBRAM1	1A:6	0	**Single Bank RAM Access 1.** When control bit SBRAM1 is a 1, the modem accesses the single bank RAM associated with the address in SBAD1M and SBAD1L (BR1, CR1, DR1, IO1, and AREX1 must be 0). WRT1 determines if a read or write is performed.
SBRAM2	1A:7	0	**Single Bank RAM Access 2.** When control bit SBRAM2 is a 1, the modem accesses the single bank RAM associated with the address in SBAD2M and SBAD2L (BR2, CR2, DR2, IO2, and AREX2 must be 0). WRT2 determines if a read or write is performed.

Table 3-1. Interface Memory Bit Definitions (Cont'd)

Mnemonic	Location	Default	Name/Description
SCR1	0C:4	–	**Scrambled Ones.** When the modem is configured as a high speed transmitter, status bit SCR1 = 1 indicates scrambled ones are being sent. When SCR1 = 0, scrambled ones are not being sent. When the modem is configured as a high speed receiver, status bit SCR1 = 1 indicates scrambled ones are being received. When SCR1 = 0, scrambled ones are not being received.
SETUP	1F:0	0	**Setup.** Control bit SETUP must be set to a 1 by the host after the host writes a configuration code into the CONF bits (06:0-7) or changes any of bits 0 through 6 in register 07 (07:0-6). This informs the modem to implement the configuration change. The modem resets the SETUP bit to a 0 when the configuration change request is recognized.
SHPR	1D:7	0	**Short Train Rate Sequence.** When control bit SHPR is a 1, the V.17/V.33 rate sequence is included in the short training sequence, which extends the training by 64 baud.
SHTR	07:4	0	**Short Train Mode.** When control bit SHTR is a 1 and the modem is configured as a high speed receiver (see CONF), the modem will perform a short training sequence. A successful long train at the same data rate must precede its short train. (**Note**: For V.17, a successful long train at any data rate must precede its short train.) The setting of the SHTR bit must be followed by the setting of the SETUP bit. The EQSV bit must be set and the EQFZ bit may optionally be set for Short Train operation.
SIAHND	18:6	0	**SIA Handset.** In Speakerphone mode, when control bit SIAHND is a 1, the SIAHND is configured to use microphone input and speaker output. When SIAHND is a 0, the SIAHND is configured to use line input and line output.
SKIP	07:1	0	**SKIP Enable.** When control bit SKIP is a 1, the Voice decoder may skip forward or backward during message playback. When SKIP is a 0, message playback continues as before.
SLOW	14:1	0	**Slower by 50% Playback Speed.** When control bit SLOW is a 1 and the FAST50, FAST33, and NORM control bits are reset, playback time is 150% of normal playback time. SLOW must be reset when another speed is selected. (Voice Codec Mode)
SP/HS	0E:4	1	**Speakerphone/Handset Switch.** In speakerphone mode, when control bit SP/HS is a 1, microphone/speaker operation is enabled; when SP/HS is a 0, handset in place of microphone/speaker is assumed for handset operation**.**
SQEXT	07:2	0	**Squelch Extend.** Control bit SQEXT determines the length of time the modem receiver is inhibited from receiving any signal after transmitter turn-off. The length of time is either 20 ms (SQEXT = 0) or 140 ms (SQEXT = 1). The setting of the SQEXT bit must be followed by the setting of the SETUP bit to become active.
STB	14:2	0	**Stop Bit Number.** When control bit STB is reset, one stop bit is selected; when set, two stop bits are selected. (V.23)
TBUFFER	12:0-7	00	**Transmit Data Buffer**. In V.23 mode (CONF = 24h), the host conveys output data to the transmitter in the parallel mode by writing a data byte to the TBUFFER. The data is transmitted bit 0 first.
TDBE	18:1	1	**Transmit Data Buffer Empty**. When set, status bit TDBE signifies that the modem has read TBUFFER (register 12) and the host can write new data into TBUFFER. This condition can also cause an IRQ to be asserted using the programmable interrupt. The host must clear the bit to transmit data. (V.23)
TDIS	07:6	0	**Training Disable.** When control bit TDIS is a 1, the modem as a receiver is prevented from recognizing a training sequence and entering the training state; as a transmitter the modem will not transmit the training sequence when the RTS# pin or RTSP bit is activated.
TONEPE	19:6	0	**PIA Tone Enable.** In speakerphone mode, control bit TONEPE enables (TONEPE = 1) or disables (TONEPE = 0) tone to the PIA DAC while in tone transmit mode (TTONEE = 1).
TONESE	19:5	0	**SIA Tone Enable.** In speakerphone mode, control bit TONESE enables (TONESE = 1) or disables (TONESE = 0) tone to the SIA DAC while in tone transmit mode (TTONEE = 1).

Table 3-1. Interface Memory Bit Definitions (Cont'd)

Mnemonic	Location	Default	Name/Description
TTONEE	0E:7	0	**Tone Transmit Enable.** In speakerphone mode, control bit TTONEE enables (TTONEE = 1) or disables (TTONEE = 0) tone transmit mode. Depending upon the status of TONEPE and TONESE, the corresponding voice channel will be muted for the whole period of the tone transmit mode. TTONEE must be reset in order to re-activate voice channel.
TRIG	0A:6-7	0	**Interrupt Triggering.** These two bits select how the programmable interrupt is to occur if this interrupt is enabled (PIE bit = 1). The host has the option to be continuously interrupted whenever the interrupt condition is true (DC level triggered), to be interrupted only when the interrupt condition transitions from false to true (positive edge triggered), to be interrupted only when the interrupt condition transitions from true to false (negative edge triggered), or to be interrupted when the interrupt condition transitions from false to true or from true to false (edge triggered): **Bit 7 / Bit 6 / Description** 0 0 DC Level Triggered 0 1 Positive Edge Triggered 1 0 Negative Edge Triggered 1 1 Edge Triggered
TXBQ	19:0	0	**Transmit Biquad Filter.** In Voice and ADPCM Audio Codec modes, when control bit TXBQ is a 1, the voice and audio coder input samples are filtered by the Transmit Biquad Filter before coding. In Speakerphone mode, the transmit speech is filtered by the Transmit Biquad Filter. When TXBQ is a 0, the Transmit Biquad Filter is disabled.
TXH	18:4	–	**Transmit Speech Detect.** In Speakerphone mode, when status bit TXH is a 1, transmit speech is detected. When TXH is a 0, transmit speech is not detected.
TXSEN	18:6	0	**Transmit Sensitivity.** In Speakerphone mode, when control bit TXSEN is a 1, the transmit speech detector is more sensitive to lower/softer voice levels. When TXSEN is a 0, transmit speech is not detected (TXH is a 0) with low level voice.
TXSQ	14:7	0	**Transmitter Squelch.** When control bit TXSQ is set, the transmitter analog output is squelched (forced to zero). All other transmitter functions continue as normal. When TXSQ is reset, the transmitter output functions normally. (V.23)
UE	08:3	0	**Underrun Error (Parallel Mode)**. If the host does not load in a new byte of data within X bit times of the modem setting bit TDBE, an underrun condition occurs and UE is set by the modem, The actual number of bit times depends upon the number of stop bits and word size selected. (V.23) The modem will reset UE whenever it sets TDBE.
V23HDX	15:0	0	**V.23 Half Duplex.** When control bit V23HDX is set, the modem operates in V.23/1200 half duplex. The transmitter and receiver must be set to the same V.23 configuration, 1200 bps (CONF = 24h). Carrier is under RTS control. The RTS-CTS delay is adjustable in DSP RAM. ANS should also be set to zero.
VOLDWN	0E:5	0	**Volume Down.** In speakerphone mode the speaker volume is decreased by 2 dB each time VOLDWN is set. In the Voice/Audio Codec mode, the line/speaker volume is decreased by 2 dB each time VOLDWN is set. VOLDWN is reset by the modem.
VOLUP	0E:6	0	**Volume Up.** In speakerphone mode the speaker volume is increased by 2 dB each time VOLUP is set. In the Voice/Audio Codec mode, the line/speaker volume is increased by 2 dB each time VOLUP is set. VOLUP is reset by the modem.
VOVUN	17:0	0	**Voice Overrun or Underrun.** In voice/audio codec mode, status bit VOVUN is set when the host fails to access the DBUFF input or output before new data is needed or available. VOVUN is reset when the voice/audio coder/decoder data buffer is available for proper data transfer. An overrun condition in the voice/audio coder suspends recording of new samples until the host reads DBUFF. An underrun condition in the voice/audio decoder suspends playback of data until the host writes DBUFF input.
VOX	17:3	0	**Voice Detected.** In voice/audio codec mode, status bit VOX is set when the voice/audio coder is detecting voice/audio and is reset when the voice/audio coder is not detecting voice/audio.

Table 3-1. Interface Memory Bit Definitions (Cont'd)

Mnemonic	Location	Default	Name/Description
VOXHI	19:3	--	**VOX High Energy Detect.** In Speakerphone, Voice Codec, and ADPCM Audio Codec modes when status bit VOXHI is a 1, the receive input signal energy is greater than the Sample Rate VOX turn-on threshold. When VOXHI is a 0, the receive input signal energy is less than the Sample Rate VOX turn-on threshold.
VOXLO	19:4	--	**VOX Low Energy Detect.** In Speakerphone, Voice Codec, and ADPCM Audio Codec modes when status bit VOXLO is a 1, the receive input signal energy is greater than the Sample Rate VOX turn-off threshold. When VOXL0 is a 0, the receive input signal energy is less than the Sample Rate VOX turn-off threshold.
VOXREC	1A:3	0	**Voice Activated Recording.** In voice/audio codec mode, when control bit VOXREC is a 1 and CDEN is a 1, message encoding is delayed until status bit VOX is set (thus eliminating encoding of beginning message silence). Voice activated recording provides maximum RAM storage efficiency. When VOXREC is a 0, message encoding is not delayed.
WDSZ	14:0,1	--	**Data Word Size (Parallel Mode).** In V.23 mode, the WDSZ bits set the number of data bits per character as follows: **Bit 1 / Bit 0 / Data Bits/Character** 0 / 0 / 5 0 / 1 / 6 1 / 0 / 7 1 / 1 / 8
WRT1	05:1	0	**RAM Write 1.** When control bit WRT1 is a 1 and ACC1 is a 1, the modem writes the data from the Y RAM Data 1 registers into its internal RAM at the location addressed by AREX1, ADD1, and CR1. (When the most significant bit of ADD1 is a 0, the write is performed to the X RAM location; when a 1, the write is to the Y RAM location.) When WRT1 is a 0 and ACC1 is set to a 1, the modem reads data from its internal RAM from the locations addressed by AREX1, ADD1, and CR1, and stores the data into the X RAM Data 1 registers and Y RAM Data 1 registers, respectively.
WRT2	15:1	0	**RAM Write 2**. When control bit WRT2 is a 1 and ACC2 is a 1, the modem writes the data from the Y RAM Data 2 registers into its internal RAM at the location addressed by AREX2, ADD2, and CR2. (When the most significant bit of ADD2 is a 0, the write is performed to the X RAM location; when a 1, the write is to the Y RAM location.) When WRT2 is a 0 and ACC2 is a 1, the modem reads data from its internal RAM from the locations addressed by AREX2, ADD2, and CR2, and stores the data into the X RAM Data 2 registers and Y RAM Data 2 registers, respectively.
XDAL1	02:0-7	–	**X RAM Data 1 LSB.** XDAL1 is the LSB of the 16-bit X RAM 1 data word used in reading X RAM locations.
XDAL2	12:0-7	–	**X RAM Data 2 LSB.** XDAL2 is the LSB of the 16-bit X RAM 2 data word used in reading X RAM locations.
XDAM1	03:0-7	–	**X RAM Data 1 MSB.** XDAM1 is the most significant byte of the 16-bit X RAM 1 data word used in reading X RAM locations.
XDAM2	13:0-7	–	**X RAM Data 2 MSB.** XDAM2 is the most significant byte of the 16-bit X RAM 2 data word used in reading X RAM locations.
YDAL1	00:0-7	–	**Y RAM Data 1 LSB.** YDAL1 is the LSB of the 16-bit Y RAM 1 data word used in reading Y RAM locations, or writing X or Y RAM locations in the modem.
YDAL2	10:0-7	–	**Y RAM Data 2 LSB.** YDAL2 is the LSB of the 16-bit Y RAM 2 data word used in reading Y RAM locations, or writing X or Y RAM locations in the modem.
YDAM1	01:0-7	–	**Y RAM Data 1 MSB.** YDAM1 is the MSB of the 16-bit Y RAM 1 data word used in reading Y RAM locations, or writing X or Y RAM locations in the modem.
YDAM2	11:0-7	–	**Y RAM Data 2 MSB.** YDAM2 is the MSB of the 16-bit Y RAM 2 data word used in reading Y RAM locations, or writing X or Y RAM locations in the modem.
ZEROC	09:4	0	**Zero Clamp.** In HDLC mode, when control bit ZEROC is a 1 and ABIDL is a 1, the modem will transmit continuous zeros. When ZEROC is a 0 and ABIDL is a 1, the modem will transmit continuous ones. If ABIDL is a 0, ZEROC is disabled.

3.2 SOFTWARE INTERFACE CONSIDERATIONS

3.2.1 Parallel Data Transfer

Register 10 in the interface memory is the Data Buffer (DBUFF). The modem and host synchronize parallel data transfer by observing the state of the Buffer 2 Available bit, B2A (1E:3). RAM Access 2 is not available when the modem is in parallel data mode. The flowchart in Figure 3-2 is used for parallel data transfer.

3.2.1.1 Receiving Parallel Data

In the parallel data mode (PDM = 1), the modem writes to register DBUFF every eight bit times. The modem sets the B2A bit when received data is available. The host resets the B2A bit by reading DBUFF. After the modem sets B2A, the host must respond within eight bit times or else the modem writes over register DBUFF.

While receiving, if the energy drops below the turn-off threshold for a sufficient period of time, the modem writes the last bits of received data to register DBUFF before terminating the receive process.

The modem writes the first bit of received data to the least significant bit of register DBUFF, and writes the last bit of received data to the most significant bit of register DBUFF.

3.2.1.2 Transmitting Parallel Data

The modem reads register DBUFF every eight bit times when transmitting. The modem sets the B2A bit when requesting transmit data. The host resets the B2A bit by writing to DBUFF. After the modem sets B2A, the host must respond within eight bit times or else the modem retransmits the data in register DBUFF.

If RTSP bit is reset, or SETUP bit is set while transmitting, the modem sends all of the data previously read from register DBUFF before terminating the transmit process.

The modem transmits the least significant bit of register DBUFF first, and transmits the most significant bit of register DBUFF last.

3.2.2 Programmable Interrupt Feature

The interface memory interrupt feature enables the host to select an interrupt to occur on any combination of bits within an interface memory register.

3.2.2.1 Programmable Interrupt Bits

The programmable interrupt routine runs at the sample rate in all transmit and receive modes if PIDR is a 0. The programmable interrupt can run at the data rate if PIDR is a 1. If the host sets the Programmable Interrupt Enable bit, PIE (1F:4), the modem sets the Programmable Interrupt Active bit, PIA (1F:7), and IRQ1# goes low when the interrupt condition is true. The Programmable Interrupt Request bit, PIREQ (1F:3), is set by the modem whenever the interrupt condition is true. The host must reset PIREQ after servicing the interrupt.

An interrupt may occur only within a single interface memory register based upon any combination of bits. For example, the host may select register 09h and generate an interrupt whenever bits 09:7, 09:4, and/or 09:3 are set, but may not select bits 08:7 and 09:2 to generate an interrupt. The register is selected by specifying the Interrupt Address, ITADRS (0A:0-4). (See ITADRS in Table 3-1.)

The Interrupt Bit Mask register, ITBMSK (0B:0-7), selects the bits to be tested in the interface memory register specified by ITADRS. For example, if ITBMSK is equal to FFh, all the bits are selected; if ITBMSK is equal to 0Fh, the four least significant bits are selected.

3.2.2.2 Programmable Interrupt Operating Modes

There are two operating modes (AND or OR) with each mode having four trigger options. The ANDOR bit selects the operating mode. The TRIG bits (0A:6-7) select the triggering option. (See ANDOR and TRIG bits in Table 3-1).

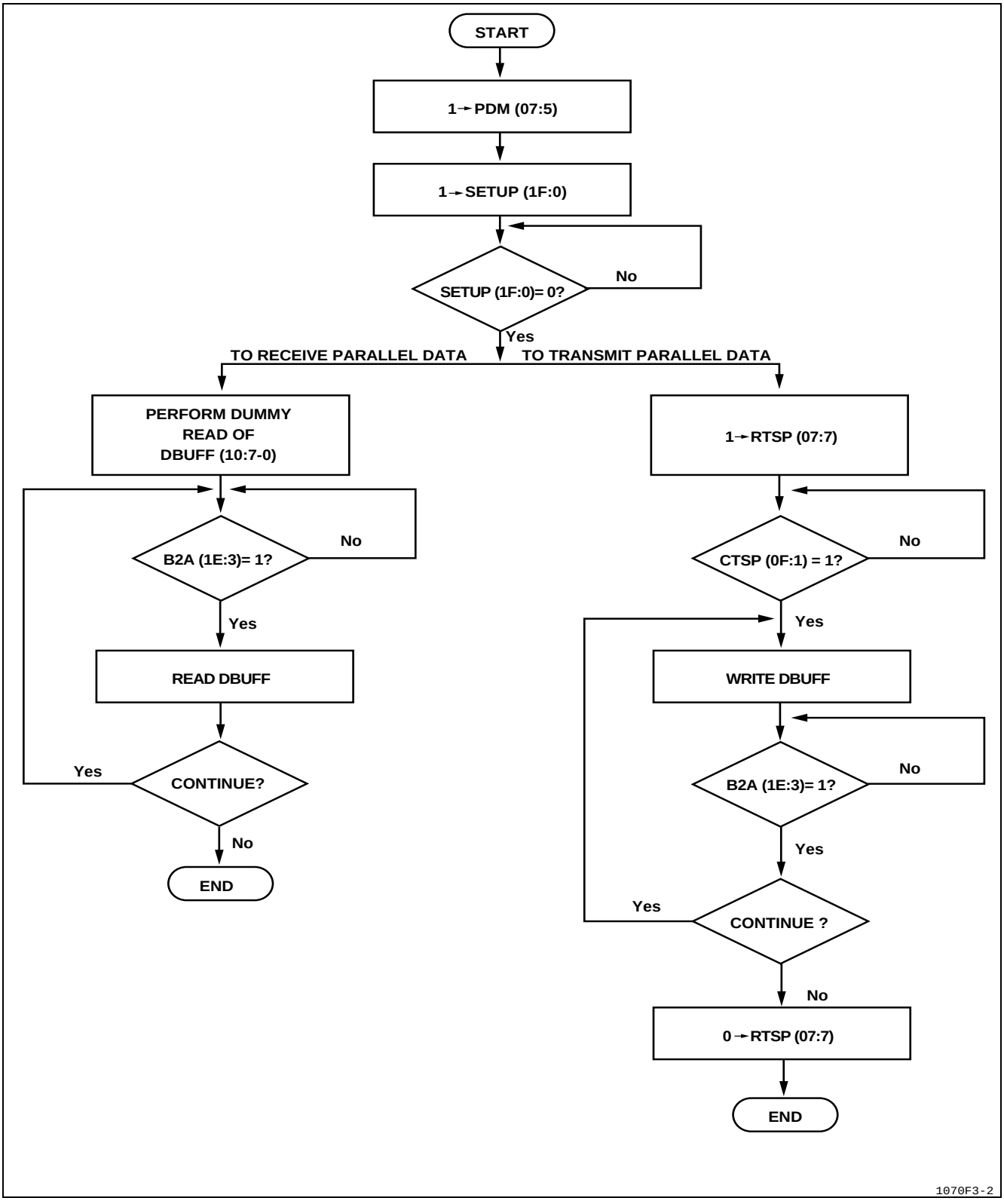

Figure 3-2. Parallel Data Transfer Routine

3.2.3 8-Bit PCM Audio Codec Mode Operation

The 8-bit Audio Mode operates when CONF = 82h.

3.2.3.1 8-Bit PCM Audio Codec Mode Transmitter

This mode allows the transmission of 8-bit audio messages.

8-bit Audio Mode transmitter operates when CONF = 82h and the RTSP bit is a 1. The host must also disable RAM Access 1 (reset ACC1 to a 0).

The value in register 00 is sent to the D/A converter for transmission. The modem sets the B1A bit every sample time to indicate that the value in register 00 has been transmitted. B1A is reset when the host writes the next byte.

3.2.3.2 8-Bit PCM Audio Codec Mode Receiver

This mode allows the recording of 8-bit audio messages.

8-bit Audio Mode receiver operates when CONF = 82h and the RTSP bit is a 0.

The host reads the A/D sample from register 00 using the DSP RAM Access Code No. 2 (Table 4-1). Reading the A/D sample simultaneously resets the B1A bit.

The slew rate is set to zero upon entering this configuration. After configuring the modem, the host must immediately write an AGC Slew Rate to DSP RAM. The AGC gain may be changed by writing to the AGC Gain Word and the maximum AGC gain may be changed by writing to the Receiver Sensitivity (MAXG). (See Section 4.)

3.2.4 16-Bit PCM Audio Codec Mode Operation

The 16-bit Audio Mode operates when CONF = 86h.

3.2.4.1 16-Bit PCM Audio Codec Mode Transmitter

This mode allows the transmission of high quality 16-bit audio messages.

16-bit Audio Mode transmitter operates when CONF = 86h and the RTSP bit is a 1. The host must also disable RAM Access 1 (reset ACC1 to a 0).

The values in registers 01 (most significant byte) and 00 (least significant byte) are sent to the D/A converter for transmission. The modem sets the B1A bit every sample time to indicate that the values in registers 00 and 01 have been transmitted. B1A is reset when the host writes the least significant byte into register 00; therefore, it is recommended that the most significant byte first be written to register 01 followed by the least significant byte to register 00.

3.2.4.2 16-Bit PCM Audio Codec Mode Receiver

This mode allows the recording of high quality 16-bit audio messages.

16-bit Audio Mode receiver operates when CONF = 86h and the RTSP bit is a 0.

The host reads the A/D sample from registers 01 (most significant byte) and 00 (least significant byte). B1A is reset when the host reads the least significant byte from register 00; therefore, it is recommended that the most significant byte first be read from register 01 followed by the least significant byte from register 00.

The slew rate is set to zero upon entering this configuration. After configuring the modem, the host must immediately write an AGC Slew Rate to DSP RAM. The AGC gain may be changed by writing to the AGC Gain Word and the maximum AGC gain may be changed by writing to the Receiver Sensitivity (MAXG). (See Section 4)

3.2.5 DTMF Receiver

3.2.5.1 Mode Selection and Description

The DTMF receiver operates concurrently with the FSK receiver and the three tone detectors. The DTMF receiver operates concurrently with Type II Caller ID CAS detectors and three tone detectors in the Voice Codec, Audio Codec, and Speakerphone modes.

The encoded DTMF receiver output is written into the four least significant bits of register 1C.

The modem sets the DTMF Signal Detected status bit, DTMFD (1C:4), to a 1 whenever a DTMF signal is successfully detected. The host must reset DTMFD after reading the register, otherwise, two or more successive detections of the same symbol may go unnoticed.

3.2.5.2 DTMF Reception Status Bits

Other status bits have been included in register 1C to facilitate host DTMF detection, primarily when used with the programmable interrupt. The Early Detection bit, EDET (1C:7), may set to a 1 approximately 20 ms after signal energy is detected. Setting this bit informs the host that the received signal appears to be a DTMF signal, but the modem has not yet completed its processing.

The Dual Tone Detected bit, DTDET (1C:6), may set to a 1 approximately 11 ms following EDET setting. DTDET is set when the received signal satisfies all DTMF criteria except on-time, off-time, and cycle-time. At this time the encoded DTMF receiver output is made available to the host in the DTMF Output Word (1C:0-3). If DTDET is not set to a 1, then the received signal has failed one or more criteria, and consequently the modem resets EDET and resumes its search.

After the on-time criteria is satisfied, the modem sets the On-Time Satisfied bit, OTS (1C:5), to a 1. If the on-time is not satisfied, the modem resets bits EDET and DTDET and resumes its search. As soon as both the off-time and cycle-time are satisfied, DTMFD is set to a 1. If these times are not satisfied, then EDET, DTDET, and OTS are reset and the receiver resumes its search. Also following DTMFD setting, EDET, DTDET, and OTS are reset. The relationship between these status bits for a valid DTMF signal is illustrated in Figure 3-3.

If, after DTDET is set to a 1, the host resets DTDET before OTS sets to a 1, then the DTMF receiver is reset to its initial state except for the programmable DTMF parameters which retain their present values (see Section 4).

If, after OTS is set to a 1, the host resets OTS before DTMFD sets to a 1, then the DTMF receiver is reset to its initial state except for the programmable DTMF parameters which retain their present values (see Section 4). See Table 13-1 for DTMF receiver performance characteristics.

Note: The DTMF copy bits (EDETC, DTDETC, OTSC, and DTMFDC in register 17) copy the corresponding actual DTMF status bits (EDET, DTDET, OTS, and DTMFD, respectively, in register 1C). The copy bits are located in the same register as the status bits for tone detection, Type II Caller ID detection, ring detection, and Voice Mode status bits to facilitate programmable interrupt service. Clearing the DTMFD status bit will automatically clear the corresponding DTMFDC copy bit within one sample time.

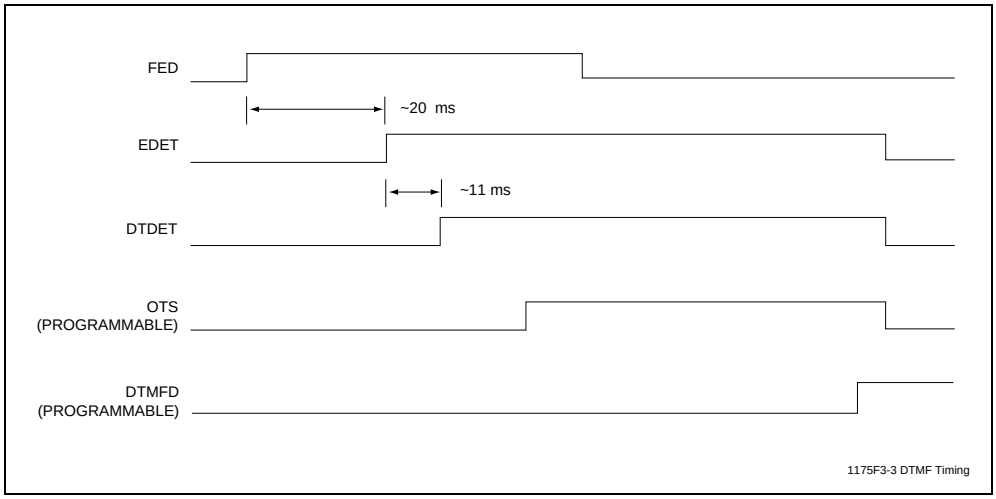

Figure 3-3. DTMF Receiver Status Bit Timing

3.2.6 V.21 Channel 2 FSK 7E Flag Detector

The V.21 Channel 2 FSK 7E flag detector can be used to detect the presence of the energy produced by the T.30 FSK 7E flag preamble while the modem is configured in any high speed receiver mode except for V.27 ter short train. FSKFLS and FSK7E bits indicate the status of the detection process (see Table 3-1 for bits description). The detection process starts after the modem enters its receiver idle mode and a waiting period of 8 bauds after FED turns on (Figure 3-4). The modem receiver normally enters the idle mode after any of the following events:

1. The host setting of SETUP bit.
2. After FED turns off with enough lapse time (about 30 ms in V.29) in data mode to return to the idle mode.
3. After the modem detects a significant gain hit in the data mode (RLSD on). The presence of an FSK signal when noise is above turn-on threshold will generate such a hit.

After the modem enters the idle mode, the modem will reset FSKFLS and FSK7E bits to a 0. If FED is on, then the modem will set FSKFLS to a 1 and start the detection process. After the completion of the detection process, if the FSK 7E signal is present the modem will set FSK7E bit to a 1 and reset the FSKFLS bit to a 0. The FSK7E bit will remain at this state until the modem enters the idle mode again or the host resets the bit to a 0.

The detector will not work properly if the modem is not allowed to complete the detection process, which lasts about 106.67 ms after FSKFLS goes to a 1.

In the event that the host sets the control bit TDIS to a 1 after the modem enters its idle mode, the modem will quickly enter the data mode after FED turns on and, hence, not allow enough time for the detector to complete its detection process. Therefore, the TDIS bit must be reset to a 0 to assure the proper function of the FSK 7E flag detector.

An example of the FSK 7E flag detector in a signal recognition algorithm is illustrated in Figure 9-26.

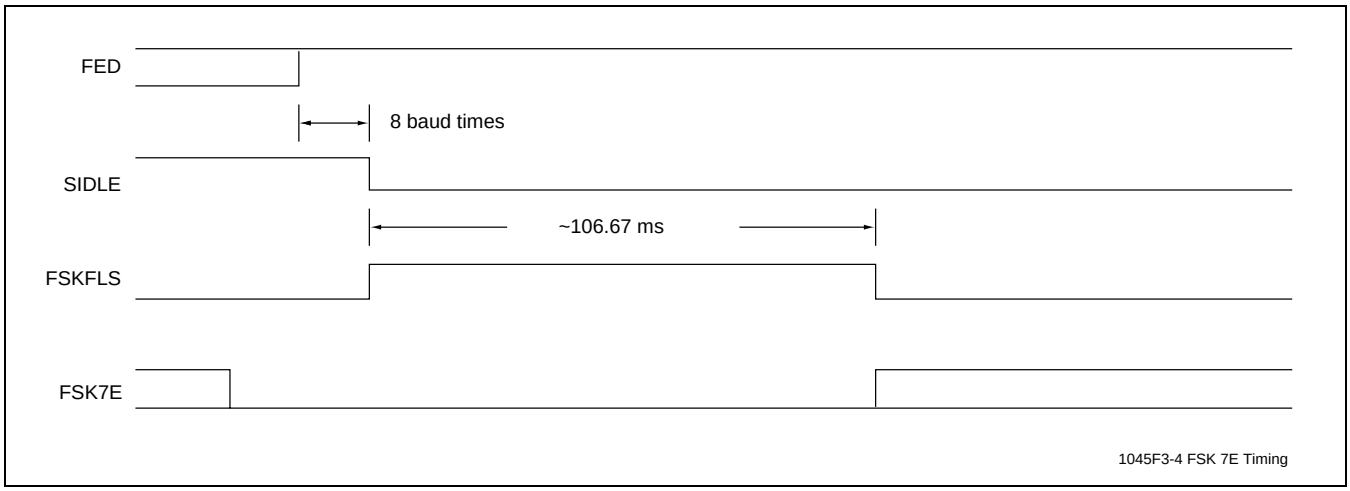

Figure 3-4. FSK 7E Flag Detector Timing

3.2.7 V.23 Mode Operation

The V.23 mode operates when CONF = 24h. DSP RAM Access 2 does not operate in this mode.

3.2.7.1 V.23 Mode Transmitter and Receiver

In both V.23 Full-duplex and Half-duplex operation, the transmitter is activated by RTSn (low) or RTSP = 1. CTSn (low) and CTSP will respond as described in Table 1-1, and data may be then sent using the TXD pin (PDM = 0) or TBUFFER (PDM = 1). V.23 data received by the modem will be presented to the host at RXD (PDM = 0) or both DBUFF and RXD (PDM = 1).

During V.23 communication, the transmitter squelch (TXSQ), break send (BRKS), and Receive Compromise Equalizer (CEQ) may be activated at any time. All other changes to the V.23 configuration (word size, parity, stop bit selection, parallel data mode, half duplex mode) require the host to set the SETUP bit before any action is taken by the modem.

In serial mode (PDM = 0), start, stop, data length, and parity are all determined by the host during transmission, and all received start, stop, and parity bits are presented to the host at the RXD pin.

In parallel mode (PDM = 1), start, stop, data length, and parity selection is done via the modem interface memory. During transmission, the host need only provide data bits to the TBUFFER register, and the modem will add the requested start, stop, and parity bits. During reception, start and stop bits are always stripped by the modem. The parity bit is NOT, in general, stripped from the data by the modem, and remains with the data as the most significant bit, for backward compatibility with previous Rockwell products. In parallel mode, the modem senses overrun, underrun, framing, and parity errors.

Figure 3-5 shows how to setup various V.23 transmit and receive modes.

3.2.8 Caller ID Mode Operation

The Caller ID (V.23 Receive only) mode operates when CONF = 22h.

3.2.8.1 Control Bits

The Receive Compromise Equalizer included in V.23 mode also functions in Caller ID mode. It may be enabled at any time during Caller ID reception by setting CEQ to a 1.

The V.23 control bits ANS (Answer) and V23HDX must be set to zero in Caller ID mode. Caller ID mode functions as described in Section 10. Figure 3-6 shows Caller ID setup.

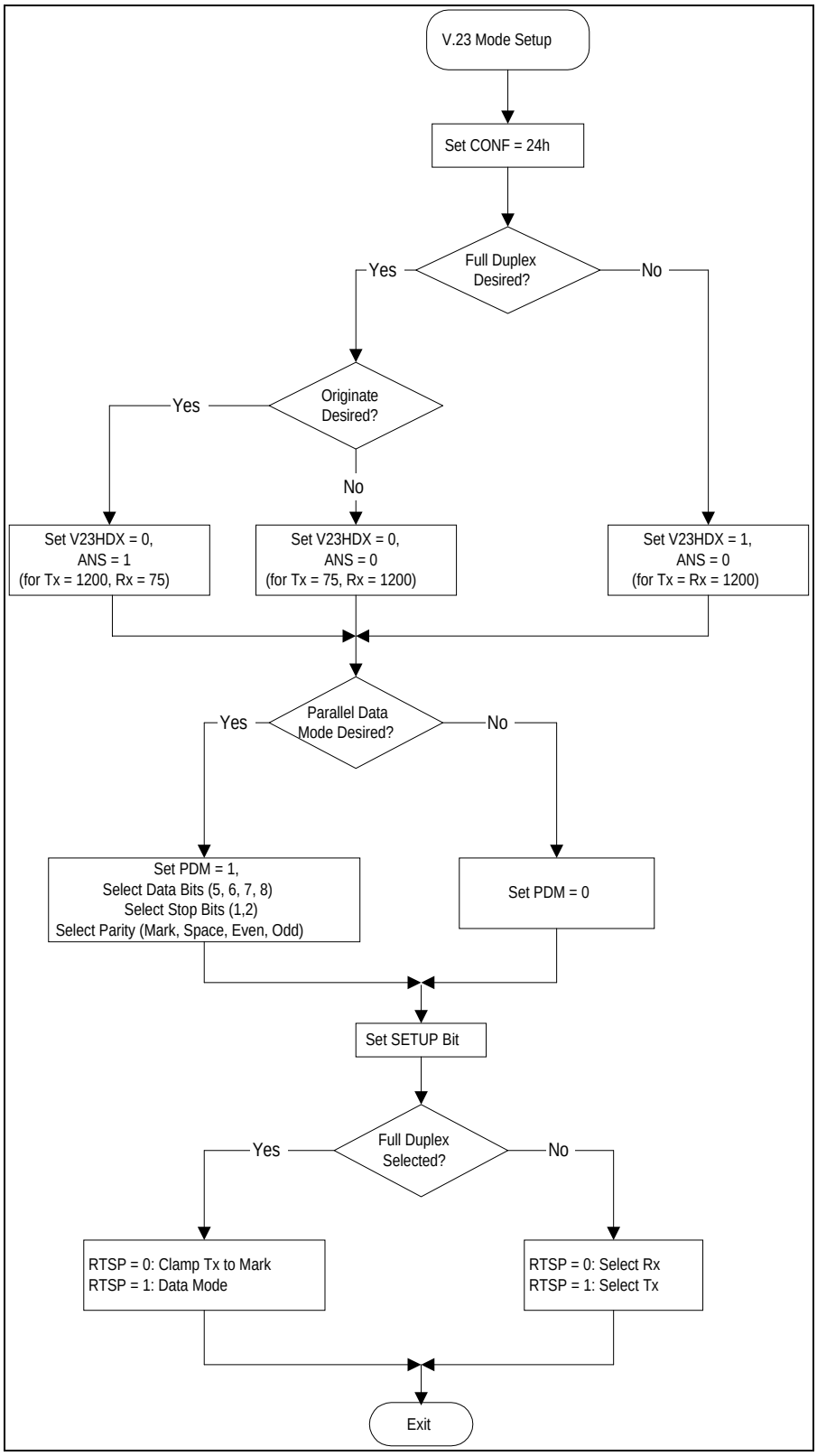

Figure 3-5. V.23 Modes Setup Procedure

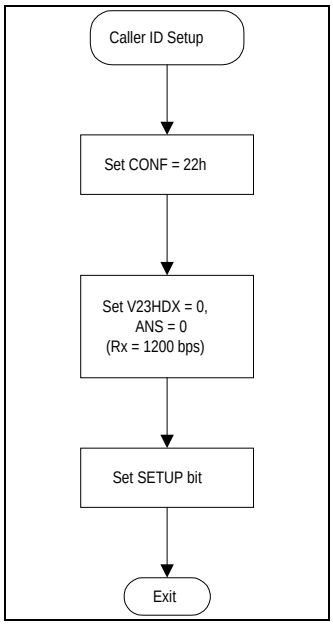

Figure 3-6. Caller ID Mode Setup Procedure

3.2.9 High Speed Timing

Several status bits in the DSP interface memory are useful to the host for monitoring various receiver conditions. These bits are significant during training and data reception/transmission. Figure 3-7 illustrates the timing relationships between these bits. Table 3-2 lists the timing values.

Table 3-2. High Speed Status Bit Timing

Mode	T1	T2	T3	T4	T5	T6	T7	T8	T9	T10	T11**	T13	Units
V.33 & V.17 Long	187.5	20.0	106.7	1240	26.7	20.0	6.3	4.2	10.9	13	20	40	ms
V.33 & V.17 Short	187.5	20.0	106.7	15.8	0*	20.0	4.6	4.2	10.9	13	20	40	ms
V.29 Long	187.5	20.0	53.3	160	0	20.0	6.3	4.2	4.2	5	20	34	ms
V.29 Short	187.5	20.0	41.7	25.8	0	7.5	4.6	4.2	4.2	5	20	34	ms
V.27 ter, 4800 Long	187.5	20.0	31.2	671	0	5.0	9.4	6.3	6.3	7	20	19	ms
V.27 ter, 4800 Short	187.5	20.0	8.8	36.3	0	5.0	3.1	6.3	6.3	7	20	19	ms
V.27 ter, 2400 Long	187.5	20.0	41.6	895	0	6.6	12.5	8.3	8.3	10	20	24	ms
V.27 ter, 2400 Short	187.5	20.0	11.7	48.3	0	6.6	4.2	8.3	8.3	10	20	24	ms

Notes:

* SHPR = 0; T5 = 26.5 ms for SHPR = 1.

** 140 ms if SQEXT = 1.

*** In parallel mode data mode with HDLC bit off, turning RTS# off immediately after loading the last byte (see Section 3.): T12 = 8 bit times.
In parallel mode data mode with HDLC bit on, turning RTS# off immediately after loading the last byte (see Section 5): T12 = 32 bit times.

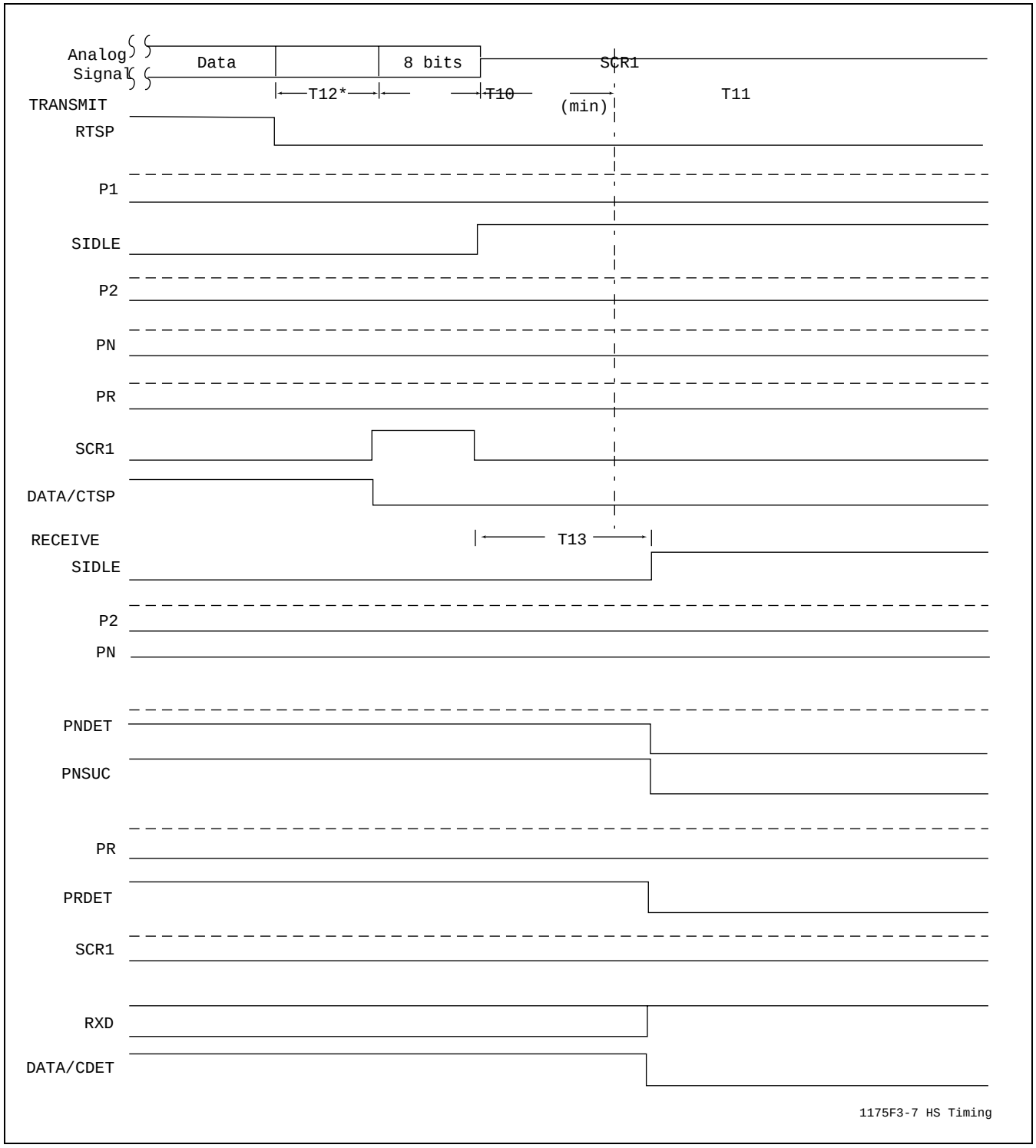

Figure 3-7. High Speed Mode Status Bit Timing

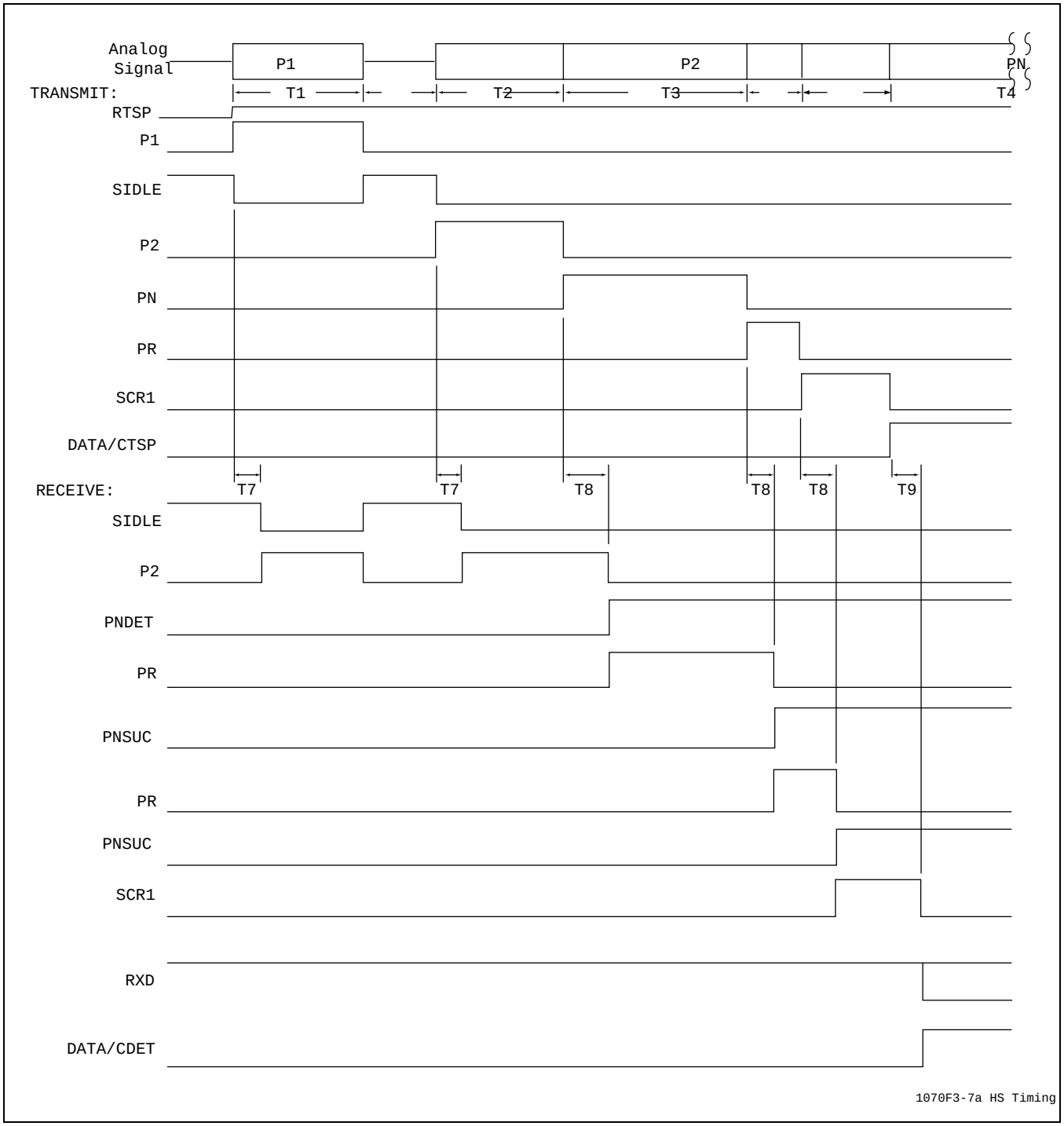

Figure 3-7. High Speed Mode Status Bit Timing (Cont'd)

3.2.10 Power-On/Reset DSP Test Mode

After Power-On Reset (POR), the modem enters into a test mode and calculates checksums on ROM, RAM and multiplier sections. The results of the checksums and ASCII values corresponding to the DSP device part number and code revision letter are written to the interface memory registers 10h through 19h approximately 20 milliseconds after POR signal goes off (see Table 3-3). The contents will remain in these registers for about 4 ms or until register 10 is read by the host.

Table 3-3. Power-On Reset Self-Test Values

Contents	Register (Hex)	Value (Hex)
Multiplier checksum upper word	19	46
Multiplier checksum lower word	18	EE
RAM checksum upper word	17	D2/07
RAM checksum lower word	16	81/04
ROM checksum upper word	15	39
ROM checksum lower word	14	37/34
DSP device upper number ASCII	13	30/35
DSP device lower word ASCII	12	30
ASCII value for " " (space)	11	20
DSP device code revision number (example = "A")	10	41

After POR, the contents of these registers are read using the following RAM Access Codes:

Table 3-4. RAM Access Codes

Function	SBRAMx	BRx	CRx	IOx	AREXx	ADDx	Read Reg. No.
DSP Device Number	0	0	0	1	0	DF	0,1
DSP Device Code Revision Number	0	0	0	1	0	DE	0,1
ROM Checksum	0	0	0	1	0	DD	0,1
Multiplier Checksum	0	0	0	1	0	DC	0,1
RAM Checksum	0	0	0	1	0	DB	0,1

Note:

1 - Read Reg. No. column only shows the registers to use when x=1. When x=2, the Read Reg. No. column value must be added to 10h.

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4. DSP RAM ACCESS

The DSP contains 16-bit words RAM. Since DSP is optimized for performing complex arithmetic, RAM is organized into real (X RAM) and imaginary (Y RAM) parts. The host processor reads or writes X RAM and Y RAM. The DSP also contains a single bank RAM (SBADxy) which the host can read or write.

4.1 INTERFACE MEMORY ACCESS TO DSP RAM

DSP interface memory is an intermediary during data exchanges between the host and DSP RAM. The address stored in interface memory RAM address registers by the host determines the DSP RAM address for data access.

The 16-bit words are transferred between DSP RAM and DSP interface memory once each baud (frame in voice and sample in speakerphone), or sample time, as selected by the BR1 and BR2 bits. The baud (frame) rate is determined by the selected configuration, but the sample rate is fixed at 9600 Hz (8000 Hz in voice and speakerphone).

Two RAM Access bits in the DSP interface memory tell the DSP to access the X RAM and/or Y RAM. The transfer is initiated by the host setting the ACC1 and/or the ACC2 bit(s). The DSP tests these bits each baud, data, or sample period.

4.1.1 Host Programmable Data

The DSP RAM access functions, codes, and registers are identified in Table 4-1. For Speakerphone mode, DSP RAM access functions, codes, and registers are identified in Section 12.

4.1.2 Host DSP RAM Read And Write Procedures

The modem main RAM has four RAM banks: Data RAM Real, Data RAM Imaginary, Coefficient RAM Real, and Coefficient RAM Imaginary. The designation (x = 1, 2) indicates x may be replaced by either 1 or 2, with 1 and 2 referring to RAM Access 1 and RAM Access 2, respectively.

To access the main RAM, write the desired RAM access code into ADDx and AREXx (x = 1, 2). Bits 0 through 6 and AREXx (x = 1, 2) of the access code specify the RAM location and bit 7 of the access code specifies a real (0) or imaginary (1) RAM location. The CRx (x = 1, 2) bit controls whether the coefficient RAM (1) or data RAM (0) is accessed.

To access single bank RAM access, write the address to SBADxM and SBADxL and set the SBRAMx bit.

4.1.3 DSP RAM Read Procedure

The DSP RAM read procedure is a 32-bit transfer from DSP RAM to the interface memory which transfers both the X RAM and Y RAM simultaneously (Figure 4-1).

1. Before reading from the DSP, reset ACC1 and/or ACC2 to a 0, then read YDAL1 to reset B1A and/or YDAL2 to reset B2A.
2. Reset WRT1 and/or WRT2 to a 0 to inform the DSP that a RAM read will occur when ACC1 and/or ACC2 is set to a 1.
3. For main RAM access, write the RAM address into ADD1 and AREX1 and/or ADD2 and AREX2, reset SBRAMx, then set CR1 and IO1, and/or CR2 and IO2 to chosen values. For single bank RAM access, write the address to SBADxM and SBADxL and set the SBRAMx bit.
4. Set ACC1 and/or ACC2 to a 1 to signal the DSP to perform the RAM read.
5. The DSP sets B1A and/or B2A after transferring the contents of RAM into the interface memory registers.
6. If B1I1E and/or B2I1E is a 1, the DSP asserts IRQ1# and sets B1IA and/or B2IA to a 1 to inform the host that setting of B1A and/or B2A is the cause.
7. If B1I2E and/or B2I2E is a 1, the DSP asserts IRQ2# when B1A and/or B2A is a 1. B1I2E and B2I2E have no effect on B1IA and B2IA, respectively.
8. Read XDAM1, XDAL1, YDAM1, and YDAL1; and/or XDAM2, XDAL2, YDAM2, and YDAL2; in this order.

Note: Reading YDAL1 clears B1IA and/or YDAL2 clears B2IA, which causes IRQ1# to return high if no other interrupt requests are pending.

9. IRQ2# returns high only when B1A and/or B2A are reset to 0.

4.1.4 DSP RAM Write Procedure

The RAM write procedure is a 16-bit transfer from interface memory to DSP RAM allowing the transfer of X RAM data or Y RAM data to occur each baud data, or sample time (Figure 4-1).

1. Before writing to DSP interface memory, reset ACC1 and/or ACC2 to a 0; then read YDAL1 and/or YDAL2 to reset B1A and/or B2A, respectively.
2. For main RAM access, write the RAM address into ADD1 and AREX1 and/or ADD2 and AREX2, reset SBRAMx, then set CR1 and IO1 and/or CR2, and IO2 to the chosen values. For single bank RAM access, write the address to SBADxM and SBADxL and set the SBRAMx bit.
3. Set WRT1 and/or WRT2 to a 1 to inform the DSP that a RAM write will occur when ACC1 and/or ACC2 is set to a 1.
4. Write the desired data into the interface memory RAM Data registers YDAL1 and YDAM1 and/or YDAL2 and YDAM2.
5. Set ACC1 and/or ACC2 to a 1 to signal the DSP to perform the RAM write.
6. The DSP sets B1A and/or B2A after transferring the contents of the interface memory registers into RAM.
7. If B1I1E or B2I1E is a 1, IRQ1# is also asserted and B1IA and/or B2IA is set to a 1 when B1A and/or B2A is set to a 1 by the DSP.
8. If B1I2E and/or B2I2E is a 1, the DSP asserts IRQ2# when B1A and/or B2A is a 1. B1I2E and B2I2E have no effect on B1IA and B2IA, respectively.
9. Clear B1IA and/or B2IA by writing into YDAL1 and/or YDAL2, which causes IRQ1# to return high if no other interrupt requests are pending.
10. IRQ2# returns high only when B1A and/or B2A are reset to 0.

Table 4-1. Modem DSP RAM Access Codes

No.[1, 2]	Function	SBRAMx	BRx	CRx	IOx	AREXx	ADDx	Read Reg. No.[4]
1a	Received Signal Sample (Pre-AGC)	0	0	1	0	0	55	2,3
1b	Received Signal Sample (Post-AGC)	0	0	0	0	0	15	2,3
2	Received Signal Sample - 8-bit Audio Mode (Post-AGC)	0	0	0	0	0	A0	0
3	Average Energy	0	0	0	0	0	14	2,3
4	AGC Gain Word	0	0	1	0	0	15	2,3
5	AGC Slew Rate Word	0	0	0	0	0	95	0,1
6	Tone 1 Frequency	0	0	1	0	0	21	2,3
7	Tone 2 Frequency	0	0	1	0	0	22	2,3
8	Tone 1 Transmit Output Level	0	0	0	0	0	22	2,3
9	Tone 2 Transmit Output Level	0	0	0	0	0	23	2,3
10	Transmit Output Level/Scaling	0	0	0	0	0	21	2,3
11	Equalizer Tap Coefficients	0	1	1	0	1	50 - 7F	0,1,2,3
12	Rotated Equalizer Output, Eye Pattern	0	1	1	0	0	17	0,1,2,3
13	Decision Points, Ideal	0	1	0	0	0	17	0,1,2,3
14	Error Vector	0	1	1	0	0	1D	0,1,2,3
15	Rotation Angle	0	1	1	0	0	8C	0,1
16	Frequency Correction	0	1	1	0	0	18	2,3
17	Eye Quality Monitor (EQM), Hard Decision	0	1	1	0	0	0D	2,3
18	Eye Quality Monitor (EQM), TCM Min. Metric[3]	0	1	1	0	0	B8	0,1
19	RLSD Turn-on Threshold	0	0	1	0	0	37	2,3
20	RLSD Turn-off Threshold	0	0	1	0	0	B7	0,1
21	Receiver Sensitivity, MAXG	0	0	1	0	0	24	2,3
29	Minimum On Time (DTMF)	0	0	1	0	0	1F	2,3
30	Minimum Off Time (DTMF)	0	0	0	0	0	1F	2,3
31	Minimum Cycle Time (DTMF)	0	0	0	0	0	9F	0,1
32	Maximum Dropout Time (DTMF)	0	0	1	0	0	9F	0,1
33	Maximum Speech Energy (DTMF)	0	0	1	0	0	1E	2,3
34	Frequency Deviation, Low Group (DTMF)	0	0	0	0	0	1D	2,3
35	Frequency Deviation, High Group (DTMF)	0	0	1	0	0	1D	2,3
36	Negative Twist Control (DTMF)	0	0	0	0	0	1E	2,3
37	Positive Twist Control (DTMF)	0	0	0	0	0	9E	0,1
38	Maximum Energy Hit Time (DTMF)	0	0	1	0	0	A3	0,1
39	Number of Additional Flags, NFLAG (HDLC)	0	0	1	0	0	85	0,1
40	Transmitter Rate Sequence Pattern[3]	0	0	0	0	0	6B	2,3
41	Receiver Rate Sequence Pattern[3]	0	0	1	0	0	9A	0,1
42	FR1 Tone Detector Coefficients	0	0	1	0	0	25-2A	2,3
	FR1 Tone Detector Coefficients	0	0	1	0	0	A5-AA	0,1
43	FR2 Tone Detector Coefficients	0	0	1	0	0	2B-30	2,3
	FR2 Tone Detector Coefficients	0	0	1	0	0	AB-B0	0,1
44	FR3 Tone Detector Coefficients	0	0	1	0	0	31-36	2,3
	FR3 Tone Detector Coefficients	0	0	1	0	0	B1-B6	0,1
47	Tone Detector Threshold	0	0	0	0	0	9D	0,1
48	Maximum Samples per Ring Frequency Period	0	0	0	0	0	53	2,3
49	Minimum Samples per Ring Frequency Period	0	0	0	0	0	52	2,3
50	Sleep Mode Enable	0	0	0	1	0	3E	0,1
51	V.23 Receive Compromise Equalizer Taps	0	0	1	0	1	18-4F	2,3
52	V.23 RTS to CTS Turn Off Transition Time	0	0	1	0	1	DD	0,1
53	V.23 RTS to CTS Turn On Transition Time	0	0	1	0	1	DE	0,1
54	V.23 Number of Bits (Caller ID only)	0	0	1	0	1	EB	0,1

Table 4-1. Modem DSP RAM Access Codes (Cont'd)

No. [1, 2]	Function	SBRAMx	BRx	CRx	IOx	AREXx	ADDx	Read Reg. No.[4]
55	Voice/Audio VOX Turn-On Threshold	0	0	1	0	0	57	2,3
56	Voice/Audio VOX Turn-Off Threshold	0	0	1	0	0	D7	0,1
57	Voice/Audio VOX A0 Filter Coefficient	0	0	1	0	0	D6	0,1
58	Voice/Audio VOX A1 Filter Coefficient	0	0	1	0	0	56	2,3
59	Voice/Audio Energy AGC Reference Level	0	0	0	0	0	9A	0,1
60	Voice/Audio Energy AGC Slew Rate	0	0	1	0	0	1A	2,3
61	Voice/Audio Energy AGC Gain Adaptation Threshold	0	0	0	0	0	1A	2,3
62	Voice/Audio Energy AGC Maximum Gain	0	0	0	0	0	9B	0,1
63	Voice/Audio Energy AGC Gain Word	0	0	1	0	0	1B	2,3
64	Voice/Audio Classifier AGC Maximum Gain	0	0	1	0	0	0B	2,3
65	Voice/Audio Classifier AGC Reference Level	0	0	1	0	0	84	0,1
66	Voice Codec Mode Data Transfer Interrupt Interval	0	0	1	0	0	03	2,3
67	Voice/Audio Decoder Volume Range	0	0	1	0	0	85	0,1
68	Room Monitor Volume Control	0	0	0	1	0	1C	0,1
69	Sample Rate AGC Filter Coefficient A0	0	0	0	0	0	C5	0,1
70	Sample Rate AGC Filter Coefficient A1	0	0	1	0	0	C6	0,1
71	Sample Rate AGC Switch AGCSW1	0	0	1	0	0	C7	0,1
72	Sample Rate AGC Energy Reference Level	0	0	1	0	0	C5	0,1
73	Sample Rate AGC Slew Rate, Rise	0	0	0	0	0	C9	0,1
74	Sample Rate AGC Slew Rate, Fall	0	0	0	0	0	C7	0,1
75	Sample Rate AGC Maximum Gain	0	0	0	0	0	C8	0,1
76	Sample Rate AGC Maximum Attenuation	0	0	1	0	0	C8	0,1
77	Sample Rate AGC Gain Word	0	0	0	0	0	C4	0,1
78	Sample Rate VOX Switch VOXSW1	0	0	1	0	0	CA	0,1
79	Sample Rate VOX Filter Coefficient A0	0	0	0	0	0	CA	0,1
80	Sample Rate VOX Filter Coefficient A1	0	0	1	0	0	CB	0,1
81	Sample Rate VOX Switch VOXSW2	0	0	1	0	0	C9	0,1
82	Sample Rate VOX Turn-On Threshold	0	0	0	0	0	CC	0,1
83	Sample Rate VOX Turn-Off Threshold	0	0	1	0	0	CC	0,1

Notes:

1. Parameter numbers refer to corresponding numbers in Section 4.
2. For all accesses, DRx = 0.
3. FM214 models only.
4. Read Reg. No. column only shows the registers to use when x = 1. When x = 2, the Read Reg. No. column value must be added to 10h.

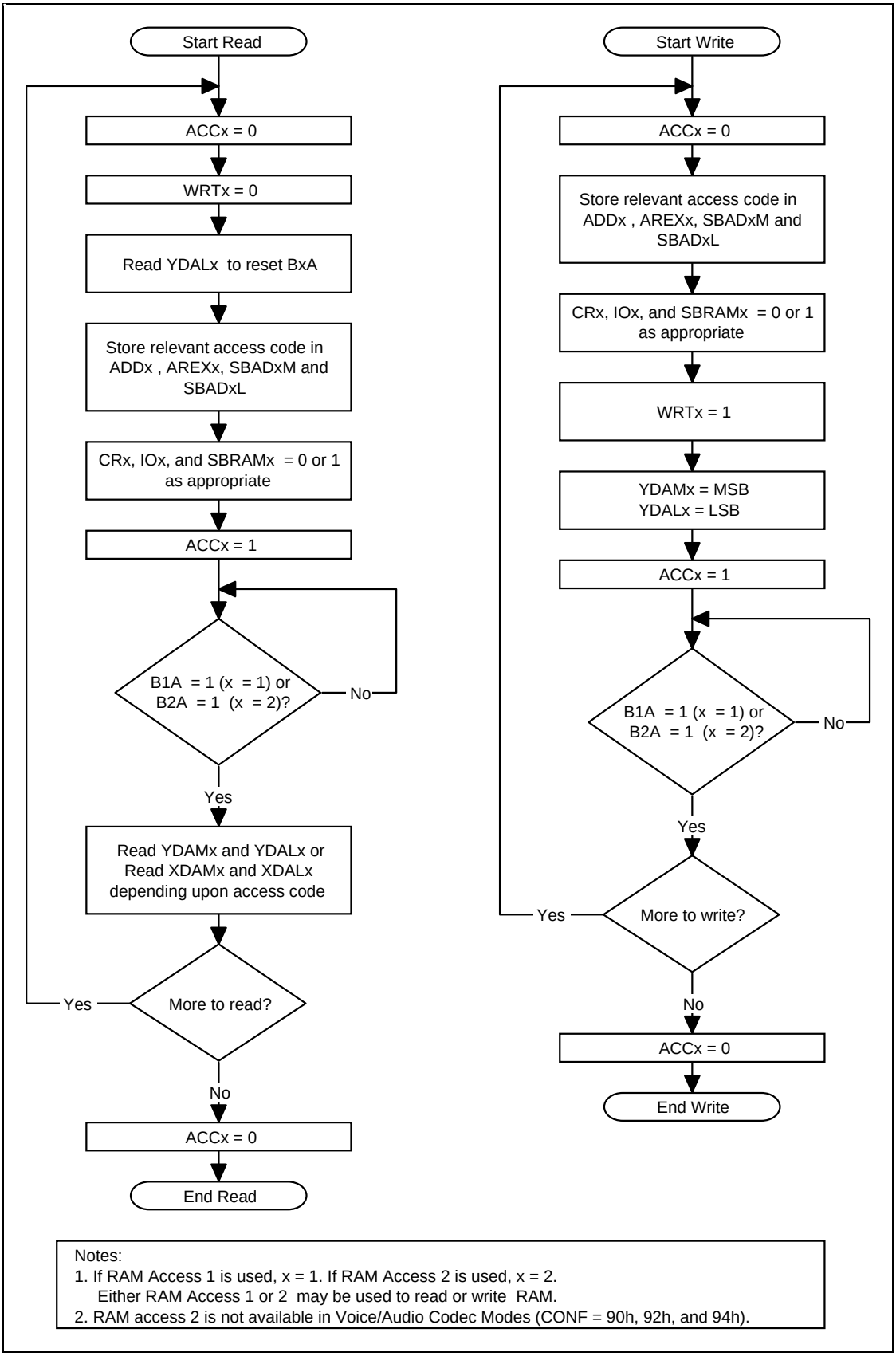


Figure 4-1. Host Flowchart - RAM Data Read and RAM Data Write

4.2 DIAGNOSTIC DATA SCALING

No. 1a Received Signal Sample (Pre-AGC) = A/D Sample Word

Format: 16 bits, signed, twos complement

Equation: V_{INT} (Volts)= [(A/D Sample Word x V_{MAX}/32768) + 2.5V

Where: V_{MAX} = 1.6V

V_{EXT} is the input to the IA

V_{INT} is the output of the IA and input to the DSP.

No. 1b Received Signal Sample (Post-AGC) = A/D Sample Word

Format: 16 bits, signed, twos complement

Equation: V_{INT} (Volts)= [(A/D Sample Word x V_{MAX}/32768) + 2.5V

VEXT = V_{INT}/LOG_{10}^{-1} [AGC Gain (dB)/20]

Where: V_{MAX} = 1.6V

V_{EXT} is the input to the IA

V_{INT} is the output of the IA and input to the DSP.

No. 2 Received Signal Sample - 8-bit Audio Mode (Post-AGC) = A/D Sample Word

Format: 8 bits, signed, twos complement

Equation: V_{INT} (Volts)= [(A/D Sample Word)8] x (1.6/128) + 2.5V

$V_{EXT} = V_{INT}/LOG_{10}^{-1}$ [AGC Gain (dB)/20]

Where: V_{EXT} is the input to the IA

V_{INT} is the output of the IA and input to the DSP.

No. 3 Average Power

Format: 16-bits, positive, twos complement

Equation: Post-AGC Average Power (dBm) = 10 Log [(Average Power Word)h/889h]

Pre-AGC Average Power (dBm) = Post-AGC Avg. Power in dBm - AGC gain in dB

Typical Value: 0889h

No. 4 AGC Gain

Format: 16-bits, unsigned

Equation : AGC Gain (dB) = 50 [1 - (AGC Gain Word)h/32768]

No. 5 AGC Slew Rate

Format: 16 bits, positive, twos complement

The AGC Slew Rate can be approximated by the following equation.

Equation: AGC Slew Rate = [19968/(Sample rate x AGC gain fall time constant in seconds)]h

Note: AGC gain tracks the input signal with an exponential function with respect to time, and its fall time is approximately 5 times faster than its rise time. The above equation was determined based upon a 40 dB change in input signal.

No. 6 Tone 1 Frequency
No. 7 Tone 2 Frequency

Format: 16 bits, unsigned

Equation: N = 6.8267 x Frequency (in Hz) for 9600 Hz sampling rate

N = 8.192 x Frequency (in Hz) for 8000 Hz sampling rate

Convert N to hexadecimal then store in RAM.

No. 8 Tone 1 Transmit Output Level
No. 9 Tone 2 Transmit Output Level

Format: 16-bits, positive, twos complement

Calculate the transmit output level (power) of each tone independently by using the equation for Transmit Output Level (No. 10).

Total power transmitted in tone configuration is the result of both tone 1 power and tone 2 power.

No. 10 Transmit Output Level (Ps)

Format: 16-bits, positive, twos complement

Equation: Transmit Output Level = $18426\ [10^{(Po/20)}]$ or $18426\ [10^{(P_S/20)}]$

Where: Po = output power in dBm with a 600 ohm load termination.
Ps = output power in dBm with a series 600 ohm resistor into a 600 ohm load (Ps = Po – 6).

Convert Transmit Output Level to hexadecimal and store in RAM.

Default Value: 7FFFh

Note: For the modem interface circuits shown in Figure 14-1, the maximum transmit output level (Ps) is -1 dBm at TXA.

No. 11 Equalizer Tap Coefficients

Access codes 50h through 7Fh represent 48 complex taps.

The equalizer tap coefficients can be useful for restoring modem operation after loss of equalization without requesting a training sequence from the transmitter. Since the equalizer tap coefficients are complex numbers, they require two write operations per tap, one for the real part and one for the imaginary part. When writing the imaginary part, the access codes 50h through 7Fh must be changed to D0h through FFh. When writing the real part, or when reading the complex number, the access codes 50h through 7Fh are correct.

Format: 16 bits, signed, twos complement, real

16 bits, signed, twos complement, imaginary

No. 12 Rotated Equalizer Output (Eye Pattern)
No. 13 Decision Points (Ideal)

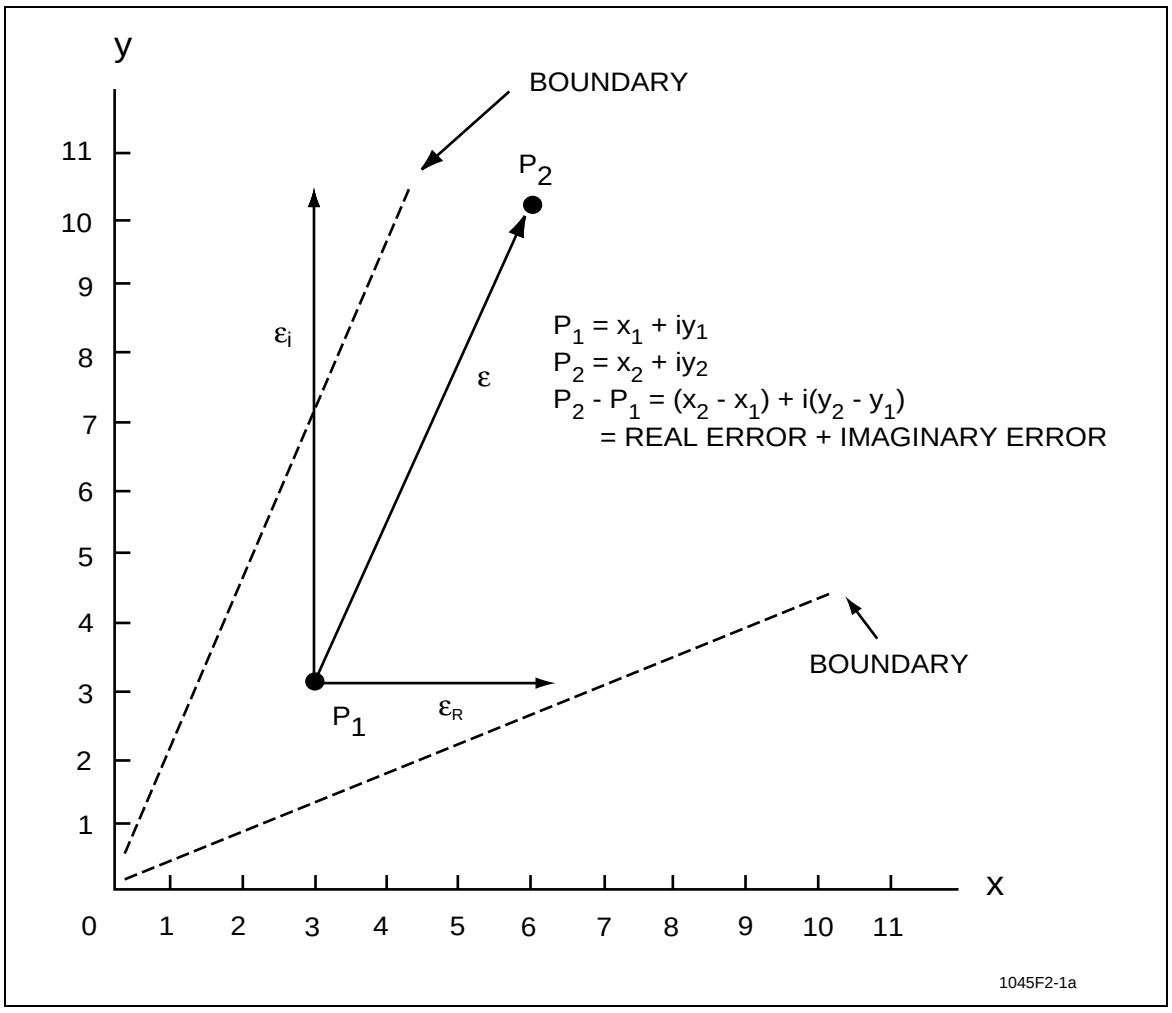
Format: 16 bits, signed, twos complement, real

16 bits, signed, twos complement, imaginary

No. 14 Error Vector

Represents the difference between the received point (P2) and the nearest ideal point (P1).

Format: 16 bits, signed, twos complement, real
16 bits, signed, twos complement, imaginary



Error Vector Maximum Values

Configuration	Bit Rate	Registers 3 and 2 Real Error (Re)	Registers 1 and 0 Imaginary Error (Im)	Magnitude $\sqrt{(Re^2 + Im^2)}$
V.29	9600	<0C00h	<0C00h	<0E66h
V.29	9200	<2400h	<2400h	<1AD4h
V.29	4800	<1C00h	<1C00h	<1C00h
V.27 ter	4800	<1C00h	<1C00h	<1C00h
V.27 ter	2400	<1C00h	<1C00h	<1C00h

No. 15 Rotation Angle

Represents instantaneous correction for phase and frequency errors.

Format: 16-bits, twos complement

Equation: Rotation Angle (degrees) = [(Rotation Angle Word)h/10000h] x 180

No. 16 Frequency Correction

Represents component of rotation angle caused by frequency error.

Format: 16 bits, twos complement

Equation: Frequency Correction (Hz) = [(Freq. Correction Word)h/10000h] x Baud in Hz

Range: FC00h to 0400h representing ±37.5 Hz

No. 17 Eye Quality Monitor (EQM) Hard Decision

Equals the filtered squared magnitude of the error vector. Proportionality to bit error rate is determined by particular application. Stabilizes in approximately 700 baud times from RLSD# going active.

Format: 16 bits, positive, twos complement

No. 18 Eye Quality Monitor (EQM) TCM Minimum Metric (FM214 models)

Equals the filtered squared magnitude of the path length for TCM modes. Stabilizes in approximately 1200 baud times from RLSD# going active.

Format: 16 bits, positive, twos complement

No. 19 RLSD Turn-On Threshold
No. 20 RLSD Turn-Off Threshold
No. 21 Receiver Sensitivity (MAXG)

Three parameters can be programmed by the host to control the RLSD turn-on and turn-off thresholds: (1) Post-AGC Turn-on Threshold, (2) Post-AGC Turn-off Threshold, and (3) Receiver Sensitivity (MAXG) - AGC Gain Word Limit.

Format: 16 bits, positive, twos complement

Equation: RLSD Turn-on Threshold = 2185 (10 (TON + 50 – [(MAXG/64)0.098])/10)

RLSD Turn-off Threshold = 2185 (10(TOFF +50 – [(MAXG/64)0.098])/10)

Receiver Sensitivity (MAXG) = 655.36 [50 - Gain Limit (dB)]

Where: TON is the turn-on threshold in dBm.

TOFF is the turn-off threshold in dBm.

MAXG is programmable in RAM and defaults to 0FC0h (4032).

No. 29 Minimum On-Time (DTMF)

The on-time is defined as the minimum period of time of the DTMF signal beginning when the signal is detected and ending when the energy is below the turn-off threshold. The on-time parameter cannot be set below 29.6 ms (0000h). The default on-time parameter is set for 40.0 ±1 ms. The on-time will vary with signal level. To increase or decrease the on-time parameter value, convert the increase/decrease into hex and add/subtract to/from the current value. (See Section 13.)

Format: 16-bits, positive, twos complement

Equation: Minimum On-Time ± [(Increase/Decrease in ms)9.6]h

Range: 0 to 7FFFh

Default Value: 007Ah (CONF = 21h); 005Fh (CONF = 9xh)

No. 30 Minimum Off-Time (DTMF)

The minimum off-time is defined as the minimum period of time of the DTMF signal beginning when the energy falls below the turn-off threshold and ending when a gain hit is detected. The off-time parameter is equal to the desired minimum off-time minus the drop out time. The default off-time is set for 40.0 ± 1 ms with a default drop out time parameter of 5.0 ms. To increase or decrease the off-time parameter value, convert the increase/decrease into hex and add/subtract to/from the current value. (See Section 13.)

Format: 16-bits, positive, twos complement

Equation: Minimum Off-Time ± [(Increase/Decrease in ms)9.6]h (drop out time equal to 5.0 ms).

Range: 0 to 7FFFh

Default Value: 013Eh (CONF = 21h); 010Fh (CONF = 9xh)

No. 31 Minimum Cycle-Time (DTMF)

The minimum cycle-time is defined as the minimum period of the DTMF signal beginning when the signal is detected and ending when the next signal begins. The cycle-time parameter is equal to the desired minimum cycle-time minus the drop out time. The default cycle-time parameter is set for 93.0 ±1 ms with a default drop out time parameter of 5.0 ms. To increase or decrease the cycle-time parameter value, convert the increase/decrease into hex and add/subtract to/from the current value. (See Section 13.)

Format: 16-bits, positive, twos complement

Equation: Minimum Cycle-Time ± [(Increase/Decrease in ms)9.6]h (dropout time equal to 5.0 ms).

Range: 0 to 7FFFh

Default Value: 022Ah (CONF = 21h); 01C7h (CONF = 9xh)

No. 32 Minimum Dropout-Time (DTMF)

The minimum dropout time is defined as the maximum period of the DTMF signal beginning when the signal energy drops below the turn-off threshold and ending when the signal energy returns that is considered to be part of the on-time. The default dropout-time parameter is set to 5.0 ms. (See Section 13.)

Format: 16-bits, positive, twos complement

Equation: [(Desired Time in ms)9.6]h

Range: 0 to 7FFFh

Default Value: 0029h (CONF = 21h); 0022h (CONF = 9xh)

No. 33 Maximum Speech Energy (DTMF)

This parameter specifies the maximum relative speech energy that may be detected and still receive DTMF signals. The speech energy is measured in the frequency region of second or third harmonics of the DTMF tones. To disable the speech energy detector, set this parameter to its full scale positive value 7FFFh. Decreasing the value of this parameter may degrade signal-to-noise ratio (SNR) performance, but may reduce false settings of status bit EDET due to speech signals. To increase or decrease the maximum speech energy parameter value, convert the increase/decrease into hex and add/subtract to/from the current value. (See Section 13.)

Format: 16-bits, positive, twos complement

Equation: Maximum Speech Energy ± (Increase/Decrease)h

Range: 0 to 7FFFh

Default Value: 0519h (CONF = 21h); not available (CONF = 9xh)

No. 34 Frequency Deviation, Low Group (DTMF)

This parameter controls the acceptable frequency range for the low group DTMF tones. Increasing the value of this parameter increases the frequency range. The frequency range will vary from one DTMF symbol to another. To increase or decrease the parameter value, convert the increase/decrease into hex and add/subtract to/from the current value. (See Section 13.)

Format: 16-bits, positive, twos complement

Equation: Frequency Deviation ±(Increase/Decrease)h

Range: 0 to 7FFFh

Default Value: 034Ah (CONF = 21h); 0288h (CONF = 9xh)

No. 35 Frequency Deviation, High Group (DTMF)

This parameter controls the acceptable frequency range for the high group DTMF tones. Increasing the value of this parameter increases the frequency range. The frequency range will vary from one DTMF symbol to another. To increase or decrease the parameter value, convert the increase/decrease into hex and add/subtract to/from the current value. (See Section 13.)

Format: 16-bits, positive, twos complement

Equation: Frequency Deviation ±(Increase/Decrease)h

Range: 0 to 7FFFh

Default Value: 0444h (CONF = 21h); 0260h (CONF = 9xh)

No. 36 Negative Twist (DTMF)

This parameter controls the acceptable negative twist for the DTMF signals. Decreasing this parameter increases the acceptable negative twist level. The twist will vary from one DTMF symbol to another. To increase or decrease the parameter value, convert the increase/decrease into hex and add/subtract to/from the default value. (See Section 13.)

Format: 16-bits, positive, twos complement

Equation: Negative Twist ±(Increase/Decrease)h

Range: 0 to 7FFFh

Default Value: 2800h (CONF = 21h); 0C2Eh (CONF = 9xh)

No. 37 Positive Twist (DTMF)

This parameter controls the acceptable positive twist for the DTMF signals. Decreasing this parameter increases the acceptable positive twist level. The twist will vary from one DTMF symbol to another. To increase or decrease the parameter value, convert the increase/decrease into hex and add/subtract to/from the default value. (See Section 13.)

Format: 16-bits, positive, twos complement

Equation: Positive Twist ±(Increase/Decrease)h

Range: 0 to 7FFFh

Default Value: 1420h (CONF = 21h); 3295h (CONF = 9xh)

No. 38 Maximum Energy Hit Time (DTMF)

This parameter is a counter value which represents the number of sample times (the duration) of an allowed energy impulse during the DTMF off-time measurement. A value of 0000h means no gain hits will be tolerated during the off time.

Format: 16-bits, positive, twos complement

Equation: [(Desired Time in ms)(9.6)]h

Range: 0 to 7FFFh

Default Value: 0 (CONF = 21h); 0 (CONF = 9xh)

No. 39 Number of Additional Flags (HDLC)

This parameter controls the number of flags between frames or at the end of the final frame. See Section 5 for more information.

Format: 16-bits, positive, twos complement

Equation: Desired number of flags - 1

Default Value: 0

No. 40 Transmitter Rate Sequence Pattern (FM214 models only)
No. 41 Receiver Rate Sequence Pattern (FM214 models only)

The following rate sequence patterns can be sent and detected by the modem as enabled by the ASPEED bit (see ASPEED description in Table 3-1):

Encoding:

ASPEED	Data Rate	Rate Sequence Pattern
0	V.17, all rates	0111h*
1	14400 bps	0171h*
1	12000 bps	01B1h*
1	9600 bps	01F1h*
1	7200 bps	0331h*

1. * The most significant bit of the rate sequence pattern corresponds to bit 0 in the V.17 rate sequence pattern.

Format: 16-bits, unsigned

No. 42 FR1 Tone Detector Coefficients

See Section 6 for scaling information.

No. 43 FR2 Tone Detector Coefficients

See Section 6 for scaling information.

No. 44 FR3 Tone Detector Coefficients

See Section 6 for scaling information.

No. 47 Tone Detector Threshold

This parameter represents the threshold value (1/8 by default) to compare with the output of the energy average in the tone detector. This parameter is used for all 3 filters.

Format: 16 bits, twos complement, positive value

Equation: 215 (1 - Threshold desired) h

Default Value: 7000h

No. 48 Maximum Samples per Ring Frequency Period (RDMAXP)

This parameter determines the maximum period on RINGD (GPI7) that will be indicated on RI. The default value of 71.4 ms corresponds to the minimum ring frequency of 14 Hz. This allows proper detection of frequencies as low as 15 Hz.

Format: 16 bits, twos complement, positive value

Equation: Maximum period samples = Sampling frequency (samples/sec)/minimum ring frequency (Hz)

Convert to hex and store in RAM.

Default Value: 023Bh (71.4 ms) for 8000 Hz sample rate

No. 49 Minimum Samples per Ring Frequency Period (RDMINP)

This parameter determines the minimum period on RINGD (GPI7) that will be indicated on RI. The default value of 13.9 ms corresponds to the maximum ring frequency of 72 Hz. This allows proper detection of frequencies as high as 68 Hz.

Format: 16 bits, twos complement, positive value

Equation: Minimum period samples = Sampling frequency (samples/sec)/maximum ring frequency (Hz)

Convert to hex and store in RAM.

Default Value: 006Fh (13.9 ms) for 8000 Hz sample rate

No. 50 Sleep Mode

Writing a 0 to this register puts the modem DSP into the Sleep Mode and the PIA/SIA into reset mode.

The modem will go through the power-on sequence and resume normal operation with default values in response to a hardware power-on reset, or a write to the scratchpad interface by the host.

No. 51 V.23 Receive Compromise Equalizer Taps

Access codes 18h through 4Fh represent 56 taps.

Format: 16 bits, signed, twos complement, real

Default Values: The default values of the Receive Compromise Equalizer provide 50% compensation (both amplitude and group delay) of a 1040 Tellindus line (which approximates a CCITT 1040/1025 line). Access code 4Fh is used for the first equalizer tap, and Access code 18h is used for the last equalizer tap.

No. 52 V.23 RTS to CTS Turn Off Transition Time

This parameter controls the minimum RTS to CTS turn off transition time.

Format: 16 bits, positive, twos complement

Equation: [Desired time in tenths of milliseconds]h

Default Value: 0014h (2 ms)

No. 53 V.23 RTS to CTS Turn On Transition Time

This parameter controls the minimum RTS to CTS turn on transition time.

Format: 16 bits, positive, twos complement

Equation: [Desired time in tenths of milliseconds]h

Default Value: 0064h (10 ms)

No. 54 V.23 Number of Bits (Caller ID only)

This parameter selects the number of bits per character for Caller ID mode, including one start bit and one stop bit. Caller ID mode does not use a parity bit. Characters from 5 to 8 data bits (7 to 10 bits total) are supported. In parallel mode, the start and stop bits will be stripped from received data before it is placed in DBUFF.

Format: 16 bits, positive, twos complement

Equation: [Desired number of bits per received character]h

Default Value: 000Ah (8 data bits, 1 start bit, 1 stop bit, no parity - standard for Caller ID)

No. 55 Voice/Audio VOX Turn-On Threshold

When status bit VOX (17:3) is reset and the average energy of the message being encoded exceeds the VOX turn-on threshold, the modem sets the VOX bit to indicate speech is being detected. The VOX turn-on threshold should be less than the AGC gain adaptation threshold when the Energy AGC is not disabled and bit DCVOX is zero.

Format: 16 bits, signed, twos complement

Equation: $Level = (10^{[x/20]})(23315)$

Where: x = VOX turn-on threshold in dBm.

Default Value: 0088h (-44.68 dBm)

No. 56 Voice/Audio VOX Turn-Off Threshold

If status bit VOX (17:3) is set, the modem resets VOX when the average energy of the message being encoded falls below the VOX turn-off threshold for a minimum period of time equal to the time constant of the VOX energy averaging filter. The time constant is specified by the VOX energy averaging filter coefficient A0 (see No. 57).

Format: 16 bits, signed, twos complement

Equation: $Level = (10^{[x/20]})(23315)$

Where: x = VOX turn-off threshold in dBm.

Default Value: 0044h (-50.70 dBm)

No. 57 Voice/Audio VOX A0 Filter Coefficient

The VOX energy averaging filter coefficient A0 is a function of the filter time constant.

Format: 16 bits, signed, twos complement

Equation: A0 = 917.5/x

Where: x = VOX turn-off time constant in seconds.

Default Value: 03A8h (0.98 sec.)

No. 58 Voice/Audio VOX A1 Filter Coefficient

The VOX energy averaging filter coefficient A1 is a function of the filter coefficient A0.

Format: 16 bits, signed, twos complement

Equation: A1 = 7FFFh - A0

Where: A0 = VOX energy averaging filter coefficient.

Default Value: 7C57h

No. 59 Voice/Audio Energy AGC Reference Level

Energy reference level for the Energy AGC. The default value is loaded each time the modem is configured to Voice Codec Mode (CONF = 90h or 98h), or Audio Codec Mode (CONF = 92h or 94h).

Format: 16 bits, signed, twos complement

Equation: $Level = (10^{[x/20]})(23315)$

Where: x = AGC energy reference level in dBm.

Default Value: 0380h (-28.31 dBm)

No. 60 Voice/Audio Energy AGC Slew Rate

Slew rate for the Energy AGC. The slew rate controls how rapidly the AGC will adapt the average message energy to the AGC reference level. Larger/smaller slew rate values correspond to faster/slower average energy convergence to AGC reference level. The default value is loaded each time the modem is configured to Voice Codec Mode (CONF = 90h or 98h) or Audio Codec Mode (CONF = 92h or 94h).

Format: 16 bits, signed, twos complement

Default Value: 3C00h

No. 61 Voice/Audio Energy AGC Gain Adaptation Threshold

If the energy of the message being encoded exceeds the AGC gain adaptation threshold then the encoder AGC gain will be increased/decreased when the average energy is less/greater than the AGC reference level. The AGC gain adaptation threshold should be greater than the Voice Mode VOX turn-on threshold whenever the Energy AGC is not disabled and bit DCVOX is zero. The default value is loaded each time the modem is configured to Voice Codec Mode (CONF = 90h or 98h) or Audio Codec Mode (CONF = 92h or 94h).

Format: 16 bits, signed, twos complement

Equation: $Threshold = (10^{[x/20]})(23315)$

Where: x = AGC gain adaptation threshold in dBm.

Default Value: 00A3h (-43.11 dBm)

No. 62 Voice/Audio Energy AGC Maximum Gain Word

Maximum gain for the Energy AGC. The default value is loaded each time the modem is configured to Voice Codec Modes (CONF = 90h or 98h) or Audio Codec Mode (CONF = 92h or 94h).

Format: 16 bits, signed, twos complement

Equation: Maximum Gain = [25 - x](655.36)

Where: x = Maximum gain in dB

Range: 0 dB < x < 25 dB

Default Value: 1C00h (14.0625 dB)

No. 63 Voice/Audio Energy AGC Gain Word

Gain word for the Energy AGC.

Format: 16 bits, signed, twos complement

Equation: Gain in dB = 25 - [(Voice Mode AGC Gain)/655.36]

No. 64 Voice/Audio Classifier AGC Maximum Gain

Maximum gain for the Classifier AGC. The default value is loaded each time the modem is configured to Voice Codec Mode (CONF = 90h or 98h) or Audio Codec Mode (CONF = 92h or 94h).

Format: 16 bits, signed, twos complement

Equation: Maximum Gain = (819.2)(x)

Where: x = Maximum gain in dB

Default Value: 6000h (30 dB)

No. 65 Voice/Audio Classifier AGC Reference Level

Energy reference level for the Classifier AGC. The default value is loaded each time the modem is configured to Voice Codec Mode (CONF = 90h or 98h) or Audio Codec Mode (CONF = 92h or 94h).

Format: 16 bits, signed, twos complement

Equation: Level = (256)(x) - 757

Where: x = AGC reference level in dBm

Default Value: DC00h (-33.04 dBm)

No. 66 Voice Codec Mode Data Transfer Interrupt Interval

The data transfer interrupt interval specifies the number of sample periods between modem generated interrupts within data block transfers. Following an interrupt, the host reads 8-bits of data from DBUFF (see Table 3-1) when the encoder is enabled (see CDEN bit in Table 3-1) or writes 8-bits of data to DBUFF when the decoder is enabled (see DCDEN bit in Table 3-1).

Format: 16 bits, signed, twos complement

Equation: Value = (number of sample periods) - 1

Range: (See Section 8.1 and 8.2)

Default Value: 0002h (representing 3 sample periods between interrupts)

No. 67 Voice/Audio Decoder Volume Range

The volume control provides a 2 dB loss to the output each time control bit VOLDWN (OE:5) is set and the decoder is enabled. The voice/audio decoder volume range parameter limits the maximum loss.

Format: 16 bits, positive, two's complement

Equation: $(10^{[(x+1)/20]})(32768)$

Where: x = lower range limit in dB

Range: 0004h - 7FFFh

Default Value: 0170h (-40 dB)

No. 68 Room Monitor Volume Control

The amplitude of the PIA DAC signal in the Room Monitor Mode can be adjusted. An increase in the value written to the modem shifts the value sent to the PIA DAC left by one, thereby doubling its amplitude.

Format: 16 bits, unsigned

Equation: dB gain = 6 * x

Range: 0 < x < 7FFFh

Default Value: 0

No. 69 Sample Rate AGC Filter Coefficient A0

The Sample Rate AGC average magnitude filter coefficient A0 is a function of the filter time constant.

Format: 16-bits, signed, twos complement

Equation: A0 = 4.1/x

Where x = filter time constant in seconds.

Default Value: 7FFFh (125 usec)

No. 70 Sample Rate AGC Filter Coefficient A1

The Sample Rate AGC average magnitude filter coefficient A1 is a function of filter coefficient A0.

Format: 16-bits, signed, twos complement

Equation: A1 = 7FFFh - A0

Where A0 is the Sample Rate AGC Filter Coefficient

Default Value: 0000h

No. 71 Sample Rate AGC Switch AGCSW1

The Sample Rate AGC Switch AGCSW1 enables/disables average magnitude squared operation.

Format: 16-bits, signed, twos complement

Equation: AGCSW1 = 0000h, average magnitude squared enabled

AGCSW1 = 7FFFh, average magnitude squared disabled

Default Value: 0000h

No. 72 Sample Rate AGC Energy Reference Level

Energy reference level for the Sample Rate AGC.

Format: 16-bits, signed, twos complement

Equation: Level = $(10^{[x/20]})(23315)$

Where x = AGC energy reference level in dBm

Default Value: 0380h (-28.31 dBm)

No. 73 Sample Rate AGC Slew Rate, Rise

This Sample Rate AGC Slew Rate controls how rapidly the AGC will adapt the input signal average magnitude energy to the reference level during rise time. Larger/smaller slew rate values correspond to faster/slower convergence periods.

Format: 16-bits, signed, twos complement

Default Value: 0064h

No. 74 Sample Rate AGC Slew Rate, Fall

This Sample Rate AGC Slew Rate controls how rapidly the AGC will adapt the input signal average magnitude energy to the reference level during fall time. Larger/smaller slew rate values correspond to faster/slower convergence periods.

Format: 16-bits, signed, twos complement

Default Value: 03E8h

No. 75 Sample Rate AGC Maximum Gain

Maximum gain for the Sample Rate AGC.

Format: 16-bits, signed, twos complement

Equation: Maximum Gain = [25 - x](655.36)

Where x = Maximum Gain in dB

Range: 0 dB < x < 25 dB

Default Value: 0000h (25 dB)

No. 76 Sample Rate AGC Maximum Attenuation

Maximum attenuation for the Sample Rate AGC.

Format: 16-bits, signed, twos complement

Equation: Maximum Attenuation = [25 - x](655.36)

Where x = Maximum Attenuation in dB

Range: -25 dB < x < 0 dB

Default Value: 599Ah (-10 dB)

No. 77 Sample Rate AGC Gain Word

Gain word for the Sample Rate AGC.

Format: 16-bit, signed, twos complement

Equation: Gain in dB = 25 - [(AGC Gain Word)/655.36]

No. 78 Sample Rate VOX Switch VOXSW1

The Sample Rate VOX Switch VOXSW1 enables/disables applying Sample Rate AGC gain prior to VOX operation.

Format: 16-bits, signed, twos complement

Equation: VOXSW1 = 0000h, applied AGC gain enabled

VOXSW1 = 7FFFh, applied AGC gain disabled

Default Value: 7FFFh

No. 79 Sample Rate VOX Filter Coefficient A0

The Sample Rate VOX average magnitude filter coefficient A0 is a function of the filter time constant.

Format: 16-bits, signed, twos complement

Equation: A0 = 4.1/x

Where x = filter time constant in seconds.

Default Value: 7FFFh (125 usec)

No. 80 Sample Rate VOX Filter Coefficient A1

The Sample Rate VOX average magnitude filter coefficient A1 is a function of filter coefficient A0.

Format: 16-bits, signed, twos complement

Equation: A1 = 7FFFh - A0

Where A0 is the Sample Rate VOX Filter Coefficient

Default Value: 0000h

No. 81 Sample Rate VOX Switch VOXSW2

The Sample Rate VOX Switch VOXSW2 enables/disables average magnitude squared operation.

Format: 16-bits, signed, twos complement

Equation: VOXSW2 = 0000h, average magnitude squared enabled

VOXSW2 = 7FFFh, average magnitude squared disabled

Default Value: 7FFFh

No. 82 Sample Rate VOX Turn-On Threshold

When status bit VOXHI (19:3) is a 0 and the average magnitude energy is greater than the VOX Turn-On Threshold, the modem sets bit VOXHI else the modem resets VOXHI.

Format: 16-bits, signed, twos complement

Equation: Level = $(10^{[x/20]})(32768)$

Where x = VOX Turn-On Threshold in dB

Default: 0088h (-47.6 dB)

No. 83 Sample Rate VOX Turn-Off Threshold

When status bit VOXLO (19:4) is a 0 and the average magnitude energy is greater than the VOX Turn-Off Threshold, the modem sets bit VOXLO else the modem resets VOXLO.

Format: 16-bits, signed, twos complement

Equation: Level = $(10^{[x/20]})(32768)$

Where x = VOX Turn-Off Threshold in dB

Default: 0044h (-53.7 dB)

4.3 INTEGRATED ANALOG CONTROL REGISTERS

The modem has an internal primary integrated analog (PIA) codec and an internal secondary integrated analog (SIA) codec that provide gain, filtering, internal analog switching, and an internally sourced microphone bias output. The IA is controlled by three control registers and an address register located in internal RAM space which are accessed via the modem interface memory. These registers provide individual controls for the IA's inputs, outputs, gain, and switching. The registers are located in internal RAM. The LSB of each 16-bit address contents is used to control the PIA. The MSB of each 16-bit address contents is used to control the SIA. Figure 4-2 shows the PIA/SIA signal flow control.

Register	SBRAMx	BRx	CRx	IOx	AREXx	ADDx	PIA Reg*	SIA Reg*
IACR1	0	0	0	0	0	D0	0	1
IACR2	0	0	0	0	0	D4	0	1
IACR3	0	0	0	0	0	D5	0	1
IAADD	0	0	0	0	0	CE	0,1	0,1
*Registers to use when x=1. When x=2, add 10h.								

For changes made to IACR1/IACR2/IACR3 to be effective the host must write to IAADD with values 0002h/0006h/00007h. Configuration default values are shown below.

	DEFAULT VALUE		
CONFIGURATION	IACR1	IACR2	IACR3
V.17/V.33	1D9Eh	0008h	0000h
V.29	1D9Eh	0008h	0000h
V.27ter	1D9Eh	0008h	0000h
V.21 Ch. 2	1D9Eh	0008h	0000h
V.23/Caller ID	1D9Eh	0008h	0000h
Tone Transmit/Detect	1D9Eh	0008h	0000h
Voice/Audio Codec	0D16h	0008h	0000h
Speakerphone	0D16h	0008h	0000h

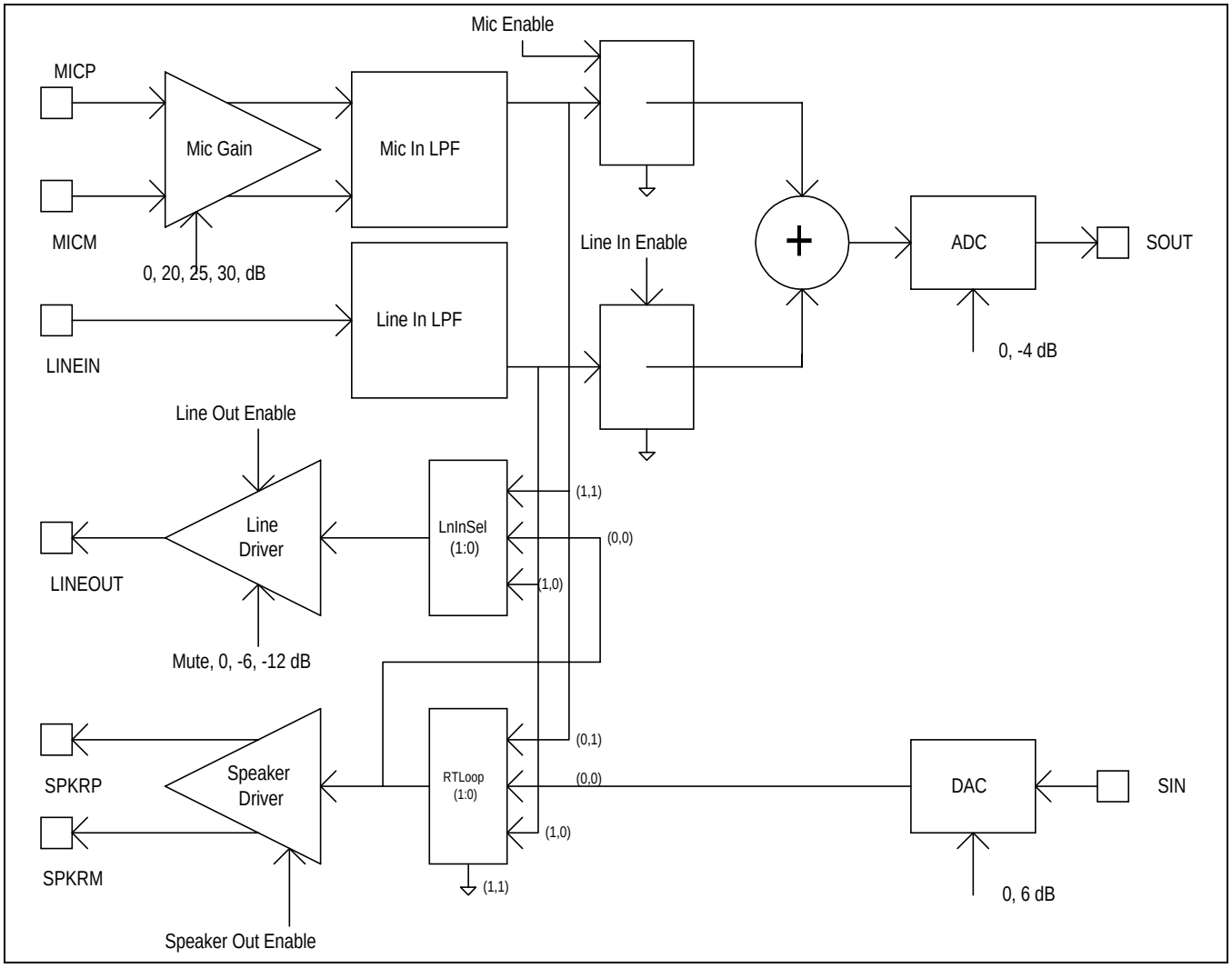


Figure 4-2. PIA/SIA Signal Flow Control

4.3.1 IACR1 IA Control Register 1

The bits in IA Control Register IACR1 control DAC gain, Mic gain, LINEOUT enable, SPKRP and SPKRM enable, ADC gain, LINEIN enable, and MICP and MICM enable.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DAC Gain	Mic Gain		LINEOUT Enable	SPKR(P/M) Enable	ADC Gain	LINEIN Enable	MIC(M/P) Enable

Bit 7 **DAC Gain Enable.**
When control bit DAC Gain is a 1, the modem transmit output level is increased by 6 dB in the DAC. When control bit DAC Gain is a 0, the transmit output level is not increased in the DAC (0 dB).

Bits 6-5 **Mic Gain.**
Control bits Mic Gain select one of four amplifications for the MIC(P/N) pins.
00 = 0 dB
01 = 20 dB
10 = 25 dB
11 = 30 dB

Bit 4 **LINEOUT Enable.**
When control bit LINEOUT Enable is a 1, the IA line output driver is enabled. When LINEOUT Enable is a 0 the IA line output driver is tristated.

Bit 3 **SPKR(P/M) Enable.**
When control bit SPKR(P/M) is a 1, the IA speaker output driver is enabled. When SPKR(P/M) is a 0 the IA speaker output driver is tristated.

Bit 2 **ADC Gain.**
When control bit ADC Gain is a 0, the ADC gain is -4 dB applied to both ADC inputs before summation and analog-to-digital conversion. When control bit ADC Gain is a 1, the ADC Gain is 0 dB.

Bit 1 **LINEIN Enable.**
When control bit LINEIN Enable is a 1, the line input signal at pin LINEIN is routed to the ADC input. When control bit LINEIN Enable is a 0, the line input signal at pin LINEIN is not routed to the ADC input.

Bit 0 **MIC(M/P) Enable.**
When control bit MIC(M/P) Enable is a 1, the microphone input signal at pins MICM and MICP are routed to the ADC input. When control bit MIC(M/P) Enable is a 0, the microphone input signal at pins MICM and MICP are not routed to the ADC input.

4.3.2 IACR2 IA Control Register 2

The bits in IA Control Register IACR2 control the speaker driver output to microphone input loopback, line output driver attenuation, microphone input to speaker driver output loopback, line input to speaker driver output loopback, and microphone bias voltage.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TxRxLoop	__	__	LINEOUT Attenuation		RxTxLoop		MICBIAS Select

Bit 7 **TxRxLoop.**
When control bit TxRxLoop is a 1 the speaker driver transmit output signal is looped back to the microphone receiver input signal. When TxRxLoop is a 0, this transmit-receive loopback is disabled.

Bit 6 **Reserved.**
Control bit 6 is reserved for modem use. Do not alter.

Bit 5 **Reserved.**
Control bit 5 is reserved for modem use. Do not alter.

Bits 4-3 **LINOUT Attenuation.**
Control bits LINEOUT Attenuation select one of four attenuations for the line output driver.
00 = Analog Ground (Mute)
01 = 0 dB
10 = -6 dB
11 = -12 dB

Bits 2-1 **RxTxLoop.**
Control bits RxTxLoop select and enable one of two receive-transmit loopback and speaker output driver mute.
00 = RxTx Loop disabled
01 = Microphone input looped back to speaker driver output
10 = Line input looped back to speaker driver output
11 = Speaker driver output connected to analog ground (Mute)

Bit 0 **MICBIAS Select.**
When control bit MICBIAS Select is a 1 the voltage present at the MICBIAS output is analog ground (2.5V). When control bit MICBIAS Select is a 0 the voltage present at the MICBIAS output is 2.2V.

4.3.3 IACR3 IA Control Register 3

The bits in IA Control Register IACR3 control the line driver input selection.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
—	—	—	—	—	—	LnInSel	

Bit 7 **Reserved.**
Control bit 7 is reserved for modem use. Do not alter.

Bit 6 **Reserved.**
Control bit 6 is reserved for modem use. Do not alter.

Bit 5 **Reserved.**
Control bit 5 is reserved for modem use. Do not alter.

Bit 4 **Reserved.**
Control bit 4 is reserved for modem use. Do not alter.

Bit 2 **Reserved.**
Control bit 2 is reserved for modem use. Do not alter.

Bits 1-0 **LnInSel.**
Control bits LnInSel select one of three input signals for the Line Driver.
00 = DAC Filter Output
10 = Line In Filter Output
11 = Mic In Filter Output

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5. HDLC FRAMING

The modem supports High Level Data Link Control (HDLC) framing. This protocol is a standard used for data communications. Synchronous Data Link Control (SDLC) is a bit-oriented protocol which is a subset of HDLC. The same format is used in both protocols although all SDLC fields must be eight-bit octets. The modem uses the SDLC eight-bit octet format.

5.1 HDLC FRAMES

Data and control information on a HDLC link are transmitted via frames. These frames organize the information into a format specified by an ISO standard that enables the transmitting and receiving station to synchronize with each other. This format is shown in Figure 5-1.

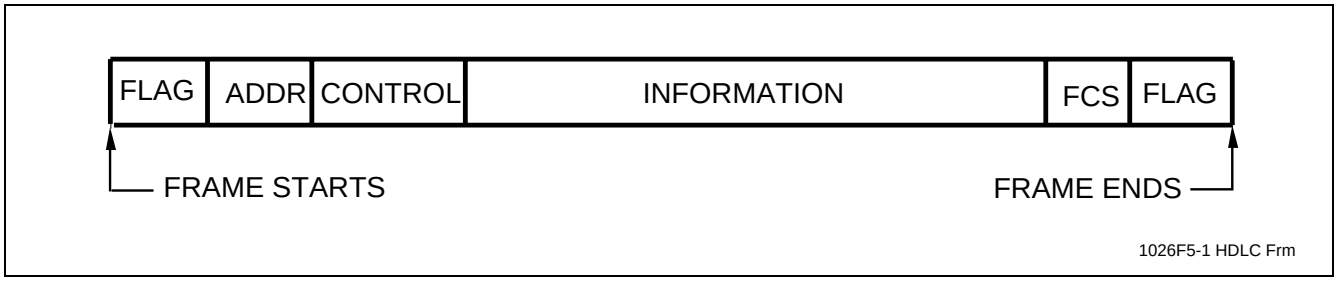

Figure 5-1. HDLC Frame

5.1.1 Frame Fields

5.1.2 Flags

All frames start and end with a flag sequence. The beginning flag and the ending flag are defined by the bit pattern 01111110 (7Eh). The ending flag for one frame can also serve as the beginning flag for the following frame. If separate ending and beginning flags are used, the final zero in the ending flag of one frame may also serve as the first zero of the beginning flag in the following frame. This process is known as "zero-sharing". The zero-sharing bit pattern is 011111101111110.

5.1.3 Address Field

The address field informs the receiver where the information is to go (if the primary station is transmitting) or where the message originated (if a secondary station is transmitting). This field is eight bits in length for the "basic" format.

For the "extended" format, the length is N number of octets, each octet having the first bit a binary zero with the exception of the last octet that begins with a binary one.

Broadcast Address = 11111111

Null Address = 00000000

5.1.4 Control Field

The control field defines the function of the frame. It may contain a command or response. The control field might also contain send or/and receive sequence numbers. This field can be in one of the following formats:

1. Information Transfer Format
2. Supervisory Format
3. Unnumbered Format

This field is normally eight bits in length. However, certain protocols allow for an "extended" control field. For example, it is 16 bits in length for modulo 128 operation of the LAP and LAPB procedures.

5.1.5 Information Field

The modem treats the address field, the control field, and any other transmitted data, except for the flags and the Frame Check Sequence, as the information field. The information field does not have a set length; however, this field follows the SDLC protocol in being in the format of eight bit bytes.

5.1.6 Zero Insertion

Since flags mark the beginning and ending of a frame, some method must be implemented to inhibit or alter the transmission of data that appear as flags. The method used is called "zero insertion". HDLC procedures require that a zero be transmitted following any succession of five continuous ones. This includes all data in the address, control, information and Frame Check Sequence fields. Use of zero insertion denies any pattern of 01111110 to ever be transmitted between beginning and ending flags.

5.1.7 Zero Deletion

When transmitting flags, zero insertion is disabled. During reception of data, after testing for flag recognition, the receiver removes a zero that immediately follows five continuous ones. This is termed "zero deletion". A one that follows five continuous ones signifies either a frame abort (at least seven ones with no zero insertion) or a flag (01111110). The sixth one is, therefore, not removed.

5.1.8 Frame Check Sequence (FCS)

The purpose of the Frame Check Sequence (FCS) is to give a shorthand representation of the entire transmitted information field and to compare it to the identically generated shorthand representation of the received sequence. If any difference occurs, the received frame was in error and should be re-transmitted.

The FCS computation is done on all fields within the frame but does not include the flags. Cyclic Redundancy Check (CRC) is the method used. The polynomial is specified in ITU-T T.30 and X.25 as follows:

$x^{16} + x^{12} + x^5 + 1$

The polynomial is implemented as shown in Figure 5-2.

The FCS is sent as two bytes of data immediately preceding the ending flag of the frame. The FCS register is first preset to all binary ones. The register is then modified by shifting in the data (no flags) contained in the address, control, and information fields. Following the last bit of data, the ones complement of the FCS register is transmitted as the 16-bit FCS. The FCS is transmitted with the highest order bit (x15) first.

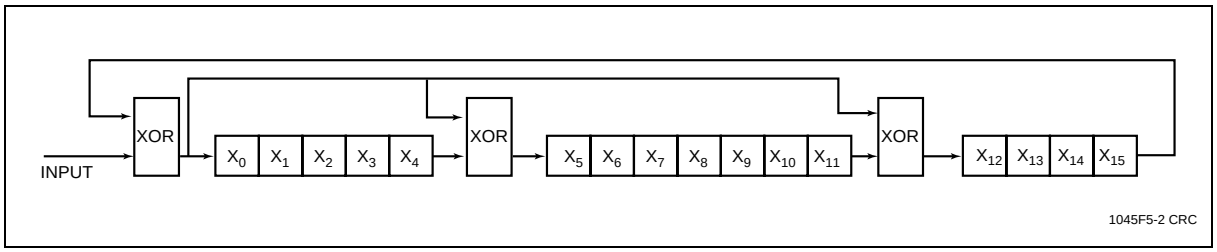

Figure 5-2. CRC Polynomial Implementation

5.1.9 Frame Abortion, Frame Idle, And Time Fill

Frame abortion prematurely finishes transmission of a frame. This occurs by sending at least seven consecutive ones with no zero insertion. This abort pattern terminates a frame immediately and does not require a FCS or an ending flag.

An abort pattern followed by a minimum of eight additional consecutive ones idles the data link. Thus, seven to fourteen ones establish the abort pattern; fifteen or more ones constitute an idle pattern.

Interframe time fill is accomplished by transmitting continuous flags without zero-sharing between flags. Therefore, the transmitter must be capable of sending multiple flags to maintain the active state in the receiver if any time fill is required.

5.2 IMPLEMENTATION

A representation of the HDLC process is shown in Figure 5-3. The events are numbered in order of occurrence from one to four.

1. The beginning flag is transmitted. The receiver sees the flag and now becomes aligned with the transmitter. Both the receive and the transmitter FCS registers are preset to FFFFh.
2. The information field is transmitted. The data is also run through the FCS register before zero insertion. At the receive end, after the zero deletion algorithm, the data is presented to the user and then run through the FCS register.
3. The FCS is inverted and then transmitted. The transmitted FCS is passed through the receiver's FCS register. The shift register will contain 1111000010111000 if the frame has been received correctly.
4. The ending flag is transmitted. The signal timing is illustrated in Figure 5-4.

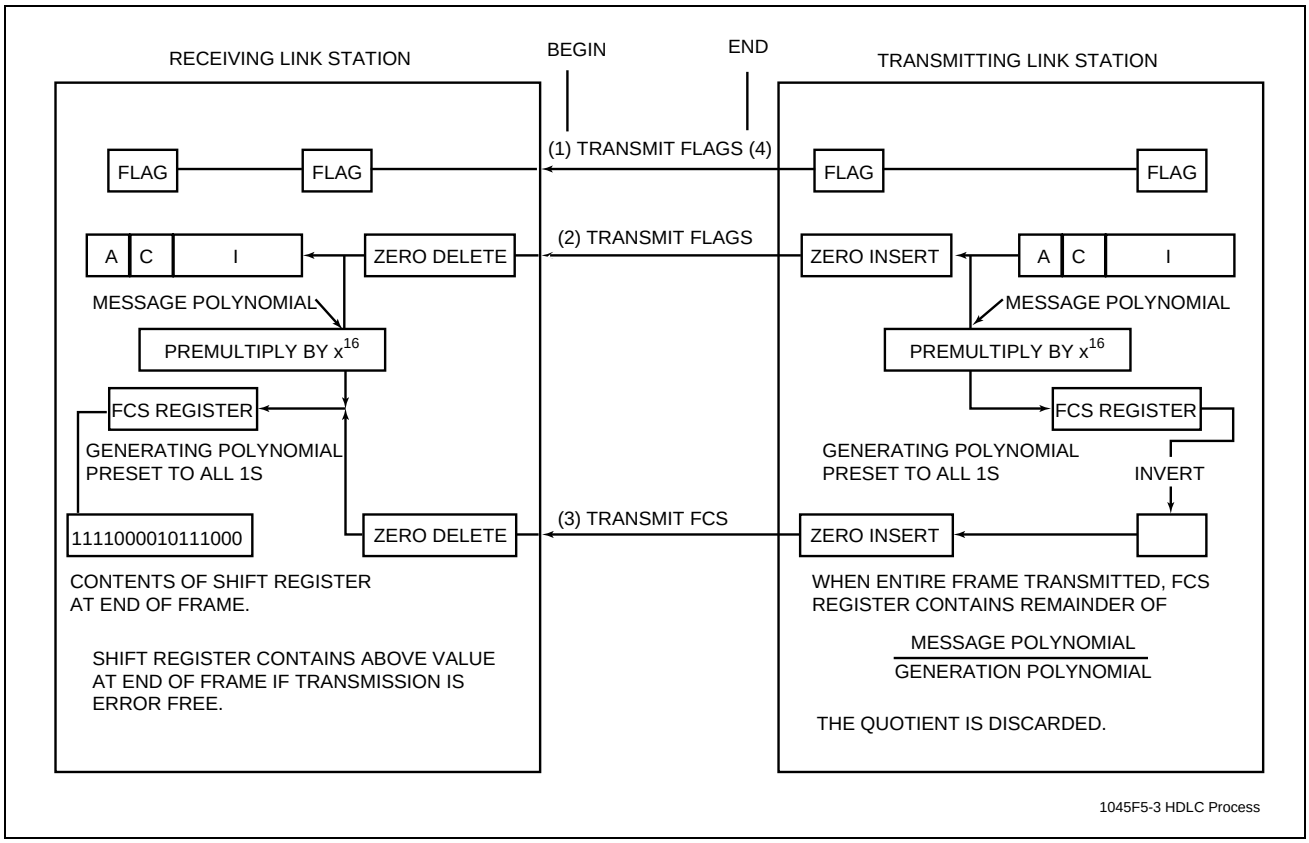

Figure 5-3. HDLC Process

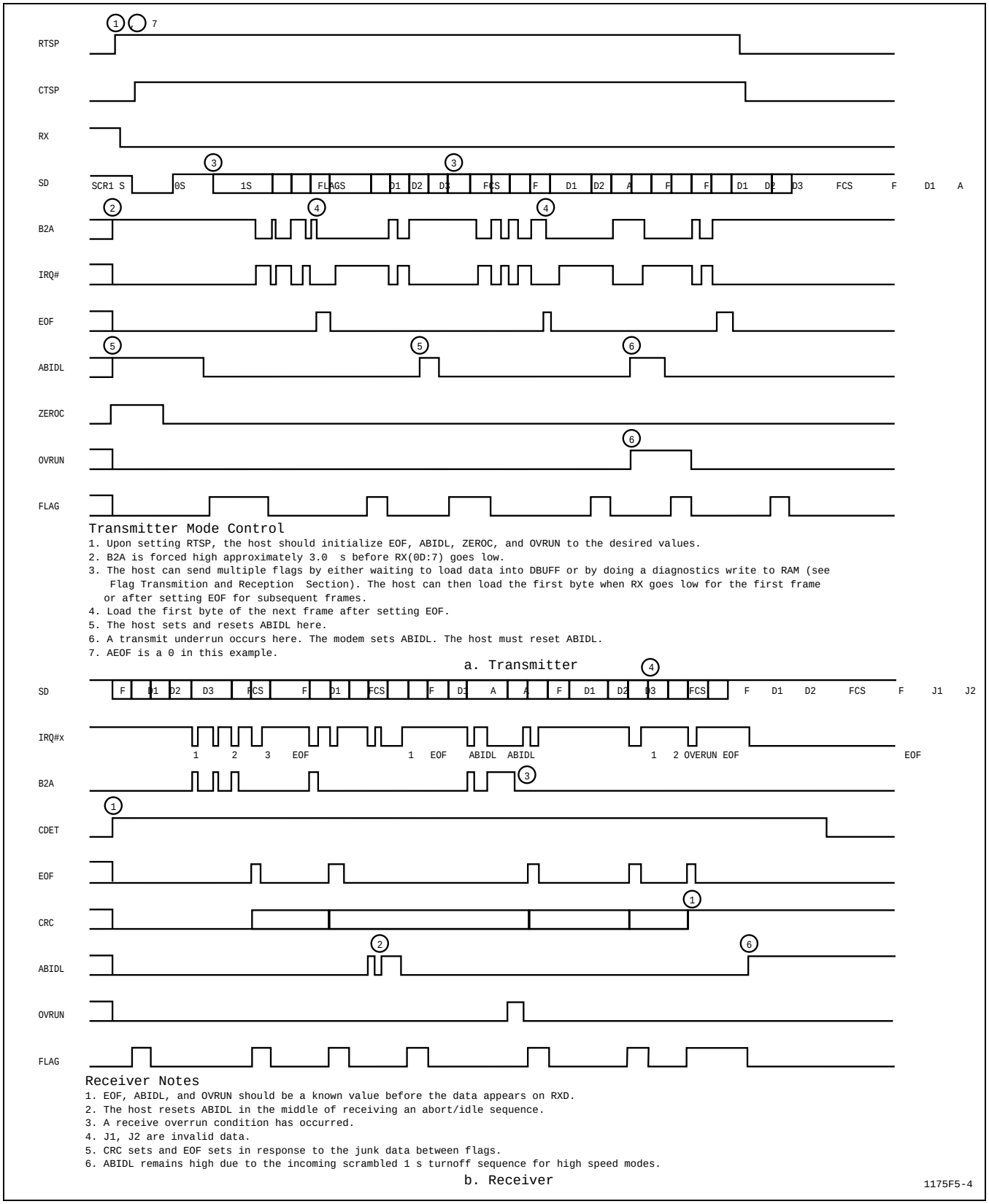

Figure 5-4. HDLC Signal Timing

5.2.1 Mode Selection

In order to use HDLC in the modem, the host processor must:

1. Set up the modem configuration.
2. Set the parallel data mode bit (PDM).
3. Set the HDLC mode bit.
4. Set the SETUP bit.

RAM Access 1 (using ADD1) remains available while RAM Access 2 (using ADD2) is unusable in the parallel data mode. HDLC transmission cannot be performed using the serial interface.

The format of the data input to the modem is in groups of 8-bit bytes. As in the parallel data mode, the least significant bit of the byte is transmitted first.

5.2.2 Transmission and Reception Rate

HDLC implemented in the modem runs under the following transmitter and receiver modes:

V.33 and V.17

V.29

V.27 ter

V.21

V.21 with DTMF receiver

5.2.3 Transmitter and Receiver Initialization

The HDLC transmitter and receiver is initialized differently than other modes upon power-up, reconfiguration, or turning on RTS# input or RTSP bit. Table 5-1 shows the states of the interface memory bits for HDLC initialization.

Table 5-1. Transmitter and Receiver Initialization

Parameter	Transmitter	Receiver
ABIDL	0 (Note 2)	0 (Note 2)
AEOF	0 (Note 2)	0 (Note 2)
B2A	1	Not initialized
CRC	0 (Note 1, 2)	0 (Note 2)
EOF	0 (Note 2)	0 (Note 2)
FLAG	0	0
OVRUN	0 (Note 2)	0 (Note 2)
ZEROC	0 (Note 2)	0 (Note 2, 3)

Notes: 1.

1. Not applicable in the transmitter.
2. Zeroed only upon power-up; unchanged elsewhere.
3. Not applicable in the receiver.

5.2.4 Flag Transmission and Reception

The modem transmitter sends at least one flag as the opening flag of the first frame. As long as the user does not load the 8-bit transmit data register, DBUFF (register 10h), with data, the modem sends continuous flags with no zero-sharing (0111111001111...). This facilitates transmission of the preamble as specified in T.30. Thus, the transmitter defaults to transmitting time-fill and, therefore, keeps the receiving link station active.

To assist the user in transmitting more than one flag between frames or at the end of the final frame, a counter can be accessed through modem diagnostics. This counter decrements directly in the signal processor's RAM. This means that the number written will only last for one group of flags. For example, FSK should have at least two beginning flags for the first frame and at least two ending flags for the final frame. However, frames between these two require only one flag. This is why the counter decrements directly and one flag is transmitted as a default. Diagnostics should be setup as shown below:

ADD1 = 85h

AREX1 = 0

BR1 = 0

CR1 = 1

WRT1 = 1

The value to write into YDAM1 and YDAL1 should be 1 less than the number of flags desired. This value can be written anytime after the RX bit returns to zero and before FLAG is set by the modem.

Using the FSK example above, assume three flags are to be transmitted at the beginning of the first frame and at the end of the final frame.

1. Turn on RTS.
2. Wait until the RX bit is reset by the modem.
3. Disable diagnostics 1 (reset ACC1).
4. Setup diagnostics 1 as above, write 00h into YDAM1, and write 02h into YDAL1.
5. Enable diagnostics 1 (set ACC1).
6. Wait until B1A is set before resetting WRT1.
7. For the ending flag of the final frame, immediately after loading in the final byte of data or after setting EOF, again setup diagnostics 1 as above, write 00h into YDAM1, and write 02h into YDAL1.

Another method exists for sending extra flags. The host must simply do nothing since flags are transmitted as the default condition. In other words, after the final zero in a flag is transmitted, the modem looks to see if the host has loaded new data into DBUFF (B2A is reset). If no new data is loaded before this time, another flag is sent. Therefore, if more than one flag is desired, the host must wait N-1 multiples of eight bit times after FLAG is set by the modem to load new data into DBUFF, where N is the number of flags. The host then has seven bit times in which to load new data and thus prevent another flag from being sent. For example, if three flags are desired between frames, the host must wait at least 16 bit times and not more than 23 bit times after FLAG is set by the modem.

As the default condition, the modem receiver continually searches for the flag data pattern. When one or more flags are detected, the interface memory status bit FLAG (09:0) is set. The flags themselves are not presented to the host through the DBUFF register. Therefore, as soon as a flag is observed, the modem examines the next byte of received data. If it is a flag, an abort/idle sequence, or a FCS, it is not given to the user. Instead, the appropriate status bits are set or reset.

The modem also has the capability to detect consecutive flags with zero-sharing.

5.2.5 Information Field Transmission and Reception

For information field transmission, the host should wait for CTSP (0F:1) to transition high. The host must then load the data into DBUFF and then wait for the data available bit B2A (1E:3) to be set by the modem before loading in the next byte of data. If AEOF is 0 and the next byte is not loaded into DBUFF within the next eight bit times, the modem will set OVRUN (09:7), indicating an underrun condition has occurred. To tell the modem that the host wants to end the frame, the host must set EOF as soon as the modem has taken the last byte of the frame (B2A sets). When the modem recognizes EOF being high, the modem will reset EOF and will transmit the FCS and closing flag. Once the host sets EOF, the host may load in the first byte of data of the next frame into DBUFF. If the host wants to end transmission, the host must wait for EOF to return low before turning off RTS or RTS#.

The automatic frame ending feature can be used to more easily facilitate the use of a DMA interrupt system. With this feature, data is transmitted as described in the above paragraph. However, when AEOF (15:5) is set by the host, the ending of the frame occurs "automatically," without the host having to perform any handshaking. When the host is finished sending the data in the frame, the host should wait until EOF is set to a 1 by the modem. The modem will then send the 16-bit FCS and at least one ending flag. When EOF is set to a 1 by the modem, the host can then load in the first byte of data of the next frame. EOF will be set to a 0 by the modem at the beginning of flag transmission. Therefore, the underrun condition as described in the previous paragraph is the exact same condition that causes the 16-bit FCS and ending flag to be transmitted when AEOF is set to 1.

In the receiver, only the information field data between flags is passed to the user through the DBUFF register by the use of the handshaking bit B2A. The user must wait for B2A to be set by the modem and then take the data. If AEOF is 0 and the host does not read the data within eight bit times, OVRUN will set indicating an overrun condition, and the data in DBUFF will be overwritten by the next byte.

Furthermore, no flags, abort/idle sequence, or FCSs are given to the user via the DBUFF register. Since these fields are not presented to the user, there is at least a 16-bit time delay in the reception of data when receiving these fields. This allows the FCS and ending flag, continuous flags, or the abort/idle sequence to be flushed out of the internal buffers.

5.2.6 FCS and Ending Flag Transmission and Reception

If AEOF is 0, the host ends a frame by loading in his last byte of data into DBUFF, waiting until the modem has taken it (B2A sets), and then setting EOF. After setting EOF, the host may load in the first byte of data of the next frame into DBUFF. When the modem recognizes that the host wants to end the frame, the modem will reset EOF. To terminate data transmission, the host may turnoff RTS or RTSP when the modem resets EOF. After resetting EOF, the modem will automatically transmit the 16-bit FCS and at least one flag that signifies the end of the current frame and, if another frame follows, the beginning of the next frame.

For the case when AEOF is set to 1 (automatic end of frame), the host ends a frame by loading the last byte of data and waiting until EOF is set to 1 by the modem. The host may then load in the first byte of data of the next frame. To terminate data transmission, the host may turn off RTS or RTSP when the modem sets EOF to 1. The modem will then automatically transmit the 16-bit FCS and at least one flag that signifies the end of the current frame and, if another frame follows, the beginning of the next frame. The modem will set EOF to 0 upon sending a flag.

Upon the receipt of an ending flag in the current frame (which may also be the beginning flag of the next frame), the modem examines the data in the FCS register and compares it to the remainder. If the FCS register remainder is correct, CRC (09:1) is reset. Conversely, if the remainder is incorrect, the CRC bit is set. This is the only time CRC is updated (except upon power-up). Following this determination, the modem sets EOF. Thus, once the modem sets EOF, the host can examine CRC to determine whether or not an erred frame was received. It is left to the host to reset the EOF bit. If the user does not reset EOF before the end of the next frame, the host will not get any indication that the following frame has ended.

5.2.7 Abort/Idle Sequence Transmission and Reception

An abort/idle sequence can be sent by the host setting the bit ABIDL (09:3) in the interface memory. This stops any normal frame transmission, as well as continuous flag transmission, and sends continuous ones. After the setting of ABIDL is detected, the modem first completes the transmission of the current byte of data. Immediately after this transmission, the modem sends eight consecutive ones. After these eight bit times, if ABIDL is still set, eight ones are sent again. To discontinue this sequence, ABIDL must be reset. Then, if no new data is loaded into DBUFF, continuous flags are sent. If new data is loaded into DBUFF (B2A is reset), the modem sends a beginning flag and then the data in DBUFF. The modem will also recognize the setting of ABIDL while transmitting the FCS, thereby allowing the receiver to recognize that the transmitted frame should be discarded.

The modem has the ability to send continuous zeros. To accomplish this, ABIDL and ZEROC (09:4) must be set. The modem completes the transmission of the current byte and then sends eight consecutive zeros. After this time, if ABIDL remains set, eight zeros are sent again. To discontinue this sequence, ABIDL must be reset or, if continuous ones are desired, ZEROC only must be reset. However, if no new data is loaded in DBUFF and ABIDL is reset, continuous flags are sent regardless of the state of ZEROC. Then, if new data is loaded into DBUFF (B2A is reset), the modem sends a beginning flag and then the data in DBUFF.

The modem in HDLC mode not only continually searches for flags, but also continually searches for an abort/idle sequence. When the receive modem encounters this data pattern, it sets the abort/idle receive bit ABIDL. It is left up to the host to reset this bit. However, receiver processing will continue unaffected by the state of this bit.

The reception of data immediately following the abort/idle sequence is treated as invalid and is not presented to the user. Therefore, to re-establish transmitter and receiver synchronization, the receiver must see at least one flag. At least one flag and three bytes of data must be received following the abort sequence before any data is given to the host.

5.2.8 Underrun and Overrun Conditions

A bit in the interface memory OVRUN (09:7) is used to indicate to the host processor that a transmit underrun condition has occurred. If the host does not load in a new byte of data within eight bit times, OVRUN and ABIDL will be set by the modem and the modem will automatically send a minimum of eight continuous ones. This abort sequence will continue until the host resets ABIDL. After the host resets ABIDL, the modem will finish sending the current byte of ones and will then send a flag. At the end of sending a flag, if B2A is reset, the modem will interpret the data in DBUFF as being the first byte of the next frame. After uploading this data for the first byte of the frame, the modem will reset OVRUN. The modem will always reset OVRUN every time it sets B2A, except upon transmitter HDLC initialization. (The underrun condition is not applicable when AEOF = 1.)

In the receiver, the OVRUN bit will inform the host that an overrun condition occurred. The overrun condition takes place when the receiver fails to take the byte of data in DBUFF within eight bit times. The modem will thus overwrite the data in DBUFF and, if the host has not taken the data (B2A is not reset), the modem will set OVRUN. To detect further overrun occurrences, the host must reset this bit.

5.2.9 Transmit Mode Control

After power-up, reconfiguration, or turning RTS# input or RTSP bit on, the host must wait for CTS# output or CTSP bit to turn on before starting frame transmission.

There are two ways in which the user can signal the modem to exit current HDLC execution. The first way is by setting the SETUP bit which tells the modem that a new configuration is desired. The second way is by turning off RTS# input or by resetting the RTSP bit in the interface memory. In both cases, the following events will occur:

1. When AEOF is set to a 0 and if exiting after making sure the modem took the data in DBUFF, setting EOF to a 1, and then waiting for EOF to be set to a 0 by the mode, the modem sends the last byte of data followed by the 16-bit FCS sequence and a closing flag. The modem then either goes through the turn-off sequence (if RTS output or RTSP bit is turned off), or sets up the new configuration (if SETUP is set to 1).
2. When AEOF is a set to a 1 and if exiting after making sure the modem sets EOF to a 1, the modem sends the last byte of data followed by the 16-bit FCS sequence and a closing flag. The modem then either goes through the turn-off sequence (if RTS output or RTSP bit is turned off), or sets up the new configuration (if SETUP is set to 1).
3. Exiting during the transmission of an abort sequence, the modem finishes sending the last byte of the abort sequence, then either goes through the turn-off routine or sets up to a new configuration.

5.3 EXAMPLE APPLICATION

Refer to Section 3 for a description of the bits associated with the HDLC and programmable interrupt functions.

5.3.1 Transmitter Example

1. the modem configuration to the desired speed for transmitting, enable HDLC, parallel data mode, and RTSP. (AEOF defaulted to 0).
2. Wait until CTSP goes low and returns to a high level.
3. Place the first byte of data into DBUFF. The modem transmits a flag followed by this byte of data.
4. As soon as B2A is set, load in the next byte of data. This must occur within eight bit times of B2A being set.
5. After all information but the last byte is given to the modem, load in the last byte of data in the frame as in step 4.
6. To end the frame, the host must load in the last byte of data into DBUFF, wait for B2A to be set, and then set EOF.
7. Repeat steps 3 through 6 for all frames to be transmitted.
8. When the last byte of the final frame is loaded into register DBUFF, wait for B2A to return high. Then set EOF and wait for EOF to return low before resetting RTSP. The modem transmits the last byte followed by the 16-bit FCS and at least one closing flag, depending upon if diagnostics was used to write into the flag counter RAM location as mentioned previously. The modem then goes through its normal turn-off routine.

5.3.2 Receiver Example

The steps to perform a typical HDLC reception are:

1. Set the modem configuration to the desired speed for receiving, enable HDLC, and parallel data mode.
2. Perform a dummy read of DBUFF to reset B2A.
3. Wait until the modem has properly configured.
4. Monitor, through interrupts, the EOF, ABIDL, and B2A bits in the interface memory.
5. Wait for an interrupt. If it is caused by B2A being set, read the data in DBUFF. This indicates that the first byte of the first frame is ready for host reading. If the interrupt is caused by EOF being set, check CRC to determine if the current frame is in error and reset EOF. If the interrupt is caused by ABIDL, the modem is receiving the abort/idle sequence. The current frame that was aborted is invalid. The modem does not set the CRC bit or the EOF bit in this case since no FCS checking is done.
6. Continue waiting for interrupts and take appropriate action when the interrupts are received.

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6. TONE DETECTOR FILTER TUNING

This section describes a method of tuning the filters in the modem for tone detection.

6.1 PROGRAMMABLE TONE DETECTORS

The modem includes three independently programmable tone detectors (F1, F2, and F3). Upon power-up, the tone detectors are centered at 2100 Hz (F1), 1100 Hz (F2), and 462 Hz (F3); the sample rate is 9600 Hz only.

In each of the three detectors, two second-order biquadratic filters can be programmed for a variety of frequency responses. The modem sets interface memory bits FR1, FR2, and FR3 to a 1 when tone detectors 1, 2, and 3 detect energy above their respective threshold. This application note presents a method of tuning these detectors to any frequency in the 400 Hz – 3000 Hz band.

By setting bit 12TH to a 1 in the interface memory, the three tone detectors are cascaded to form a programmable 12th-order filter. In this case the modem sets only the FR3 bit to a 1 when energy is above the threshold.

6.1.1 Computation of Tone Detector Coefficients

Each tone detector consists of two cascaded second-order filters, an energy averaging filter, and a threshold comparator. A diagram of a tone detector is shown in Figure 6-1.

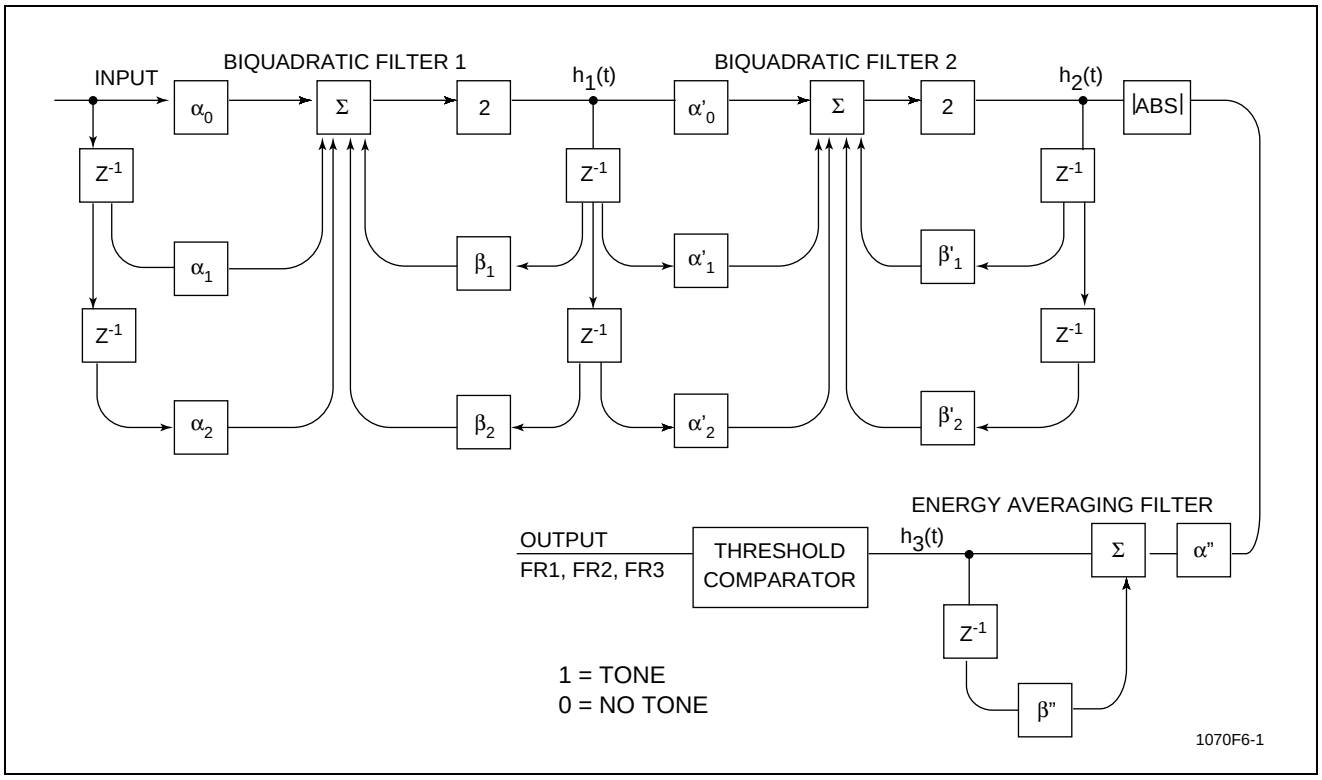

Figure 6-1. Modem Tone Detection Diagram

Filter 1 has a transfer function:

$$H_1(Z) = 2(\alpha_0 + \alpha_1 Z^{-1} + \alpha_2 Z^{-2})/(1 - 2\beta_1 Z^{-1} - 2\beta_2 Z^{-2}) \quad \text{(Eq. 1)}$$

Filter 2 has a transfer function:

$$H_2(Z) = 2(\alpha'_0 + \alpha'_1 Z^{-1} + \alpha'_2 Z^{-2})/(1 - 2\beta'_1 Z^{-1} - 2\beta'_2 Z^{-2}) \quad \text{(Eq. 2)}$$

The energy averaging filter has a transfer function:

$$H_3(Z) = \alpha''/(1 - \beta'' Z^{-1}) \quad \text{(Eq. 3)}$$

The output of the energy average is fed to a threshold comparator that sets interface memory bit FR1, FR2, or FR3 to a 1 if the output is equal to or greater than the Tone Detector threshold (default value = 1/8 of full scale), otherwise, the bits are set to a 0.

Filters 1 and 2 have frequency response as shown in Figure 6-2. When cascaded, they form a bandpass filter with a narrow bandwidth as shown in Figure 6-3.

Given the transfer functions $H_1(Z)$ and $H_2(Z)$, an analytical method is provided to compute their coefficients for any frequency in the 400 Hz – 3 kHz band. First, consider $H_1(Z)$. This transfer function can be rewritten as:

$$H_1(Z) = 2(\alpha_0 Z^2 + \alpha_1 Z + \alpha_2)/(Z^2 - 2\beta_1 Z - 2\beta_2) \quad \text{(Eq. 4)}$$

which has a conjugate pair of poles:

$$P_1 = \beta_1 + \sqrt{(\beta_1 2 + 2\beta_2)}$$

and

$$P_2 = \beta_1 - \sqrt{(\beta_1 2 + 2\beta_2)}$$

Upon power up, these poles lie on a circle of radius 0.994030884 on the Z-plane. The radius of the tone detector circle was chosen so that each filter has a high Q without being unstable (poles must lie inside the unit circle for stability). Figure 6-4 shows a Z-plane pole-zero diagram for an arbitrary conjugate pole pair on the tone detector circle. The angle $\theta = 360\ f_O/f_S$, where f_O is the desired center frequency and f_S is the sampling rate.

The following equations are derived from the angle and magnitude of the position vector pointing to a pole pair located at the desired angle:

$$\cos^{-1}(\beta_1/r) = \theta = 360° \times f_O/f_S \quad \text{(Eq. 5)}$$

$$\sqrt{[\beta_1 2 + (-\beta_1 2 - 2\beta_2)]} = r = 0.994030884 \quad \text{(Eq. 6)}$$

Solving for β_1 and β_2:

$$\beta_1 = r \cos (360° \times f_O/f_S) \quad \text{(Eq. 7)}$$

$$\beta_2 = -r^2/2 \quad \text{(Eq. 8)}$$

In deriving these equations, only $H_1(Z)$ was considered. However, the tone detector consists of two identical filters in cascade. Referring to Figure 6-3, shifting filter 1 and filter 2 above and below the desired center frequency, a response with the desired bandwidth is achieved. Furthermore, since the α_1, α'_1, α_2, and α'_2 coefficients default to zero upon power-up, α_0 controls the amplitude response, and one may set $\alpha_0 = \alpha'_0$ to uniformly raise or lower the overall cascade response.

From Equation 8:

$$\beta_2 = \beta'_2 = -r^2/2 = -0.494048699$$

Rewriting Equation 7 in terms of the offsets f_A and f'_A:

$$\beta_1 = r \cos [360° (f_O - f_A)/f_S] \quad \text{(Eq. 9)}$$

$$\beta'_1 = r \cos [360° (f_O + f'_A)/f_S] \quad \text{(Eq. 10)}$$

The frequency offset is approximately 72% of B/2 (half the bandwidth) for most applications:

$$\beta'_2 \cong 0.72 \, (B/2) \quad \text{(Eq. 11)}$$

The value of f_A should be equal to f'_A. However, f_A may be chosen 1% smaller than f'_A to compensate for the fact that the overall cascade response is not perfectly symmetrical, near DC (see Figure 6-5).

The values for the coefficients α_0 and α'_0 that set $|H(f_O)| = 0$ dB in equations 1 and 2 were measured and plotted versus center frequency f_O as shown in Figure 6-6. Three equations corresponding to three linear approximations result:

$$\alpha_0 = \alpha'_0 = [(104/319)f_O - 78.62]/32767$$

$$400 = f_O \leq 1100 \text{ Hz} \quad \text{(Eq. 12a)}$$

$$\alpha_0 = \alpha'_0 = [(44/275)f_O + 104]/32767$$

$$1100 \leq f_O \leq 1650 \text{ Hz} \quad \text{(Eq. 12b)}$$

$$\alpha_0 = \alpha'_0 = [(4/45)f_O + 221]/32767$$

$$1650 \leq f_O \leq 3000 \text{ Hz} \quad \text{(Eq. 12c)}$$

6.1.2 Energy Averaging Filter

The coefficients of the energy averaging filter are determined by a Z-domain approximation to an RC circuit of transfer function $H(S) = 1/(1 + S\tau)$:

$$\alpha'' = 1/(1 + f_S\tau) \quad \text{(Eq. 13)}$$

$$\beta'' = 1/[1 + (1/f_S\tau)] \quad \text{(Eq. 14)}$$

Upon power up, α'' and β'' are set for $\tau = 0.1$ seconds. Unless different tone detector response times are required, these coefficients need not be changed. In Speakerphone and Voice/Audio Codec modes, the coefficients should be changed to compensate for the 8000 Hz sample rate.

The Tone Detector Threshold value is programmable in DSP RAM (see Section 4).

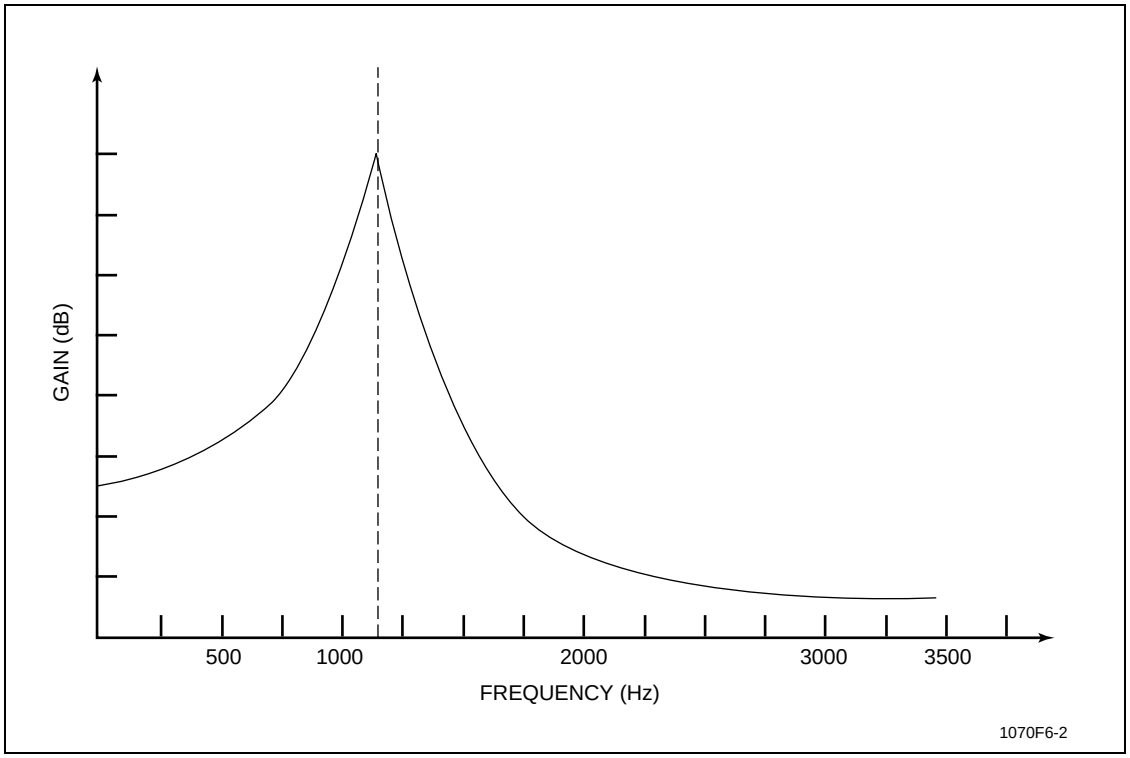

Figure 6-2. Typical Single Filter Response

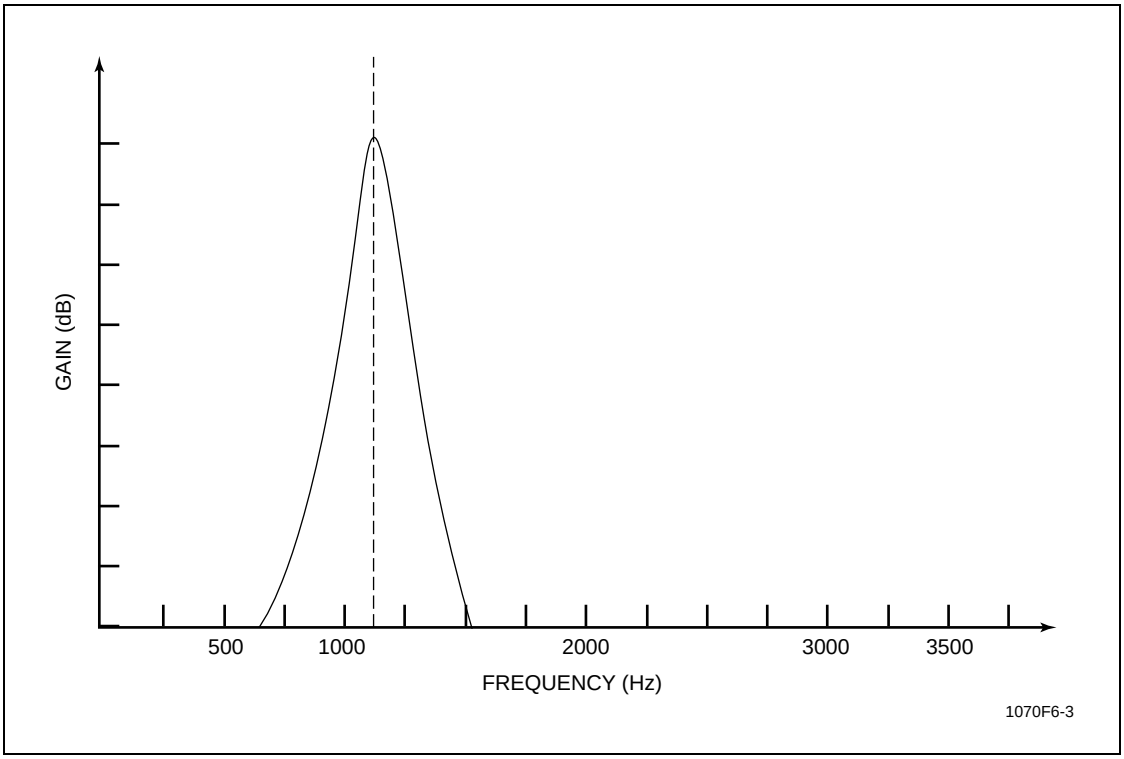

Figure 6-3. Typical Cascade Filter Response

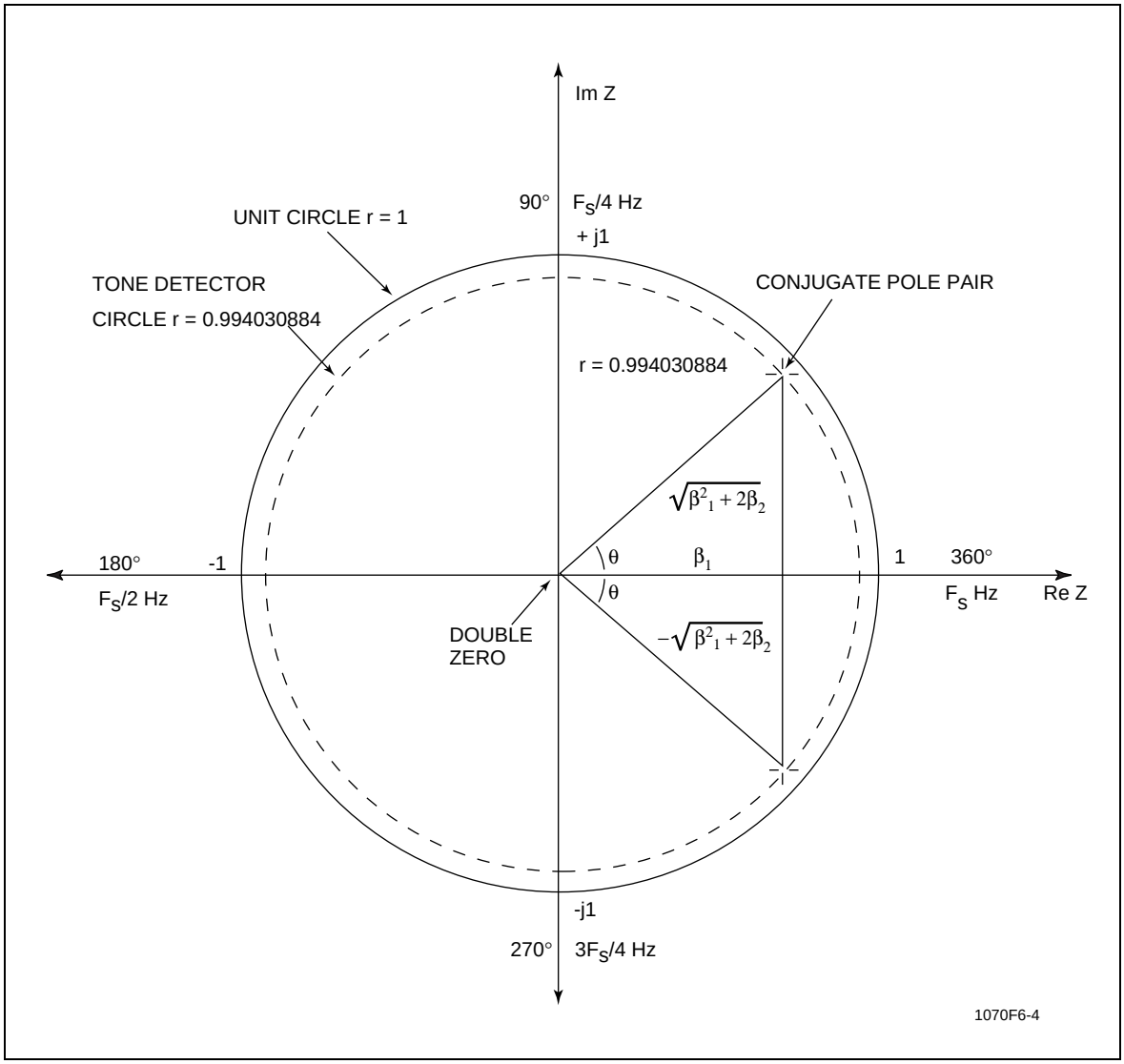

Figure 6-4. Z-Plane Pole-Zero Diagram

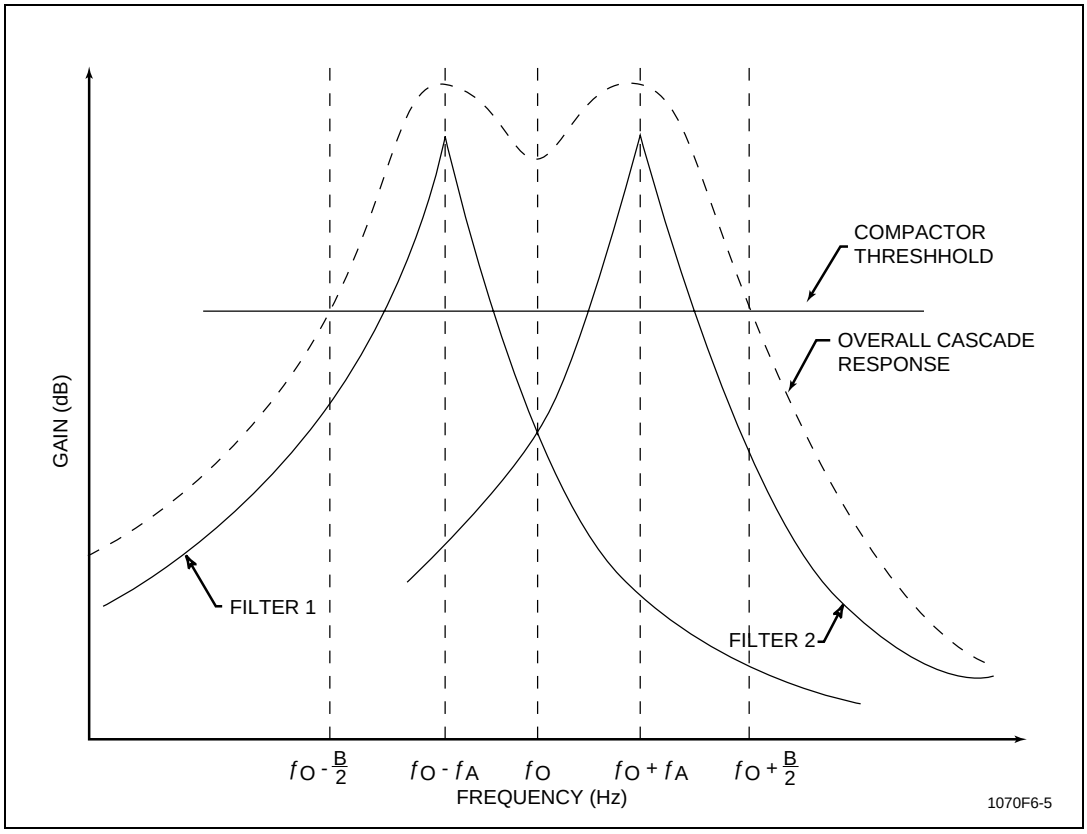

Figure 6-5. Bandwidth and Offset Frequencies

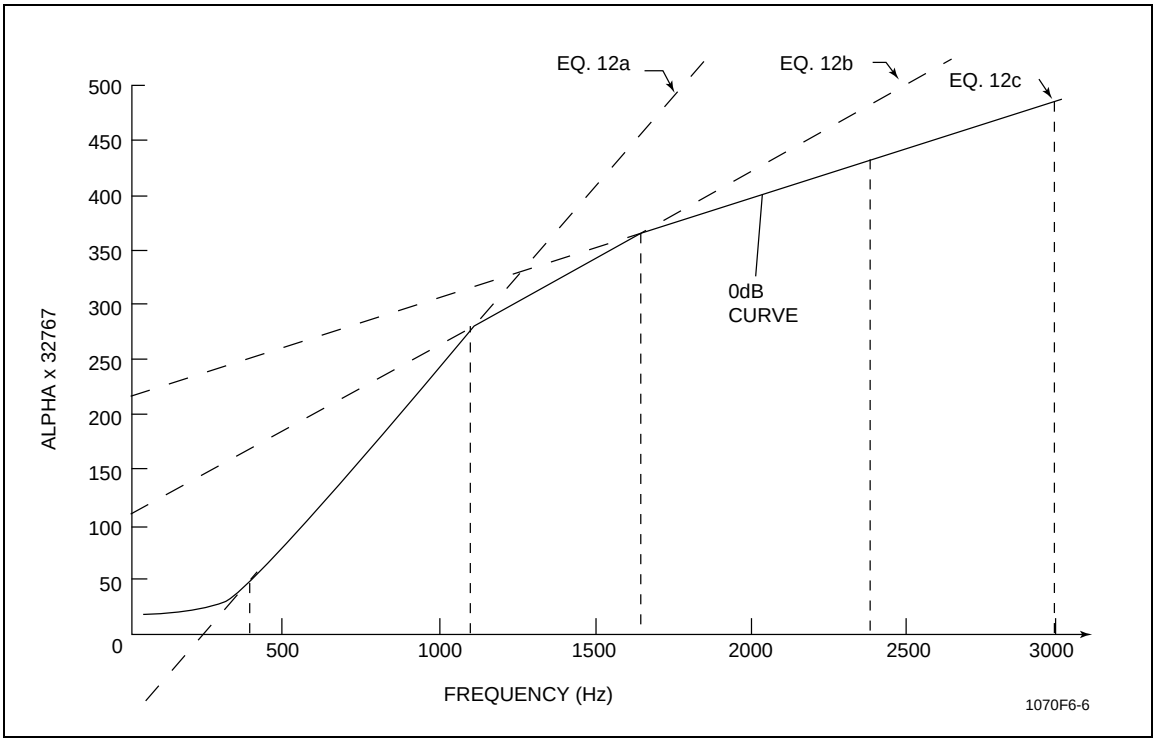

Figure 6-6. Alpha-zero Center Frequency

6.1.3 Filter Coefficients

Table 6-1 contains the RAM access codes for all filter coefficients. Refer to the Section 4 for the proper procedure for writing new coefficients into the RAM locations.

Table 6-2 contains the computed values of the filter coefficients, including those of default frequencies 462 Hz, 1100 Hz, and 2100 Hz. The value 32767 (7FFFh) is full scale in the DSP's machine units (32767 = unity). Coefficients may range from –1 to +1 (8000h to 7FFFh) in machine units. The sample rate is 9600 Hz.

6.2 TONE DETECTORS IN VOICE CODEC, AUDIO CODEC AND SPEAKERPHONE MODES

The tone detector coefficients must be reprogrammed when configured to Voice/Audio Codec and Speakerphone modes that use 8000 Hz sample rates.

Table 6-3 contains the computed values of the filter coefficients at the sample rate of 8000 Hz.

Table 6-1. Filter Coefficient RAM Access Codes

	RAM Write Access Code (Hex)		
Coefficient Name	Tone 1	Tone 2	Tone 3
α_0	25	2B	31
α_1	26	2C	32
α_2	27	2D	33
α'_0	28	2E	34
α'_1	29	2F	35
α'_2	2A	30	36
β_1	A6	AC	B2
β_2	A7	AD	B3
β'_1	A9	AF	B5
β'_2	AA	B0	B6
α''	A8	AE	B4
β''	A5	AB	B1

Notes:
In all cases:
AREXx (x=1, 2) is a 0,
CRx (x= 1, 2) is a 1,
BRx (x= 1, 2) is a 0, and
DRx (x= 1,2) is a 0.
If the most significant bit (MSB) of the address is a 0, the data is written to XRAM; if the MSB is a 1, the data is written to YRAM.

Table 6-2. Calculated Coefficient Values, 9600 Hz Sample Rate

Frequency Detected	Coefficient Name	Coefficient Value (Hex)	Coefficient Value (Decimal)
2100 Hz ±25 Hz; $f_A \cong$18 Hz	$\alpha_0 = \alpha'_0$	0198	0.01245117
	$\alpha_1 = \alpha'_1 = \alpha_2 = \alpha'_2$	0000	0.00000000
	β_1	1A4A	0.20538330
	β'_1	175A	0.18243408
	$\beta_2 = \beta'_2$	C0C4	–0.49401855
1850 Hz ±24 Hz; $f_A \cong$18 Hz	$\alpha_0 = \alpha'_0$	0180	0.01171875
	$\alpha_1 = \alpha'_1 = \alpha_2 = \alpha'_2$	0000	0.00000000
	β_1	2E37	0.36105347
	β'_1	2B69	0.33914184
	$\beta_2 = \beta'_2$	C0C4	-0.49401855
1650 Hz ±23 Hz; $f_A \cong$18 Hz	$\alpha_0 = \alpha'_0$	0170	0.01123047
	$\alpha_1 = \alpha'_1 = \alpha_2 = \alpha'_2$	0000	0.00000000
	β_1	3D48	0.47875977
	β'_1	3AA6	0.45819092
	$\beta_2 = \beta'_2$	C0C4	-0.49401855
1100 Hz ±30 Hz; $f_A \cong$ 19 Hz	$\alpha_0 = \alpha'_0$	0118	0.00854492
	$\alpha_1 = \alpha'_1 = \alpha_2 = \alpha'_2$	0000	0.00000000
	β_1	60BE	0.75579834
	β'_1	5E9C	0.73913574
	$\beta_2 = \beta'_2$	C0C4	-0.49401855
462 Hz ±14 Hz; $f_A \cong$ 10 Hz	$\alpha_0 = \alpha'_0$	0048	0.00219726
	$\alpha_1 = \alpha'_1 = \alpha_2 = \alpha'_2$	0000	0.00000000
	β_1	79F3	0.95272827
	β'_1	7974	0.95152405
	$\beta_2 = \beta'_2$	C083	–0.49601733

Table 6-3. Calculated Coefficient Values, 8000 Hz Sample Rate

Frequency Detected	Coefficient Name	Coefficient Value (Hex)	Coefficient Value (Decimal)
2100 Hz ±25 Hz; $f_A \cong 18$ Hz	$\alpha_0 = \alpha'_0$	0198	0.01245117
	$\alpha_1 = \alpha'_1 = \alpha_2 = \alpha'_2$	0000	0.00000000
	β_1	F7D0	-0.06396680
	β'_1	F43A	-0.09198279
	$\beta_2 = \beta'_2$	C0C5	–0.49403363
1850 Hz ±30 Hz; $f_A \cong 18$ Hz	$\alpha_0 = \alpha'_0$	0181	0.01174963
	$\alpha_1 = \alpha'_1 = \alpha_2 = \alpha'_2$	0000	0.00000000
	β_1	10BD	0.13077181
	β'_1	0D2A	0.10284738
	$\beta_2 = \beta'_2$	C0C5	-0.49403363
1650 Hz ±23 Hz	$\alpha_0 = \alpha'_0$	0113	0.00839260
	$\alpha_1 = \alpha'_1$	FE7B	-0.01187170
	$\alpha_2 = \alpha'_2$	0113	0.00839260
	β_1	25C4	0.29505295
	β'_1	23F8	0.28101444
	β_2	C12D	-0.49081421
	β'_2	C120	-0.49121094
1100 Hz ±30 Hz; $f_A \cong 19$ Hz	$\alpha_0 = \alpha'_0$	0118	0.00854492
	$\alpha_1 = \alpha'_1 = \alpha_2 = \alpha'_2$	0000	0.00000000
	β_1	5410	0.65675819
	β'_1	512D	0.63420078
	$\beta_2 = \beta'_2$	C0C5	-0.49403363
462 Hz ±14 Hz; $f_A \cong 10$ Hz	$\alpha_0 = \alpha'_0$	0048	0.00219726
	$\alpha_1 = \alpha'_1 = \alpha_2 = \alpha'_2$	0000	0.00000000
	β_1	7789	0.93389591
	β'_1	76D3	0.92834283
	$\beta_2 = \beta'_2$	C083	–0.49601733

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7. DTMF DIALING WITH AUTO DIALER

The modem includes tunable oscillators that can be used to perform dual-tone multi-frequency (DTMF) dialing. The frequency and amplitude of each oscillator output is under host control. A programmable tone detector can also be used in call establishment to recognize an answer tone.

This section describes the method of oscillator and filter tuning by the host processor and provides an example of an autodialer routine that may be programmed into the host.

7.1 DTMF REQUIREMENTS

EIA Standard RS-496, (Section 4), specifies requirements that ensure proper DTMF signaling through the public switched telephone network (PSTN). These tones consist of two sinusoidal signals, one from a high group of frequencies and one from a low group of frequencies, that represent each of the pushbutton telephone characters shown in Table 7-1.

Table 7-1. DTMF Signals

Low Frequency	High Frequency			
	1209 Hz	**1336 Hz**	**1477 Hz**	**1633 Hz**
697 Hz	1	2	3	A
770 Hz	4	5	6	B
852 Hz	7	8	9	C
941 Hz	*	0	#	D

Signal power is defined for the combined tones as well as for the individual tones. Both maximum and minimum power requirements are functions of loop current. By combining the various requirements of RS-496, compromise power levels can be determined that meet the power specification for all U.S. lines (when driving the PSTN from a 600 ohm resistive source). The high frequency tone should be at a higher power level than the low frequency tone by approximately 2 dB. The maximum combined power, averaged over the pulse duration, should not exceed +1 dBm. The minimum steady state power of the high frequency tone should not be less than –8 dBm.

When connecting the modem circuit to the PSTN by means of a data access arrangement (DAA) set for permissive mode, the DAA gain is –9 dB. The modem circuit must, therefore, drive the DAA input with +1 dBm of steady state high frequency power and –1 dBm of steady state low frequency power in order to meet all of the listed conditions. Since +0.5 dBm is the maximum undistorted power level for individual tones generated by the modem, the user may need to add gain in front of the DAA during DTMF dialing.

The required duration of the DTMF pulse is 50 ms minimum. By experience, a pulse duration of approximately 95 ms is more reliable. The required interval between DTMF pulses is 45 ms minimum and 3 seconds maximum. Again, by experience, an interdigit delay of approximately 70 ms is preferred.

The remaining requirements of RS-496, relative to DTMF dialing, are not influenced by the host processor. These requirements are all met by the modem's oscillators.

7.2 SETTING OSCILLATOR PARAMETERS

The oscillator frequency and output power are set by the host computer in DSP RAM using the microprocessor bus and diagnostic data routine. For a description of the microprocessor bus and other interface considerations, refer to Sections 2, 3 and 4.

To generate a DTMF tone, place the modem into TONE configuration (CONF = 80h). The user must program the frequencies and the levels of each tone. To set the frequency of tone 1, write a 16-bit hexadecimal number into RAM using RAM access code 21h with AREXx = 0, BRx = 0, DRx = 0, and CRx = 1. When setting the frequency of tone 2, use the same procedure with the RAM access code 22h with AREXx = 0, BRx = 0, DRx = 0, and CRx = 1. Set the power levels of tone 1 by writing a 16-bit hexadecimal number into RAM using RAM access code 22h with AREXx = 0, BRx = 0, DRx = 0, and CRx = 0. The RAM access code for the power level of tone 2 is 23h with AREXx = 0, BRx = 0, DRx = 0, and CRx = 0.

The hexadecimal numbers written into these RAM locations are scaled as follows:

Frequency number = 6.8267 x (desired frequency in Hz) for 9600 Hz sample rate, or

8.192 x (desired frequency in Hz) for 8000 Hz sample rate.

Power number = $18426\ [10^{(Po/20)}]$

Where Po = output power in dBm with a 600 ohm load termination. If terminating with a series 600 ohm resistor into a 600 ohm load, add 6 dB to the output power before using the above equation.

These decimal numbers must be converted to hexadecimal form then stored in RAM (see RAM data write routine).

Hexadecimal numbers for DTMF generation are listed in Table 7-2 (a 9600 Hz sample rate is assumed). Power levels are selected to give the desired output power for each tone (–1 dBm for the high frequency tone and –3 dBm for the low frequency tone if terminated with a series 600 Ω resistor into a 600 Ω load) while compensating for modem filter characteristics.

7.3 DETECTING ANSWER TONE

Frequency detector bit FR1 (08:5) can be used to detect a 2100 Hz answer tone when connection to the remote modem is successful. Bit FR1 goes active (one) when energy above the turn-on threshold is present at 2100 Hz ±25 Hz. At the end of the answer tone, FR1 returns to zero and data transmission can begin.

7.4 COMPLETE CALLING SEQUENCE

A complete calling sequence consists of several steps including modem configuration, telephone number selection, DTMF transmission, and answer tone detection. A sample flow chart for implementing an auto-dialer in host software is illustrated in Figure 7-1.

The auto-dialer routine may be entered at one of two points; either AUTO DIAL or REDIAL. When entering at AUTO DIAL, the host prompts the user to enter a phone number, which is then stored in the phone number buffer. When entering at REDIAL, the routine dials the number previously stored in the phone number buffer and does not issue a user prompt.

Interrupts not required during dialing are disabled to prevent errors in real time delays. Interrupt status is saved to allow restoring these interrupts when dialing is complete. The current modem configuration is saved prior to selecting the DTMF Transmit configuration, then restored at the completion of the auto-dialer routine to allow data transfer.

The commands for off-hook and request coupler cut through are typical of signals required by data access arrangements that may be connected to the modem for switched network operation.

Since the number to be dialed varies in length depending on the requirements of various PBX equipment, domestic telephone companies, and foreign PTTs, the number buffer must allow for numbers of different length. The method used in Figure 7-1 to determine the end of valid bytes in the buffer is zero recognition. After the last digit is entered, the carriage return must place a 00h (ASCII NUL character) in the buffer. All other bytes must be non-NUL ASCII characters. Only numeric characters (ASCII 30 through 39) are printed and dialed. Non-numeric characters are tested for comma and NUL. Comma causes a 2-second pause in dialing to allow for known delays in the telephone network or PBX. NUL ends the dialing portion of the routine and begins the answer tone detection portion. All other characters are ignored.

The answer tone detection logic allows 30 seconds for 2100 Hz recognition. If answer tone is not recognized within this time limit, the call is aborted. If answer tone is recognized, the routine jumps to the data handling software.

Table 7-2. DTMF Parameters

Digit	AREXx	ADDx (Hex)	CRx	BRx	DRx	Value (Hex)
0	0	21	1	0	0	1918
	0	22	1	0	0	23A0
	0	22	0	0	0	65AB
	0	23	0	0	0	7FFF
1	0	21	1	0	0	1296
	0	22	1	0	0	203D
	0	22	0	0	0	65AB
	0	23	0	0	0	7FFF
2	0	21	1	0	0	1296
	0	22	1	0	0	23A0
	0	22	0	0	0	65AB
	0	23	0	0	0	7FFF
3	0	21	1	0	0	1296
	0	22	1	0	0	2763
	0	22	0	0	0	65AB
	0	23	0	0	0	7FFF
4	0	21	1	0	0	1488
	0	22	1	0	0	203D
	0	22	0	0	0	65AB
	0	23	0	0	0	7FFF
5	0	21	1	0	0	1488
	0	22	1	0	0	23A0
	0	22	0	0	0	65AB
	0	23	0	0	0	7FFF
6	0	21	1	0	0	1488
	0	22	1	0	0	2763
	0	22	0	0	0	65AB
	0	23	0	0	0	7FFF
7	0	21	1	0	0	16B8
	0	22	1	0	0	203D
	0	22	0	0	0	65AB
	0	23	0	0	0	7FFF
8	0	21	1	0	0	16B8
	0	22	1	0	0	23A0
	0	22	0	0	0	65AB
	0	23	0	0	0	7FFF
9	0	21	1	0	0	16B8
	0	22	1	0	0	2763
	0	22	0	0	0	65AB
	0	23	0	0	0	7FFF

Table 7-2. DTMF Parameters (Cont'd)

Digit	AREXx	ADDx (Hex)	CRx	BRx	DRx	Value (Hex)
*	0	21	1	0	0	1918
	0	22	1	0	0	203D
	0	22	0	0	0	65AB
	0	23	0	0	0	7FFF
#	0	21	1	0	0	1918
	0	22	1	0	0	2763
	0	22	0	0	0	65AB
	0	23	0	0	0	7FFF
A	0	21	1	0	0	1296
	0	22	1	0	0	2B8C
	0	22	0	0	0	65AB
	0	23	0	0	0	7FFF
B	0	21	1	0	0	1488
	0	22	1	0	0	2B8C
	0	22	0	0	0	65AB
	0	23	0	0	0	7FFF
C	0	21	1	0	0	16B8
	0	22	1	0	0	2B8C
	0	22	0	0	0	65AB
	0	23	0	0	0	7FFF
D	0	21	1	0	0	1918
	0	22	1	0	0	2B8C
	0	22	0	0	0	65AB
	0	23	0	0	0	7FFF

7.5 SINGLE TONE GENERATION

In OEM equipment that combines the features of a modem with those of a telephone handset, the tone generators may be used to generate a caller reassurance tone (or even music) while the caller is kept on hold. To generate a single tone, make sure one of the oscillators is set to zero frequency or zero amplitude while the other oscillator is set to the desired frequency and amplitude. Common parameters for single tone generation are listed in Table 7-3. (A 9600 Hz sample rate is assumed.)

Table 7-3. Common Single Tone Parameters

Parameter	Frequency	Value (Hex)
CED	2100 Hz	3800
CNG	1100 Hz	1D55

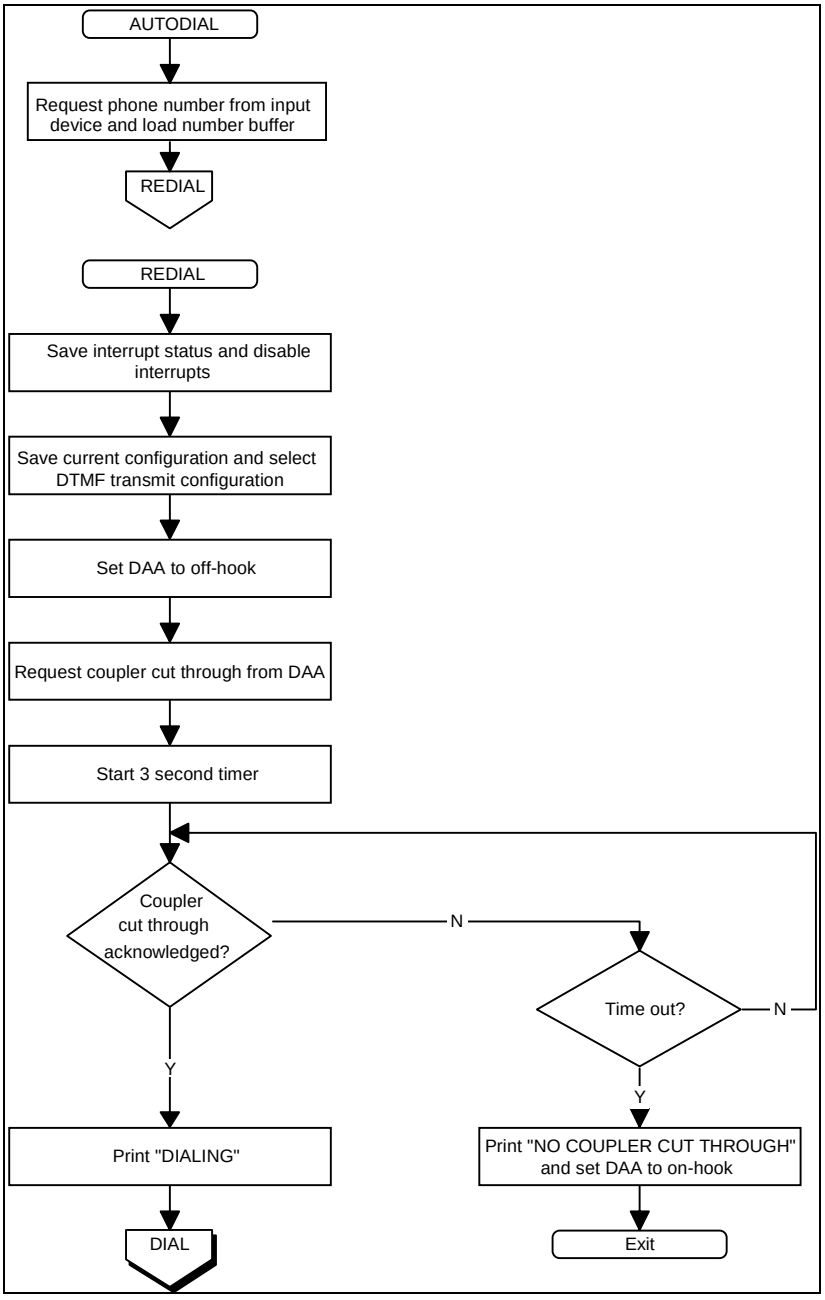

Figure 7-1. Autodialer Flowchart

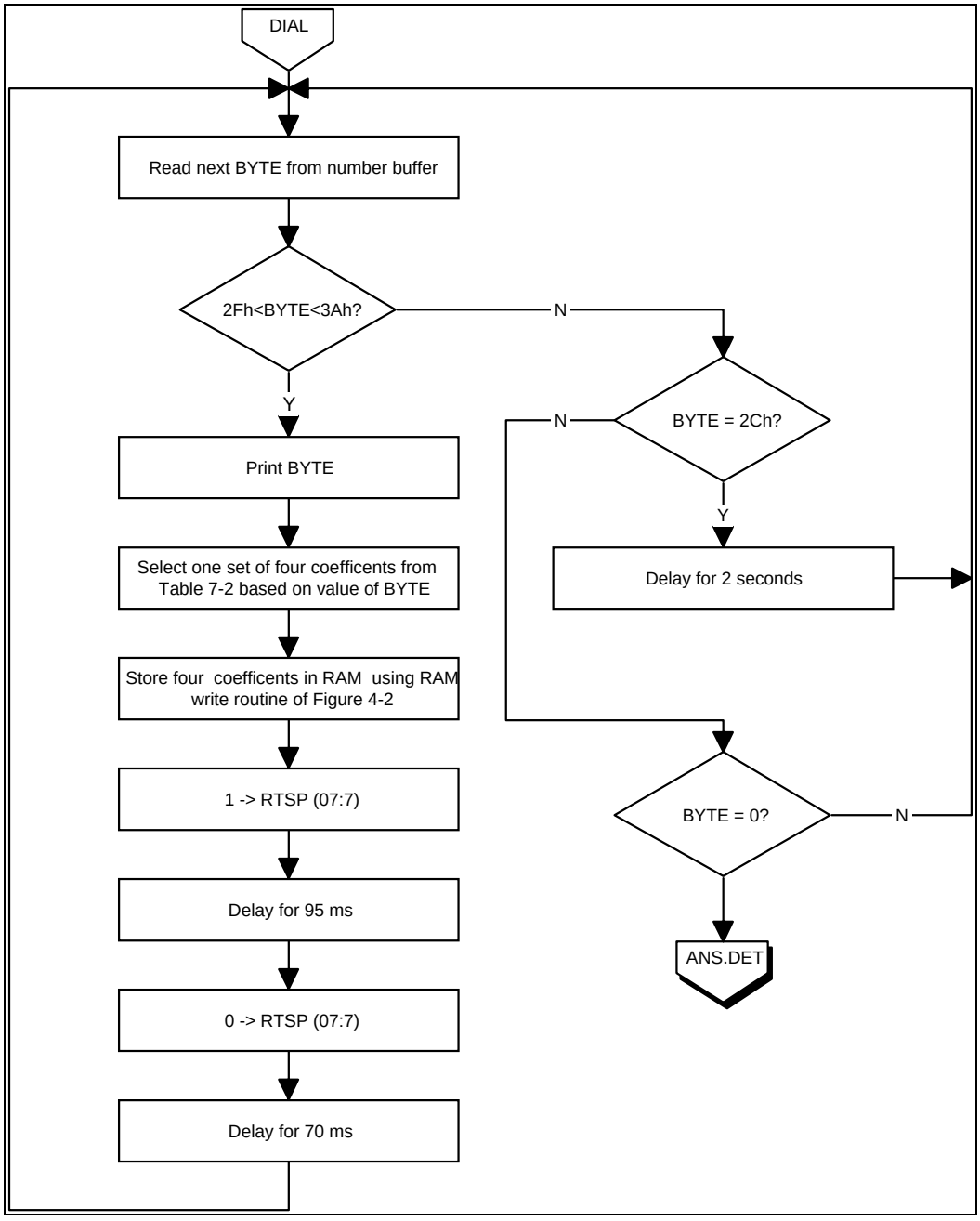

Figure 7-1. Autodialer Flowchart (Cont'd)

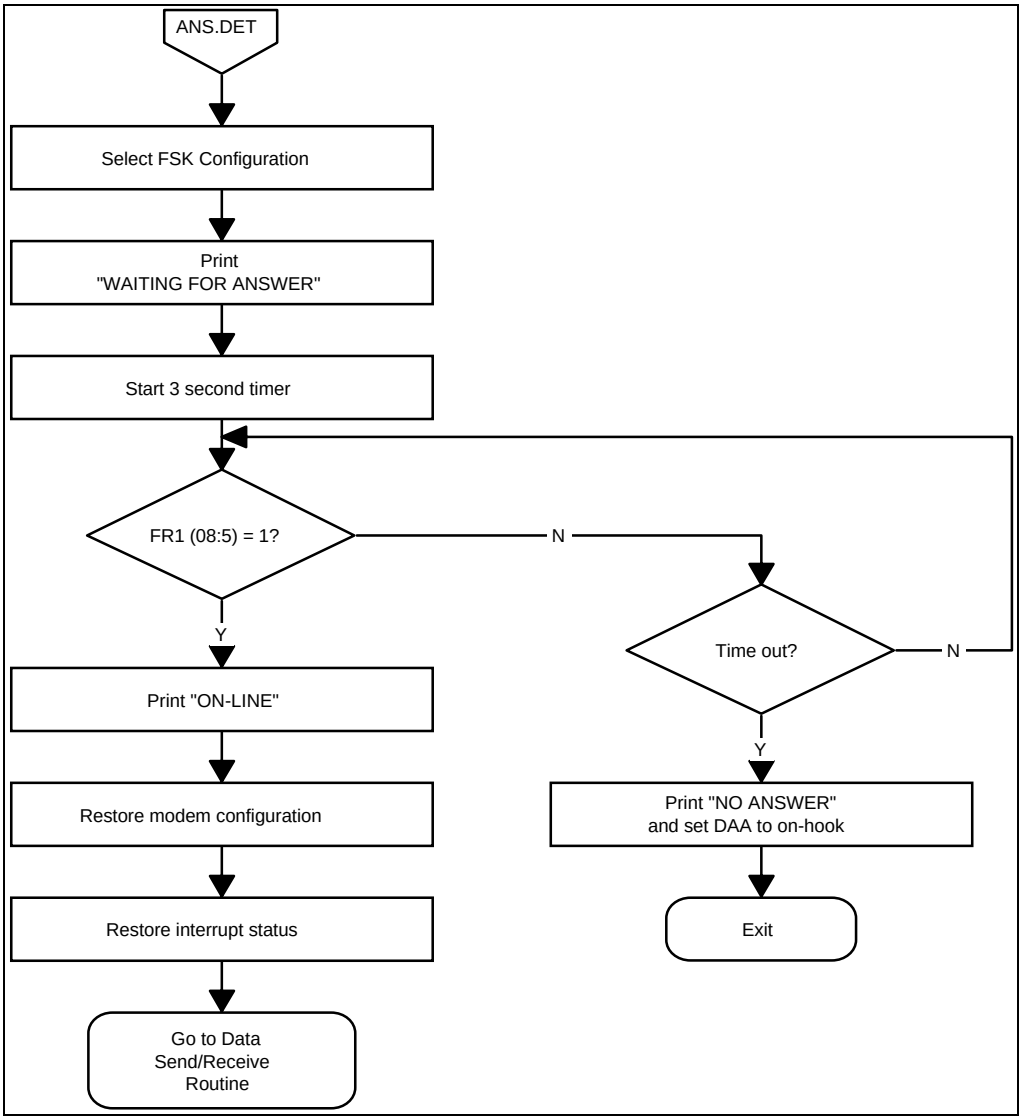

Figure 7-1. Autodialer Flowchart (Cont'd)

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8. VOICE CODEC AND ADPCM AUDIO CODEC MODES WITH ROOM MONITOR

The voice codec compresses voice with near toll quality playback at an average rate of 2.9 kbps (CONF=90h) or at a fixed rate of 4.7 kbps (CONF=98h). An average rate of 2.9 kbps provides 24 minutes of stored voice messages in 4 Mbits of memory. Optional error correction coding allows voice message storage in audio-grade random access memories (ARAM) at an average rate of less than 3.15 kbps or at a fixed rate of 5.0 kbps.

The audio codec compresses audio (music/voice) using an ADPCM algorithm at 24 kbps (CONF=92h) or 32 kbps (CONF=94h) for highest fidelity reproduction.

Available DTMF detect, Type II Caller ID CAS detect, tone detect, and tone transmit functions provide for a complete digital telephone answering machine (DTAM) implementation. DTMF detect (Section 3), Type II Caller ID CAS detect (Section 10), and three tone detectors (Section 6) operate continuously. A local line echo canceller (LEC) is used for improved DTMF and tone detection during voice and audio decoder operations. Dual/single tone transmission is permitted when the decoder is disabled (see Section 4 and control bit RTSP in Table 3-1).

Optional host programmable biquad filters are provided supporting coder pre-filtering and decoder post-filtering (Section 8.6).

The input source for the voice coder, audio coder, DTMF detect, Type II Caller ID CAS detect, and tone detect may be either the PIA or SIA. The output destination for the voice decoder, audio decoder, and dual/single tone transmit may be either the PIA or both the PIA and SIA (see control bit CODECS in Table 3-1).

Room Monitor allows the remote-end user to monitor the local room activity by listening to audio captured by the microphone connected to either the PIA or SIA input. The voice codec, audio codec, DTMF detect, tone detect, Type II Caller ID CAS detect, and tone transmit functions are also available during room monitor operation (Section 8.4).

8.1 VOICE CODER AND ADPCM AUDIO CODER

Coder error correction coding must be enabled for voice coder compression of messages with error correction and disabled for messages compressed without error correction (see control bit HDLC in Table 3-1).

The coder is enabled by setting control bit CDEN (1A:4). The coder output data is transferred from the coder to the host one byte at a time. Each byte is read from DBUFF (see Table 3-1) in response to a modem generated interrupt (see status bit B2A in Table 3-1). The maximum time interval between interrupts is seven sample periods for the voice coder and one sample period for the audio coder. The voice codec time interval is programmable having a default value of three sample periods (see Section 4). Since this parameter is used for both coder and decoder, the host must rewrite the desired interrupt time interval between coder and decoder operations if this value is different from the default value of three sample periods.

The coder output is organized into data blocks. The variable rate voice coder's output is organized into variable length data blocks from 4 to 38 bytes. The fixed rate voice coder's output is organized into fixed length data blocks. Without error correction coding the repeated data block sequence is 35, 36, 36, 36 bytes. With error correction coding the repeated sequence is 37, 38, 37, 38, 38, 37, 38, 38 bytes. The audio coder's output is organized into fixed length blocks of 120 bytes at 32k bps and 90 bytes at 24 kbps.

A data overrun condition will occur if the host does not complete the transfer of the current data block when the next data block is ready for transfer. When an overrun occurs the coder sets status bit VOVUN (17:0). The coder input samples may be discarded and coding suspended. Coding continues after data transfer resumes and the coder resets VOVUN.

For a coder implementation example refer to the flowchart shown in Figure 8-1.

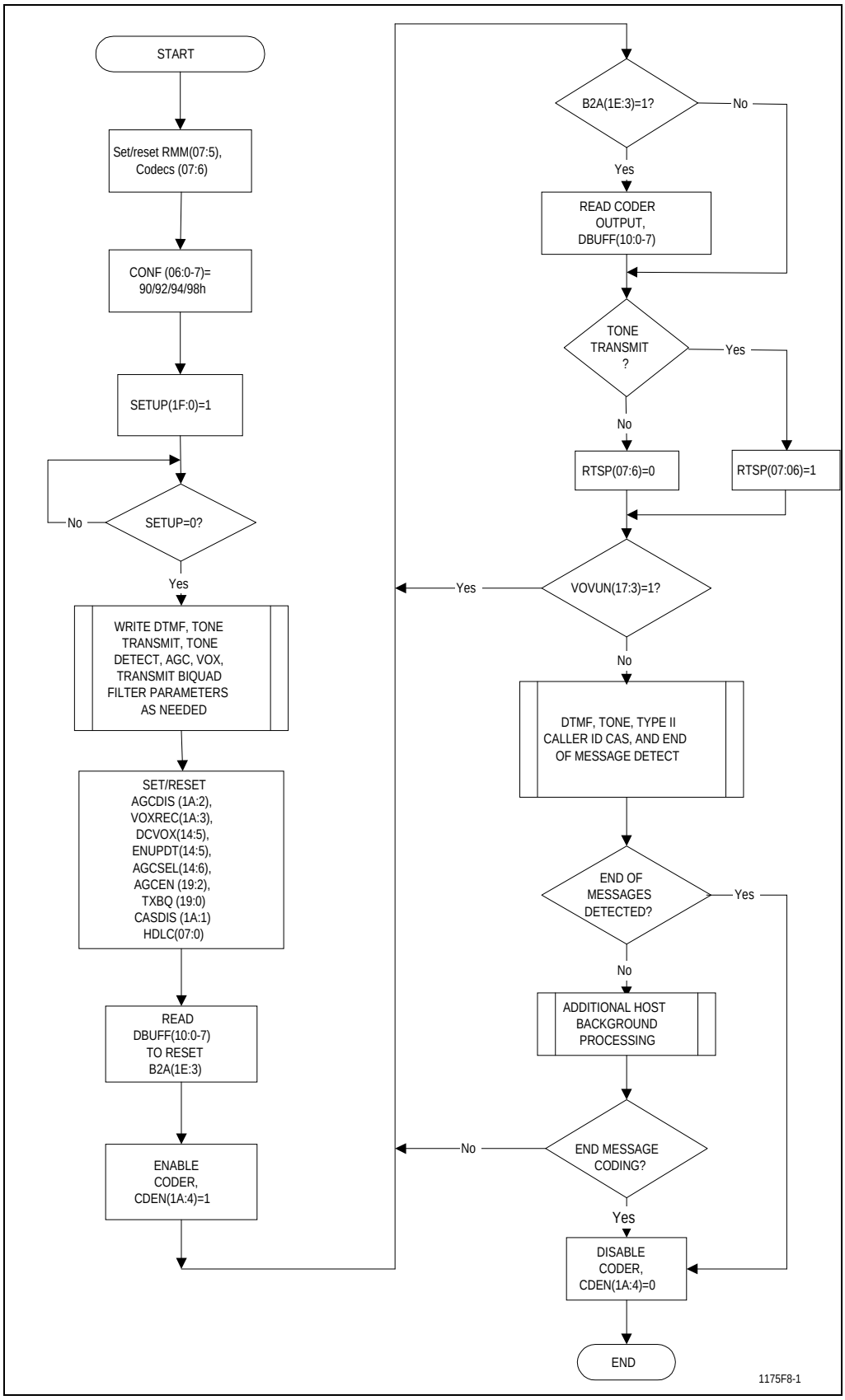


Figure 8-1. Coder Implementation

8.1.1 Voice and Audio Activated Message Encoding

Voice and Audio activated recording maximizes RAM storage efficiency. By setting control bit VOXREC (1A:3) before enabling the coder, the host automatically eliminates beginning of message silence or background noise by delaying encoding until status bit VOX (17:3) is set.

The coder sets status bit VOX when the average energy of the message being encoded exceeds the VOX Turn-On Threshold (see Section 4).

8.1.2 End of Message Detection

Accurate end of message detection improves RAM storage efficiency. The end of the message is reached when the status bit VOX (17:3) remains reset for a period of time monitored by the host. All or part of the coded data stored during this interval may be discarded.

The coder resets status bit VOX when the average energy of the input is less than the VOX Turn-Off Threshold for a period of time greater than the voice and audio coder's energy averaging filter time constant. This time constant is programmable (see Section 4).

8.1.3 Coder Automatic Gain Control (AGC)

The coder AGC achieves uniform playback energy levels by controlling the average energy of the voice or audio input. The host may choose to disable the AGC using control bits AGCDIS (1A:2) and AGCEN (19:2). Disabling the AGC is not recommended unless non-uniform playback energy levels are desired. For each design the AGC parameter values must be adjusted to establish the preferred playback level if different from the default selection. Selected parameter values are to be written to modem RAM using RAM Access after each voice or audio coder mode configuration. Three coder AGC's are provided: Energy AGC, Classifier AGC, and Sample Rate AGC. AGC selection is performed using control bits AGCSEL (14:6), AGCDIS (1A:2), and AGCEN (19:2).

The Energy AGC may be used with either the voice coder or audio coder. Control bit DCVOX (14:5) provides background noise suppression. With DCVOX reset the AGC gain is applied to the input only when status bit VOX (17:3) is set. The four Energy AGC parameters are the Energy Reference Level, Slew Rate, Gain Adaptation Threshold, and Maximum Gain.

The Classifier AGC, optimized for voice input, relies upon a voice classifier to decide when to adapt the gain using an advanced adaptation algorithm. The Classifier AGC, with control bit ENUPDT (14:5) set, compares the average input energy against an energy threshold to decide when to adapt the gain. The voice classifier dependent gain adaptation is preferred with voice input The energy threshold dependent gain adaptation is preferred with audio input. The three Classifier AGC parameters are the Energy Reference Level, Gain Adaptation Threshold, and the Maximum.

A diagram of the Energy AGC and Classifier AGC operation is shown in Figure 8-2. Flowcharts for selecting AGC parameter values are shown in Figure 8-3. Figure 8-7 shows the operating envelope for the Energy AGC and Classifier AGC parameters.

The Sample Rate AGC updates the AGC gainword and applies AGC gain to the sampled input every sample period. The seven Sample Rate AGC parameters are Energy Averaging Filter Coefficients (2), Slew Rate, AGC Switch, Energy Reference Level, Maximum Attenuation, and Maximum Gain. A diagram of the Sample Rate AGC operation is shown in Figure 8-4. Flowcharts for selecting the Sample Rate AGC parameter values are shown in Figure 8-3. Figure 8-5 shows the operating envelope for the Sample Rate AGC parameters. Figure 8-6 shows the sample rate AGC slew characteristics.

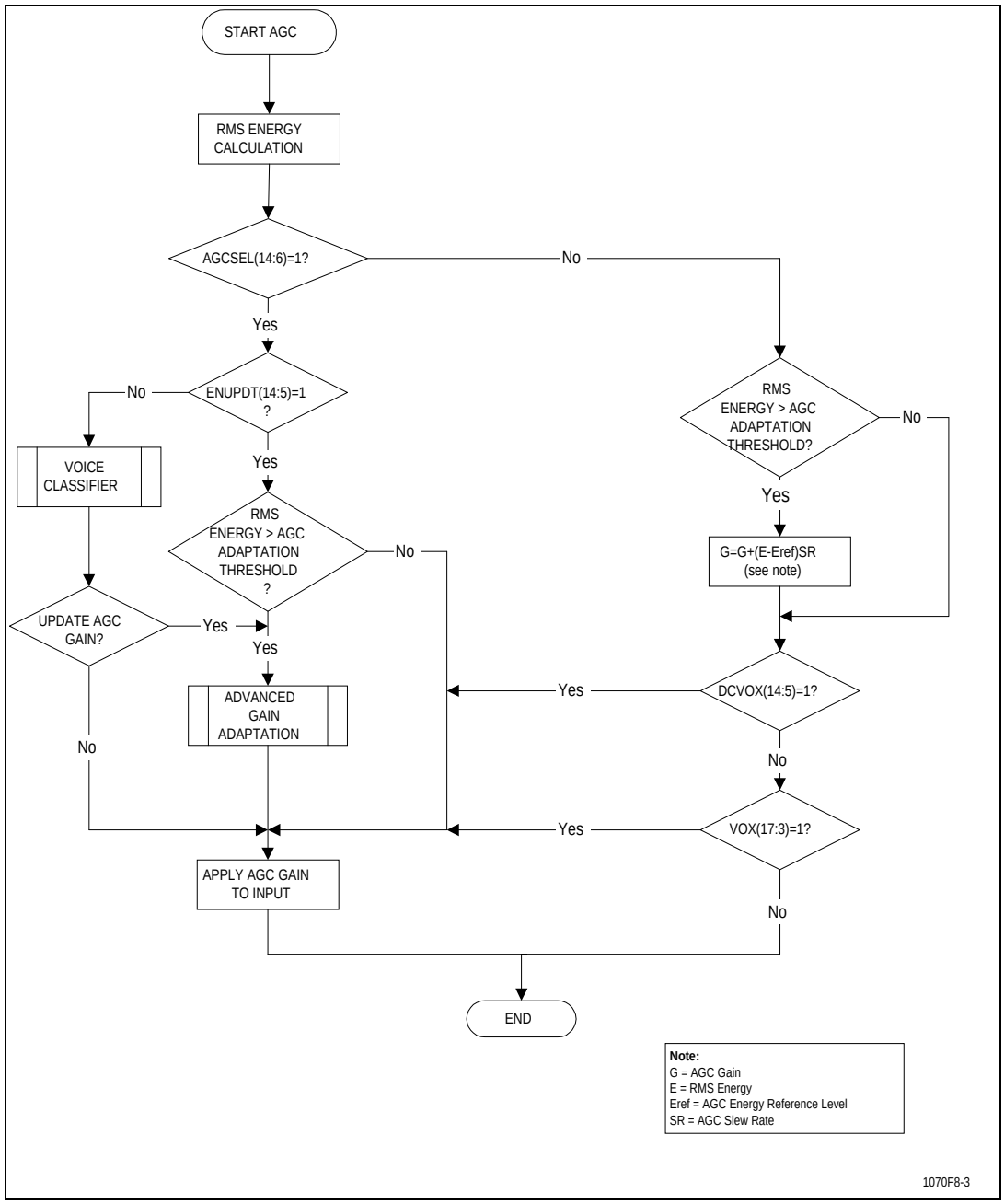


Figure 8-2. Energy AGC and Classifier AGC Operation

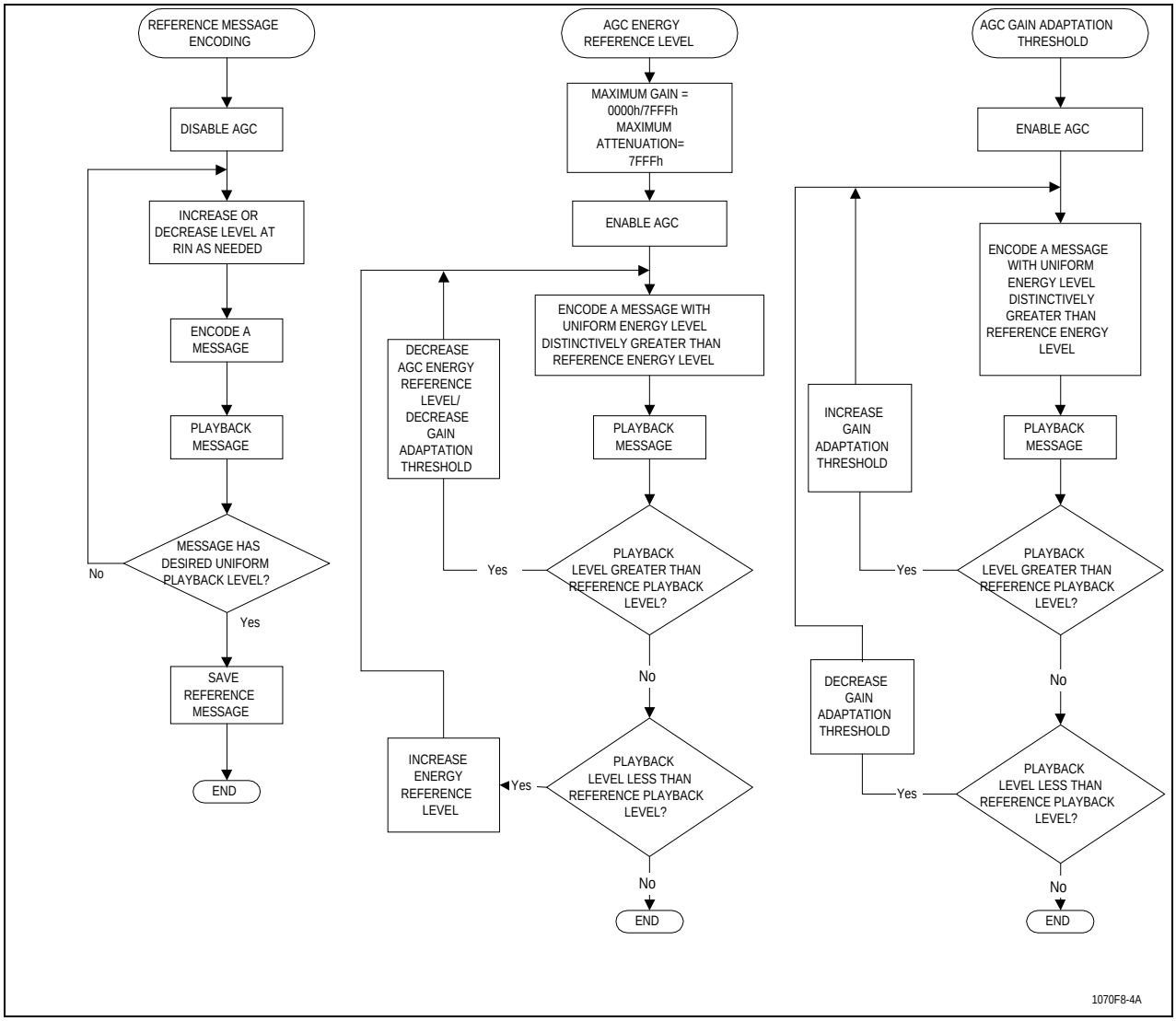


Figure 8-3. AGC Implementation

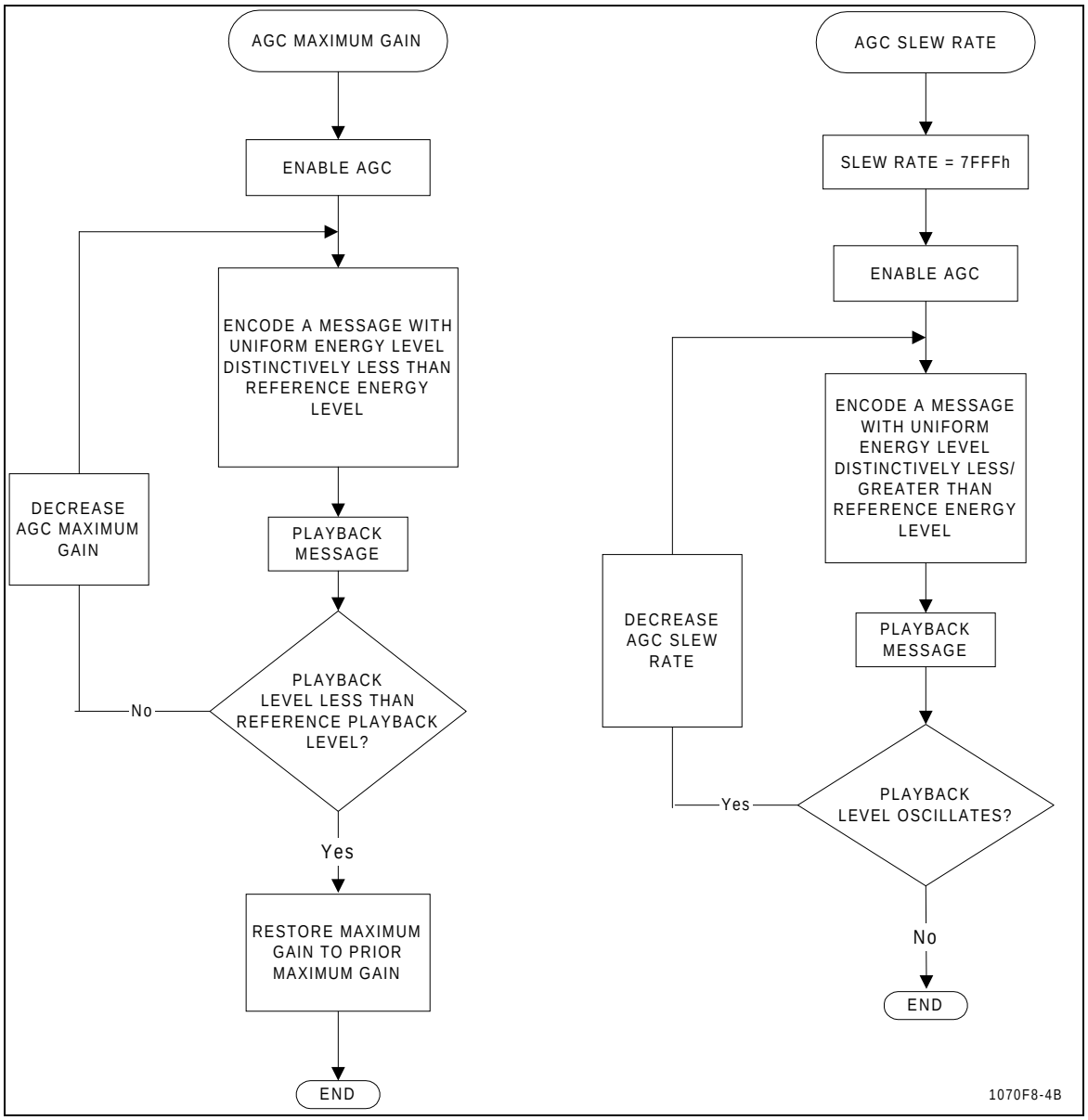


Figure 8-3. AGC Implementation (Cont'd)

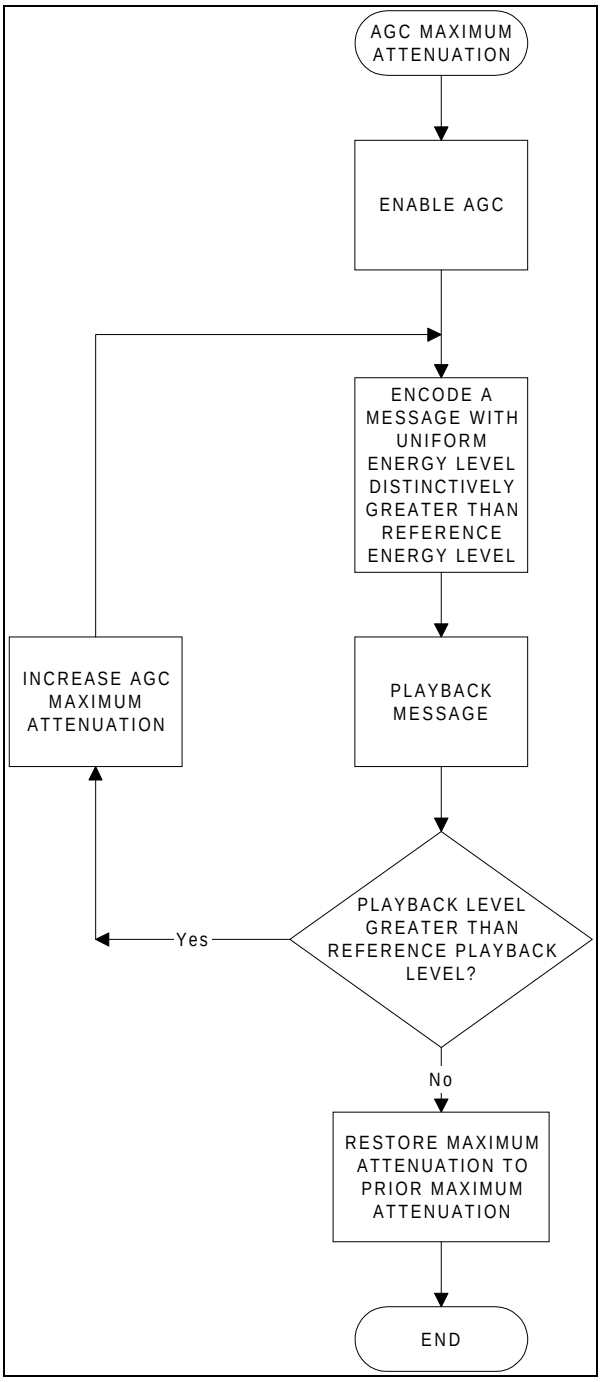


Figure 8-3. AGC Implementation (Cont'd)

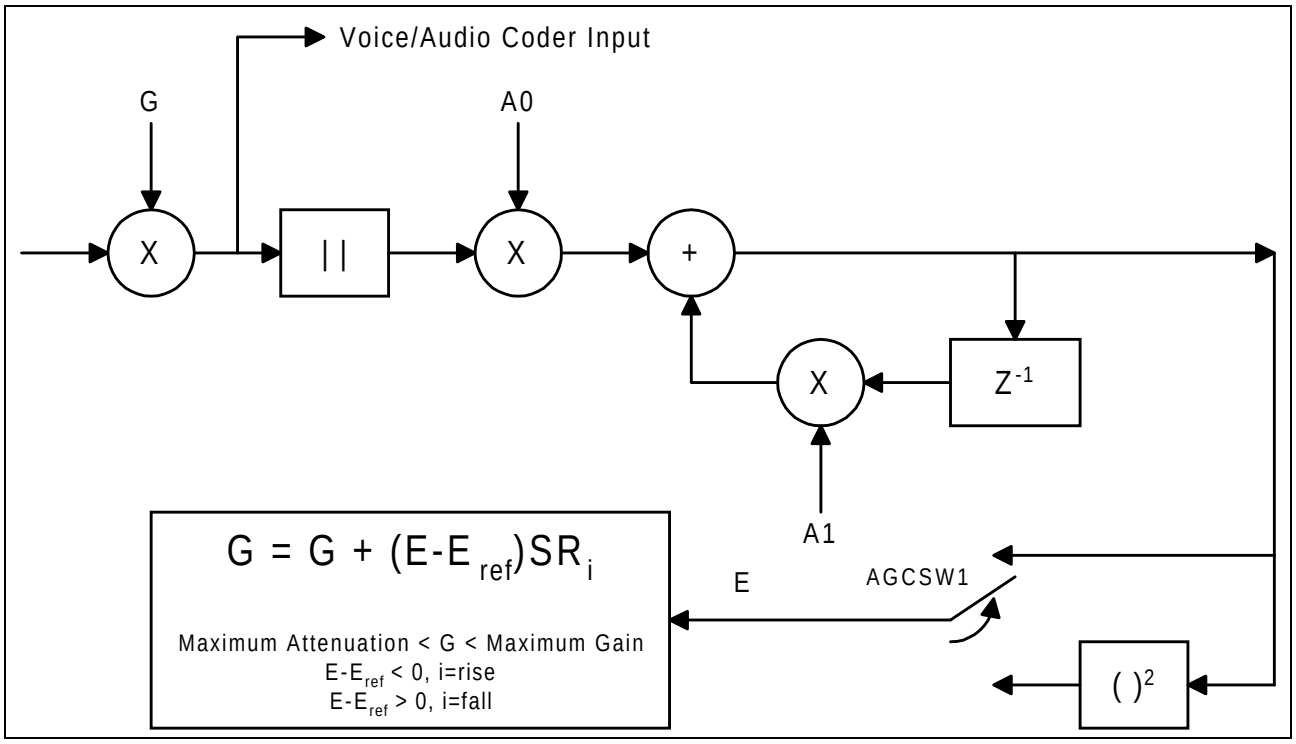


Figure 8-4. Sample Rate AGC Operation

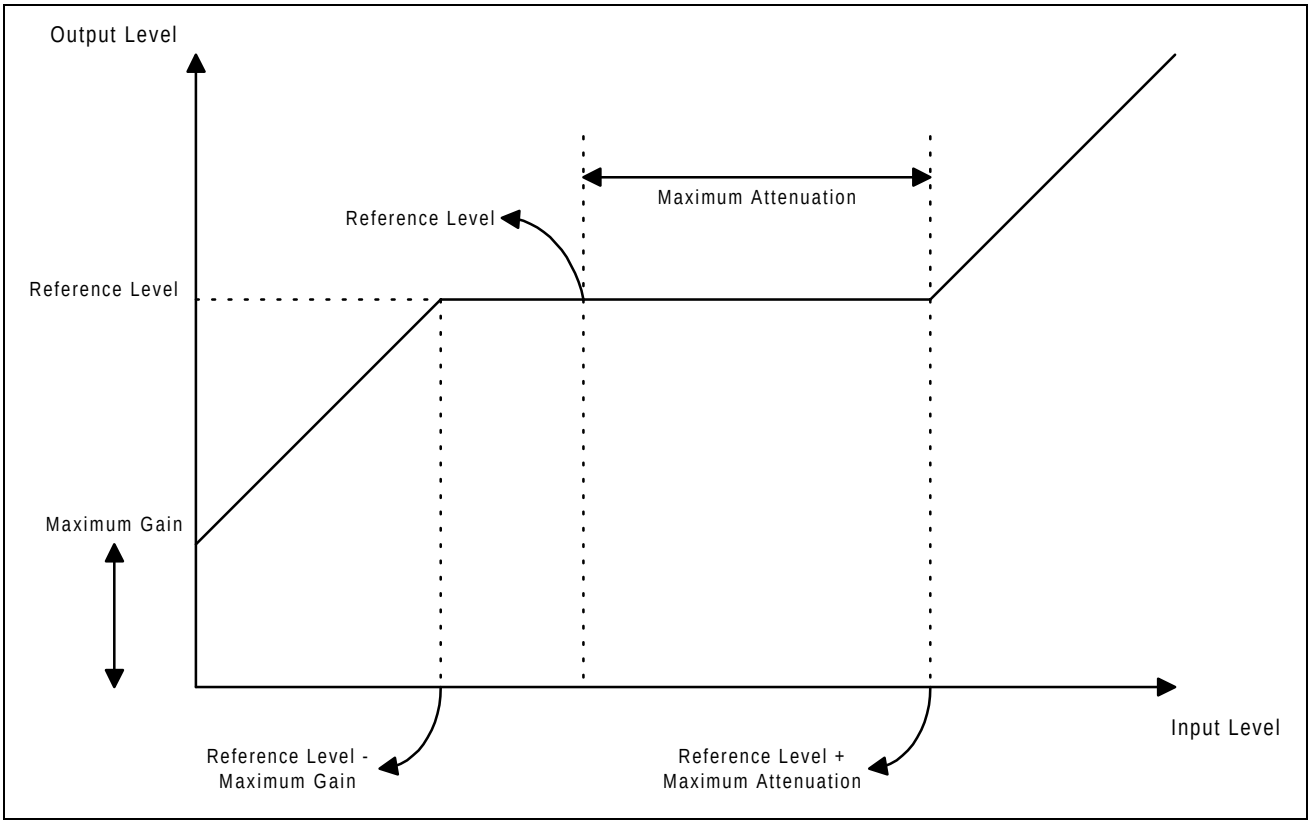


Figure 8-5. Sample Rate AGC Parameters Operating Envelope

8.1.3.1 Energy Reference Level

The Energy Reference Level establishes the desired playback energy level. Input with energy greater than the Energy Reference Level will be attenuated. Input with energy less than the Energy Reference Level will be increased.

8.1.3.2 Gain Adaptation Threshold

The AGC adapts the gain if the average input energy exceeds the Gain Adaptation Threshold. The Gain Adaptation Threshold should be positioned below the Energy Reference Level, above the expected background noise energy level, and above the VOX Turn-On Threshold if the Energy AGC is selected with control bit DCVOX (14:5) reset.

8.1.3.3 Maximum Gain

The Maximum Gain limits the gain applied by the AGC to the input. Input with energy below the Energy Reference Level will receive an energy gain less than or equal to the Maximum Gain.

8.1.3.4 Maximum Attenuation

The Maximum Attenuation limits the attenuation applied by the AGC to the input. Input with energy above the Energy Reference Level will receive an energy attenuation less than or equal to the Maximum Attenuation.

8.1.3.5 Slew Rate

The Slew Rate controls the convergence of the input energy level to the Energy Reference Level. A larger slew rate will allow fast convergence and a smaller slew rate will allow slow convergence. AGC rise time and fall time are dependent upon choice of AGC filter time constant, AGC switch AGCSW1 selection, and slew rates.

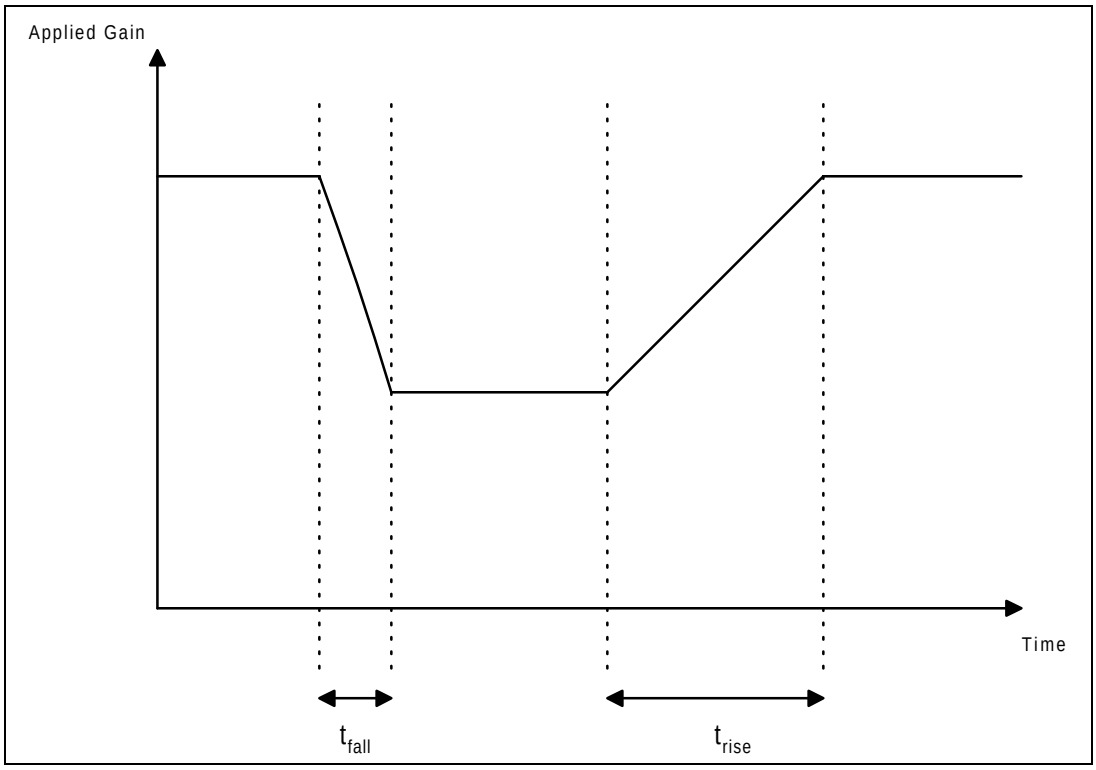


Figure 8-6. Sample Rate AGC Slew Characteristics

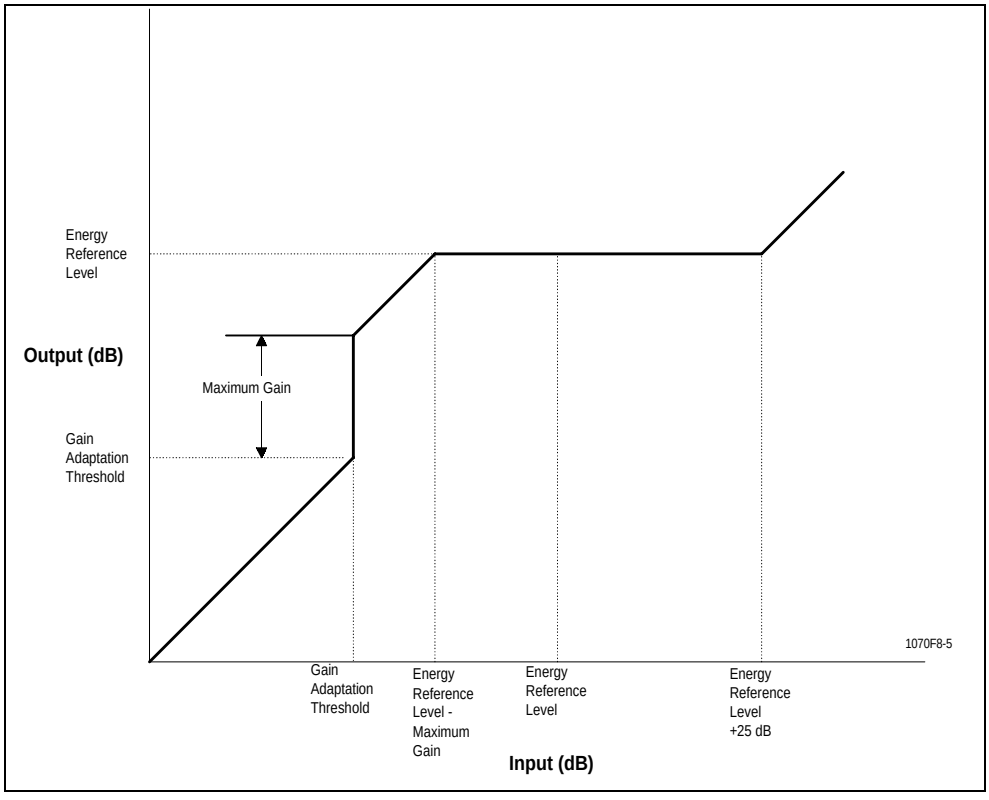


Figure 8-7. Energy and Classifier AGC Parameters Operating Envelope

8.1.3.6 Procedure For AGC Parameter Selection

If the Classifier AGC is selected ignore references to Gain Adaptation Threshold and Slew Rate. If the Classifier AGC is selected and control bit ENUPDT (14:5) set, ignore references to Slew Rate. If the Sample Rate AGC is selected, ignore references to the Gain adaptation Threshold. If the Sample Rate AGC is not selected, ignore references to Maximum Attenuation. Parameter selection should proceed in order from step one through step eight.

1. With the AGC disabled (AGCDIS (1A:2)=1, AGCEN (19:2)=0) encode a 20-second reference message. This reference message is any message having uniform energy that establishes the desired playback level.
2. If Energy AGC or Sample Rate AGC is selected set the Maximum Gain parameter to 0000h. If Classifier AGC is selected set the Maximum Gain parameter to 7FFFh. If Sample Rate AGC is selected, set Maximum Attenuation parameter to 7FFFh.
3. With the AGC enabled (AGCDIS (1A:2)=0, AGCEN (19:2)=0, or AGCDIS (1A:2)=1, AGCEN (19:2)=1) encode a message having uniform energy distinctively greater than the reference message and background noise. Begin message playback and compare the playback level of the message to the playback level of the reference message. If the playback level is less/greater than the playback level of the reference message, increase/decrease the AGC Energy Reference Level. Repeat until playback levels are equal.

   Note: If the message playback level remains distinctively greater than the reference message playback level although the Energy Reference Level has been repeatedly decreased, decrease the Gain Adaptation Threshold until the message playback level decreases and then continue adjusting the Energy Reference Level as needed.
4. With the AGC enabled encode a message having uniform energy distinctively less than the reference message and distinctively greater than the background noise. Begin message playback and compare the playback level of this message to the playback level of the reference message. If the message playback level remains distinctively less than the reference message playback level, slowly decrease the Gain Adaptation Threshold. If the message playback level becomes significantly greater than the reference message playback level, slowly increase the Gain Adaptation Threshold. Repeat until the playback levels are approximately equal.
5. With the AGC enabled encode a message having uniform energy distinctively less than the reference message and distinctively greater than the background noise as was done in step four. Begin message playback and compare the playback level of this message to the playback level of the reference message. Slowly decrease the AGC Maximum Gain. Repeat until the message playback level is less than the reference message playback level. Restore the Maximum Gain parameter to its previous value where the playback levels remained equal.
6. With the AGC enabled, encode a message having uniform energy distinctively greater than the reference message. Begin message playback and compare the playback level of this message to the playback level of the reference message. Slowly decrease the Maximum Attenuation. Repeat until the message playback level is greater than the reference message playback level. Restore the Maximum Attenuation parameter to its previous value.
7. Set the Slew Rate parameter to 7FFFh. With the AGC enabled encode a message having uniform energy distinctively less than the reference message and distinctively greater than the background noise as was done in steps four and five. Begin message playback. If the playback level oscillates reduce the Slew Rate and repeat until there are no oscillations. With the AGC enabled encode a message having uniform energy distinctively greater than the reference message and background noise as was done in step three. Begin message playback. If the playback level oscillates reduce the Slew Rate and repeat until there are no oscillations.
8. AGC parameter selection completed. Save all AGC parameters for later use.

8.1.4 Sample Rate VOX

A sample rate VOX speech detector is shown in Figure 8-8. The average magnitude of the input sample is computed using the absolute value of the input signal or (optionally) using the absolute value of the input signal after applying the computed sample rate AGC gain. The time constant of the average magnitude filter is programmable. Status bit VOXHI (19:3) is set when the average magnitude or (optional) average magnitude squared is greater than the VOXHI turn-on threshold, and VOXHI is reset when less than the VOXHI turn-off threshold. Status bit VOXLO (19:4) is set when the average magnitude or (optional) average magnitude squared is greater than the VOXLO turn-on threshold, and VOXLO is reset when less than the VOXLO turn-off threshold.

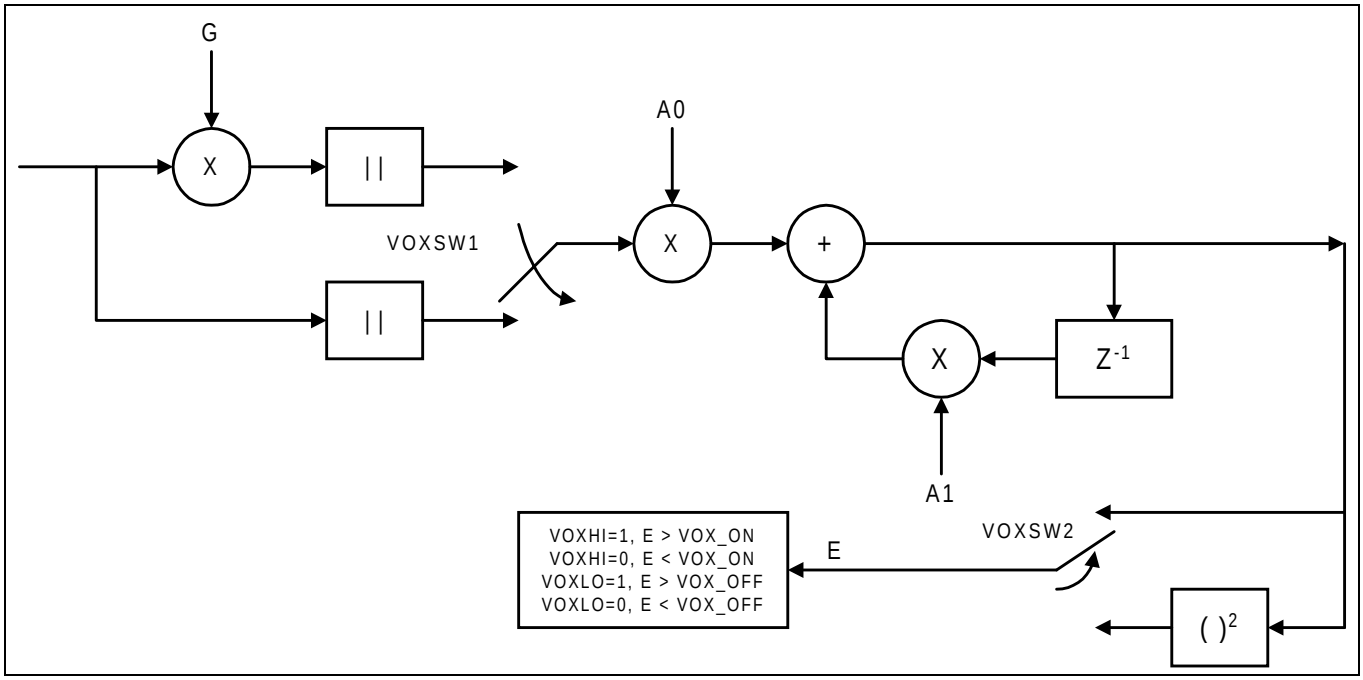


Figure 8-8. Sample Rate VOX

8.2 VOICE DECODER AND ADPCM AUDIO DECODER

Decoder error correction coding must be enabled for voice decoder playback of messages compressed with error correction and disabled for messages compressed without error correction (see control bit HDLC in Table 3-1).

The decoder is enabled by setting control bit DCDEN (1A:5). The decoder input data is transferred from the host to the decoder one byte at a time. Each byte is written to DBUFF (see Table 3-1) in response to a modem generated interrupt (see status bit B2A in Table 3-1). The maximum time interval between interrupts is three sample periods for the voice decoder and one sample period for the audio decoder. The voice codec time interval is programmable having a default value of three sample periods. Since this parameter is used for both the encoder and decoder, the host must rewrite the desired interrupt time interval between encoder and decoder operations if this value is different from the default value of three sample periods.

The host writes blocks of decoder input data to the decoder. The variable rate voice decoder has variable length data blocks from 4 to 38 bytes. The fixed rate voice decoder's input is a repeated sequence of fixed length data blocks. Without error correction coding this sequence is 36, 36, 36, 35 bytes ,and with error correction coding this sequence is 38, 38, 37, 38, 38, 37, 38, 37 bytes. The audio decoder's input is a fixed length data block of 120 bytes at 32 kbps or 90 bytes at 24 kbps.

A data underrun condition will occur when the decoder has completed decoding and playback of its last data block, and the host has not completed transfer of the next data block. When an underrun occurs the decoder sets status bit VOVUN (17:0) and suspends message playback. During this suspension the decoder output samples are forced to zero. To intentionally pause the decoder, the host may choose to halt data transfer to force an underrun condition. Message playback continues after data transfer resumes and the decoder resets VOVUN.

The voice decoder provides the host with four optional pitch synchronous playback speeds. The playback speed may be arbitrarily changed at any time during message playback (see control bits FAST33, FAST50, NORM, and SLOW in Table 3-1). At 33% faster playback speed, the message is played back in 67% of the original recorded message time. At 50% faster playback speed, the message is played back in 50% of the original recorded message time. At normal playback speed, the message is played back in the same period of time as the original recorded message. At 50% slower playback speed, the message is played back in 150% of the original recorded message time.

Skipping forward or backward during message playback within a message and between messages is also supported.

Decoder output volume control provides 2 dB gain when control bit VOLUP (0E:6) is set and 2 dB loss when control bit VOLDWN (0E:5) is set. The decoder resets bits VOLUP and VOLDWN after making the appropriate volume adjustment. The volume control range is 0 dB to -40 dB. The lower limit is programmable.

For decoder implementation refer to flowchart shown in Figure 8-9.

8.2.1 Prevent False ICM DTMF Detection of OGM DTMF

The following procedure prevents false DTMF detection from DTMF signals within the OGM.

Set SETUP(1F:0)=1

Wait for SETUP=0

Set DTMF minimum on-time to 90 ms for recording and playback.

Set encoder output delay interval to 1 sample time between bytes.

Set CDEN(1A:4)=1 to record message.

Loop until message coded.

  While DTDET(1C:6)=1

    Do NOT read coder output (10:0-7)

  Endwhile

Endloop

The maximum amount of DTMF signal coded is 90 ms. The minimum on-time of 90 ms during message record and playback provides immunity to false DTMF detection.

8.2.2 Decoder Skip Forward/Backward During Message Playback

Note: Skip will not work during message playback with speakerphone.

The variable bit rate V24 speech codec encodes speech into 60 ms speech frames.

Since each frame represents 60 ms of encoded speech, it is unlikely that the user will be skipping forward or backward in 60 ms intervals, you will only need to save markers and "first byte bit pointers" for larger multiples of frames.

Use the following steps to perform shuttle playback.

Wait for VOVUN (17:0) = 1

Disable the decoder, DCDEN (1A:5) = 0

Set control bit SKIP (07:1) = 1

Write first byte bit pointer value to 18:0-7

Write 00h to 19:0-7

Enable decoder, DCDEN (1A:5) = 1

In step 4. the first byte bit pointer refers to the first bit location in the first byte of the frame selected.

Example: if the user wants to jump ahead 6 seconds, the decoder data is advanced 100 frames. If the first bit of this frame is bit location 4 (of the first byte in memory containing this frame), then write 18:0-7 = 10h.

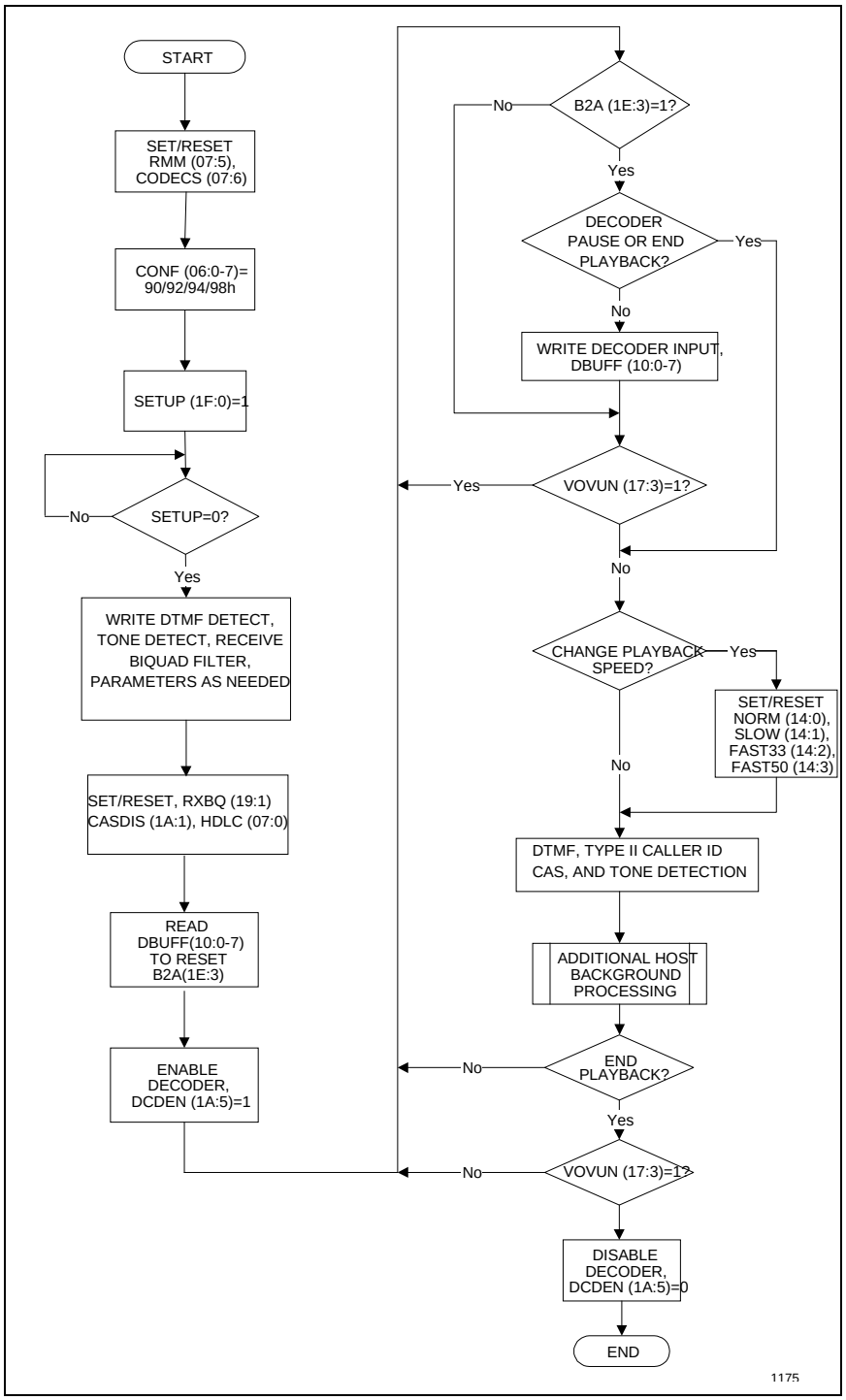


Figure 8-9. Decoder Implementation

8.3 ERROR CORRECTION CODING AND ARAM MESSAGE STORAGE

The host enables voice coder error correction coding by setting control bit HDLC (7:0) prior to message coding. Optional error correction coding allows message storage in audio-grade random access memories (ARAMs) at an average rate of less than 3.15 kbps or at a fixed rate of 5.0 kbps.

ARAMs must be mapped to identify those regions designated unsuitable for storing coded message data. The address of the unsuitable regions require error free storage locations in the ARAM. The size of this address storage location specifies the maximum number of unsuitable regions an ARAM may have.

An unsuitable ARAM segment begins with two bad bits separated by less than 30 good bits and ends at the first bad bit followed by 30 good bits. Unsuitable ARAM regions are defined by these ARAM segments. Examples of unsuitable regions for a 4 Mbit (1M x 4) ARAM are the segment itself, the row of 4096 bits containing the segment, and the entire ARAM containing at least one segment.

Additionally, the number of bad bits in the suitable ARAM region should not exceed 0.1% of the total number of bits in that region. Use of bad bits in excess of 0.1% is not prohibited, but playback quality will gradually decrease as the percentage increases.

8.4 ROOM MONITOR

Room Monitor allows the remote-end user to monitor the local room activity by listening to audio captured by the microphone connected to the SIA input or, in the absence of the SIA, to the PIA input. Room monitor operation is available in all voice codec modes and audio codec modes with DTMF detect, Type II Caller ID CAS detect, tone detect, and tone transmit features. Room Monitor volume control is provided in 6 dB steps to improve monitoring capability (see Section 4). Room monitor without SIA is entered by setting control bit RMM (07:5) prior to mode configuration. Room monitor with the SIA is entered by setting control bits RMM and CODECS (07:6) prior to mode configuration.

With the SIA present, the Line In connects to the PIA, the Line Out connects to the PIA, the Microphone In connects to the SIA, and the Speaker Out connects to the SIA. A typical Room Monitor session with SIA may proceed as follows:

1. The remote-end user is greeted by an outgoing message (OGM) from the voice or audio decoder. The remote-end user sends a known DTMF sequence requesting Room Monitor that is received and detected.
2. Control bits RMM and CODECS are set and voice or ADPCM audio codec configuration selected. An OGM is sent informing the remote-end user of the available options. For example, "Room Monitor Enabled. Press 1 to increase volume. Press 2 to record. Press 3 to end recording. Press 4 to end Room Monitor. <BEEP>."
3. The remote-end user responds, the DTMF signal is detected, and the proper action initiated.

Note: Tone transmission while recording with either the voice encoder or audio encoder will transmit the dual/single tone to both the PIA and SIA output. When not recording, tone transmission will transmit the dual/single tone to the PIA output.

Room Monitor without the SIA requires that the PIA input be switched between the Line In and Microphone In as needed, and the Line Out connected to the PIA output. Switching is accomplished by changing PIA control registers using RAM Access (see Section 4). Since during Room Monitor the PIA input is connected to the Microphone In, there can be no DTMF, Type II Caller ID CAS detect, or tone detection. For DTMF, Type II Caller ID CAS detect, or tone detection to occur, at regular intervals the Room Monitor must be disabled, the PIA input switched to Line In, and the configuration made to voice codec or ADPCM audio codec mode. Now an OGM may be sent and the remote-end user's response detected. A typical Room Monitor session without SIA may proceed as follows:

1. The remote-end user is greeted by an OGM from the voice or audio decoder. The remote-end user sends a DTMF sequence requesting Room Monitor that is received and detected.
2. An OGM is sent requesting the remote-end user to specify a Room Monitor period. For example, "Enter the Room Monitor period. Enter the number of seconds then press *. <BEEP>."
3. The remote-end user responds, the DTMF signals are detected, and a timer is initialized.
4. An OGM is sent informing the remote-end user of the available options. For example, "Room Monitor Enabled. Press 1 to increase volume. Press 2 to record. Press 3 to end recording. Press 4 to end Room Monitor. <BEEP>."
5. The remote-end user responds and the DTMF signal is detected. The PIA input is switched to the Microphone In, control bit RMM is set, and voice or audio codec configuration selected. The timer is started and the proper action initiated.

6. Short tone bursts may be sent at regular intervals to inform the remote-end user that the Room Monitor period is counting down , "<BEEP>".
7. The timer expires. The PIA input is switched to the Line IN, control bit RMM is reset, and voice or ADPCM audio codec configuration selected. Go to step 2 or go to step 4 with timer reinitialized to same Room Monitor period.

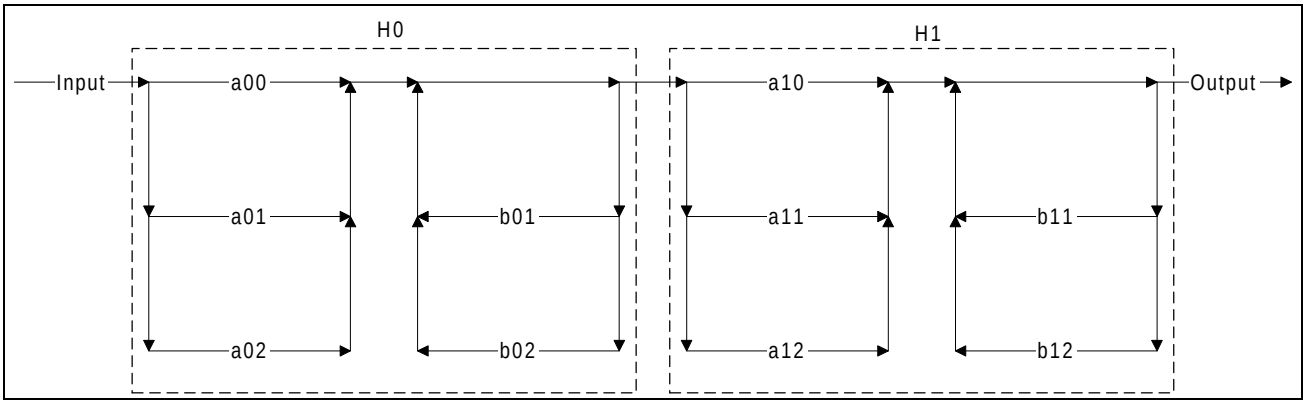
8.5 TONE, DTMF, AND TYPE II CALLER ID CAS DETECTION

The tone detectors operate with 8000 Hz sample rate. All tone detector filters need to be designed with the 8000 Hz sample rate (see Section 6). The DTMF receiver is described in Section 3.2. The Type II Caller ID CAS detector is described in Section 10.9.

8.6 Coder Biquad Pre-Filter and Decoder Biquad Post-Filter

Optional host programmable biquad filters provide support for coder pre-filtering and decoder post-filtering.

8.6.1 Filter Equations



Filter H0 has a transfer function:

$$H_0(z) = \frac{a_{00} + a_{01}z^{-1} + a_{02}z^{-2}}{1 - b_{01}z^{-1} - b_{02}z^{-2}}$$

Filter H1 has a transfer function:

$$H_1(z) = \frac{a_{10} + a_{11}z^{-1} + a_{12}z^{-2}}{1 - b_{11}z^{-1} - b_{12}z^{-2}}$$

8.6.2 Coder TX Biquad Pre-Filter

The coefficients for coder biquad filters are stored in the following RAM locations:

Function	SBRAMx	BRx	CRx	IOx	AREXx	ADDx	Read Reg. No.
Coefficient a_{00}	0	0	1	0	0	64	2,3
Coefficient a_{01}	0	0	1	0	0	66	2,3
Coefficient a_{02}	0	0	1	0	0	65	2,3
Coefficient b_{01}	0	0	1	0	0	68	2,3
Coefficient b_{02}	0	0	1	0	0	67	2,3
Coefficient b_{01}	0	0	1	0	0	6A	2,3
Coefficient b_{02}	0	0	1	0	0	69	2,3
Coefficient a_{10}	0	0	1	0	0	6B	2,3
Coefficient a_{11}	0	0	1	0	0	6D	2,3
Coefficient a_{12}	0	0	1	0	0	6C	2,3
Coefficient b_{11}	0	0	1	0	0	6F	2,3
Coefficient b_{12}	0	0	1	0	0	6E	2,3
Coefficient b_{11}	0	0	1	0	0	71	2,3
Coefficient b_{12}	0	0	1	0	0	70	2,3

All the coefficients must be scaled by a factor of 1/8.

To program the encoder biquad filter, use the following procedure:

1. Use the RAM access procedure to change the value of the coefficients.
2. Set TXBQ (19:0) to enable the coder biquad filter.
3. Set CDEN (1A:4) to enable the coder.

8.6.3 Decoder RX Biquad Post-Filter

The coefficients for decoder biquad filters are stored in the following RAM locations:

Function	SBRAMx	BRx	CRx	IOx	AREXx	ADDx	Read Reg. No.
Coefficient a_{00}	0	0	1	0	1	43	2,3
Coefficient a_{01}	0	0	1	0	1	45	2,3
Coefficient a_{02}	0	0	1	0	1	44	2,3
Coefficient b_{01}	0	0	1	0	1	47	2,3
Coefficient b_{02}	0	0	1	0	1	46	2,3
Coefficient b_{01}	0	0	1	0	1	49	2,3
Coefficient b_{02}	0	0	1	0	1	48	2,3
Coefficient a_{10}	0	0	1	0	1	4A	2,3
Coefficient a_{11}	0	0	1	0	1	4C	2,3
Coefficient a_{12}	0	0	1	0	1	4B	2,3
Coefficient b_{11}	0	0	1	0	1	4E	2,3
Coefficient b_{12}	0	0	1	0	1	4D	2,3
Coefficient b_{11}	0	0	1	0	1	50	2,3
Coefficient b_{12}	0	0	1	0	1	4F	2,3

All the coefficients must be scaled by a factor of 1/8.

In order to program the decoder biquad filter, the following procedure should be followed:

1. Use the RAM access procedure to change the value of the coefficients.
2. Set RXBQ (19:1) to enable the decoder biquad filter.
3. Set DCDEN (1A:5) to enable the decoder.

8.6.4 Default Parameters

Both encoder and decoder biquad filters are disabled by default. They are enabled by setting TXBQ (19:0) and RXBQ (19:1) respectively. These bits can be set or reset before or during the operation of the coder and decoder.

Mnemonic	Memory location	Default Value	Description
TXBQ	19:0	0	0 - disable the encoder biquad filter 1 - enable the encoder biquad filter
RXBQ	19:1	0	0 - disable the decoder biquad filter 1 - enable the decoder biquad filter

The default filter coefficients for both the encoder and the decoder biquad filters are:

Coefficient	Value	Coefficient	Value
a_{00}	1000h	a_{10}	1000h
a_{01}	0000h	a_{11}	0000h
a_{02}	0000h	a_{12}	0000h
b_{01}	0000h	b_{11}	0000h
b_{02}	0000h	b_{12}	0000h

Example:

Assume that the coder biquad filter was designed for the following coefficients

Coefficient	Value	Coefficient	Value
a_{00}	0.8784	a_{10}	0.8764
a_{01}	-1.3882	a_{11}	1.1685
a_{02}	0.5623	a_{12}	0.5344
b_{01}	1.5618	b_{11}	-1.0183
b_{02}	-0.6399	b_{12}	-0.5183

After scaling the coefficients by 1/8th and converting them to fixed-point values, the corresponding values in the RAM locations are:

Coefficient	Value	Coefficient	Value
a_{00}	E0Eh	a_{10}	E06h
a_{01}	E9CAh	a_{11}	12B5h
a_{02}	08FFh	a_{12}	088Dh
b_{01}	18FDh	b_{11}	EFB5h
b_{02}	F5C3h	b_{12}	F7B5h

9. T.30 IMPLEMENTATION

9.1 GENERAL

ITU-T Recommendation T.30 details procedures for facsimile transmission over the PSTN. This standard describes how to initiate, complete, and end a fax transmission. This section describes methods to set up host software to implement T.30.

A block diagram of a Group 3 facsimile machine is shown in Figure 9-1. The MONOFAX modem performs the modulation/demodulation process. The fax machine manufacturer must implement the interface between the modem (T.30), the data compression/decompression (T.4), and the interface to the scanner and printer.

There are five phases (A-E) to the T.30 facsimile protocol. Phase A is the call setup, in which both facsimile machines connect to the line. Phase B is a pre-message procedure which consists of identification and command sections. The actual high speed message transmission occurs during Phase C. This is followed by the post-message procedure or Phase D. Both facsimile machines release the line in Phase E.

Figure 9-2 illustrates a typical Group 3 facsimile procedure. This example on T.30 describes a facsimile call where the calling unit (originate) transmits a documents to a called unit (answer). Phase E is not included in this example since it is the call release and both ends hang up.

9.1.1 Phase A

T.30 specifies that call establishment can be realized one of four ways. The four methods of call establishment are: manual-to-manual, manual-to-automatic, automatic-to-manual, and automatic-to-automatic. Manual corresponds to operator or human intervention while automatic means machine only. The explanation that follows describes an automatic-to-automatic example.

The calling unit, or originating fax, first transmits a calling tone (CNG) to indicate it is a non-speech terminal.

Figure 9-3 describes how to set up the modem to generate a 1100 Hz (CNG) tone. Figure 9-4 describes how to set up the modem to detect a 1100 Hz tone. The called unit, or answering fax, then responds with a called station ID (CED). Figure 9-5 and Figure 9-6 describe how to accomplish this task. The end of Phase A is signified after the called unit sends a 2100 Hz (CED) tone and the calling unit has detected this tone. Some facsimile manufacturers do not configure the modem to detect these tones. In this case, the modem looks for the preamble of flags (see phase B).

9.1.2 Phase B

The pre-message procedure consists of the handshake. One machine sends an identification signal and the other machine responds with a command signal. A training check is sent at a high speed and the receiving machine informs the transmitting machine if the training check was successful. This usually occurs at V.21 300 bps Frequency Shift Keying (FSK) modulation in HDLC format.

HDLC stands for High level Data Link Control. It is a standard procedure used for data communications. HDLC is a bit-oriented protocol (normally used in synchronous communications) that defines how the data being sent over the data link is organized and arranged.

When using the HDLC protocol, the data is transmitted via frames. These frames organize the data into a format specified by an ISO (International Standards Organization) standard that enables the transmitting and receiving station to synchronize with each other. Figure 9-7 illustrates the HDLC frame structure used for the facsimile protocol.

The preamble is a series of HDLC Flags for one second ±15%. The purpose of the 7E flags is to condition the line. The flag sequence defines the beginning and ending of a frame. The address field is required to provide identification for multi-point addressing. For PSTN the format is 11111111. The control field's purpose is to provide the capability of encoding the commands and responses. The format is 1100X000 (X=0 non-final frame; X=1 final frame).

The HDLC information field provides the specific information for the control and message interchange between the two stations. In the fax protocol the format for the information field consists of two parts, the Facsimile Control Field (FCF) and the Facsimile Information Field (FIF).

The FCF contains information regarding the type of information being exchanged and the position in the overall sequence. The acronyms, functions, and format for FCF commands are defined in the T.30 Recommendation. The FIF contains additional information which further clarifies the facsimile procedure. Some examples of some information communicated with the FIF are: group capability, data rate, vertical resolution, coding scheme, recording width, recording length, and minimum scan line time.

The Frame Check Sequence (FCS) follows the FIF. The modem automatically generates the FCS or Cyclic Redundancy Check (CRC). The frame ends with an ending 7E flag. It is recommended that more than one ending flag be transmitted.

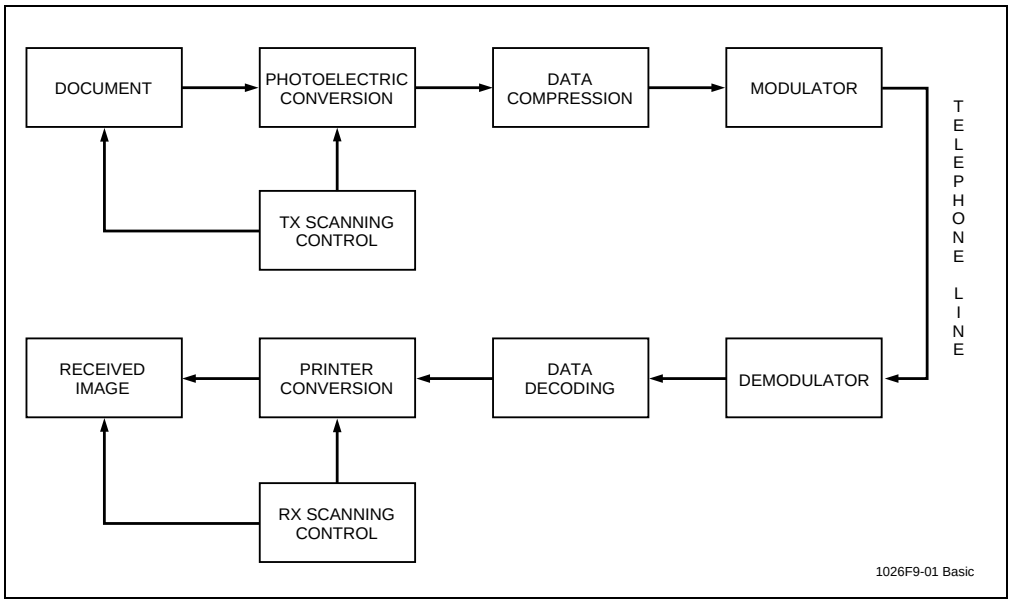


Figure 9-1. Basic Block Diagram of G3 Facsimile

CALLING UNIT	CALLED UNIT	
CNG PHASE A	CED	CALLING TONE: 1100 Hz, 0.5S ON/3S OFF INDICATE NON-SPEECH TERMINAL CALLED STATION ID: 2100 Hz, 2.6S <ON <4S
DCS TCF PHASE B	DIS CFR	DIGITAL ID SIGNAL: 300 BPS FSK, HDLC FORMAT DIGITAL COMMAND SIGNAL: 300 BPS FSK, HDLC FORMAT TRAINING CHECK: HIGH SPEED TRAIN FOLLOWED BY 1.5S OF ZEROS CONFIRMATION TO RECEIVE: 300 BPS FSK, HDLC FORMAT
MESS PHASE C		TRANSMITS DOCUMENT
EOM PHASE D	MCF	END OF MESSAGE: 300 BPS FSK, HDLC FORMAT EOP, MPS OR PRI-Q MAY BE SENT MESSAGE CONFIRMATION: 300 BPS, HDLC FORMAT POST-MESSAGE RESPONSE OF RTP, RTN, PIP OR PIN MAY BE SENT

1026F8-02 G3

Figure 9-2. G3 Facsimile Procedure

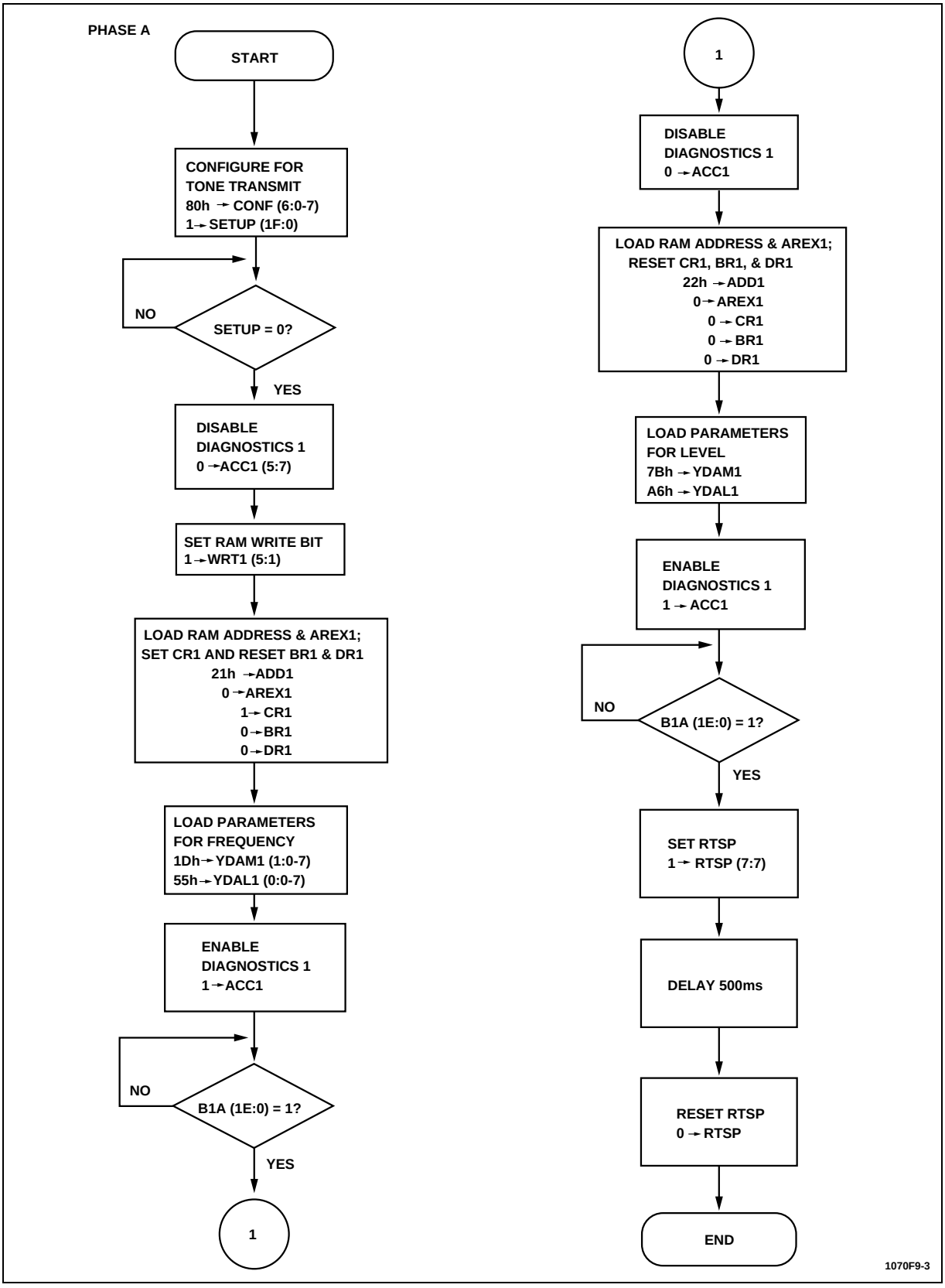


Figure 9-3. Transmit Calling Tone (CNG) (1100 Hz)

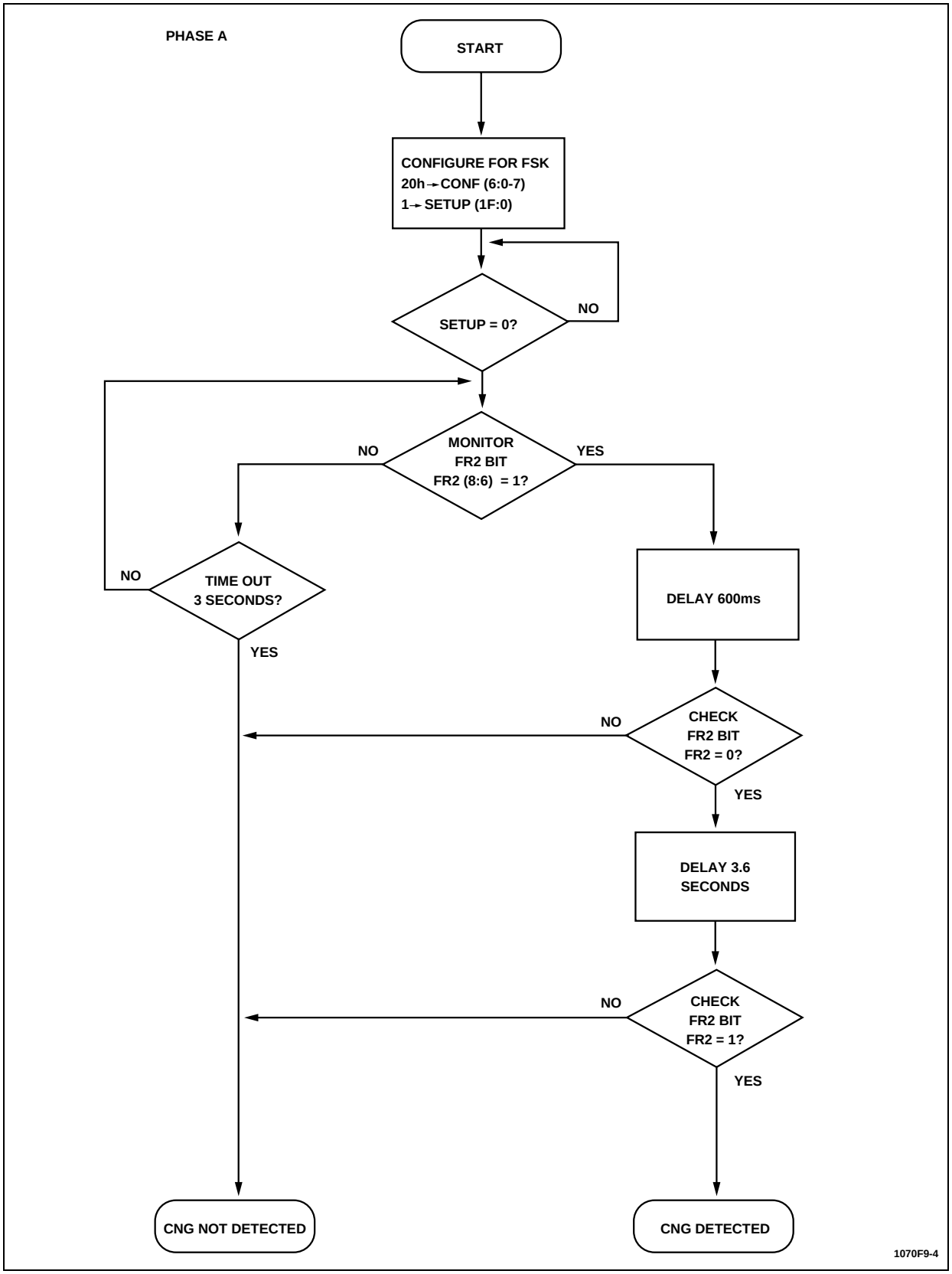


Figure 9-4. Detecting CNG Tone (1100 Hz)

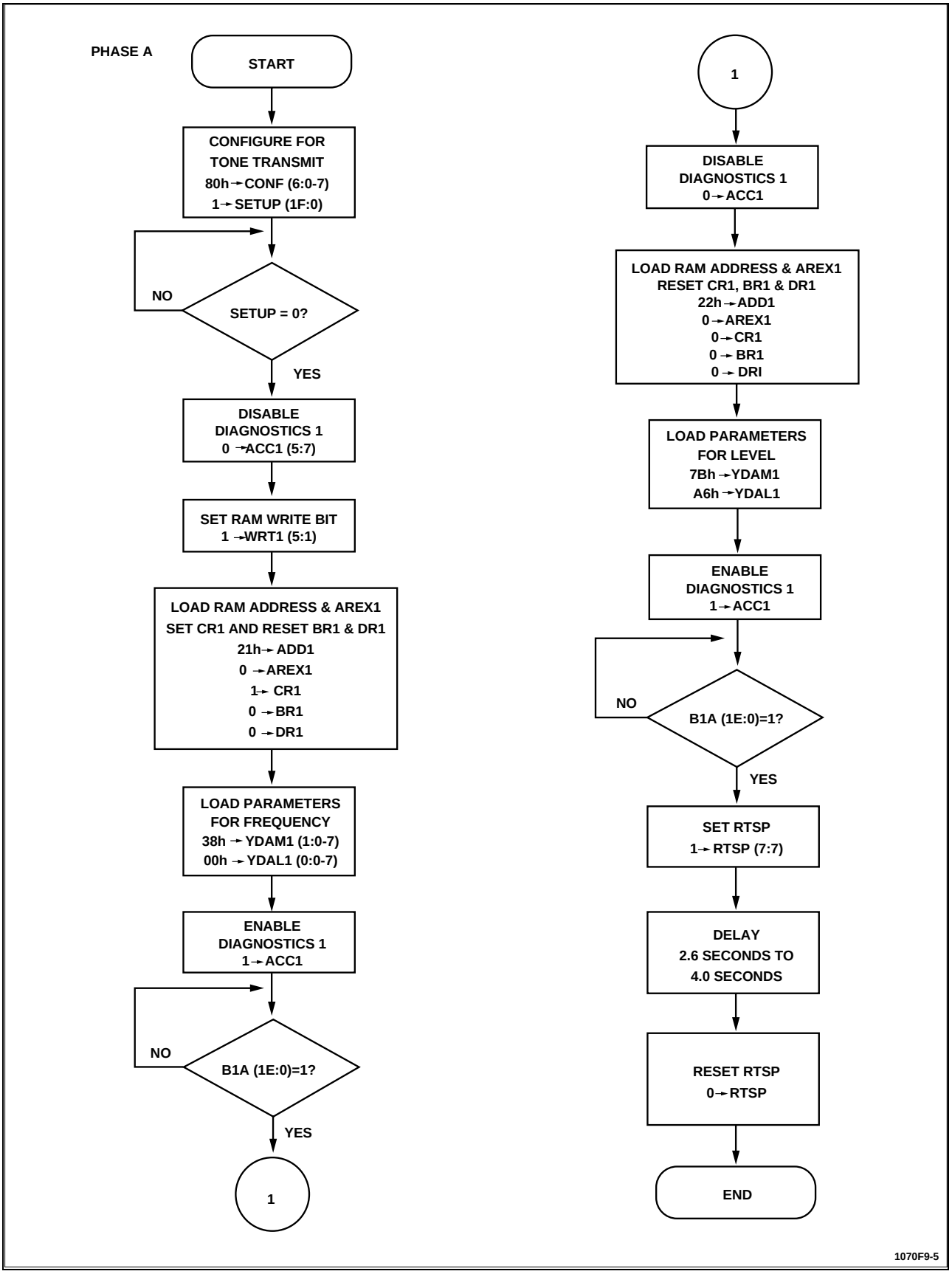


Figure 9-5. Transmit Called Tone (CED) (2100 Hz)

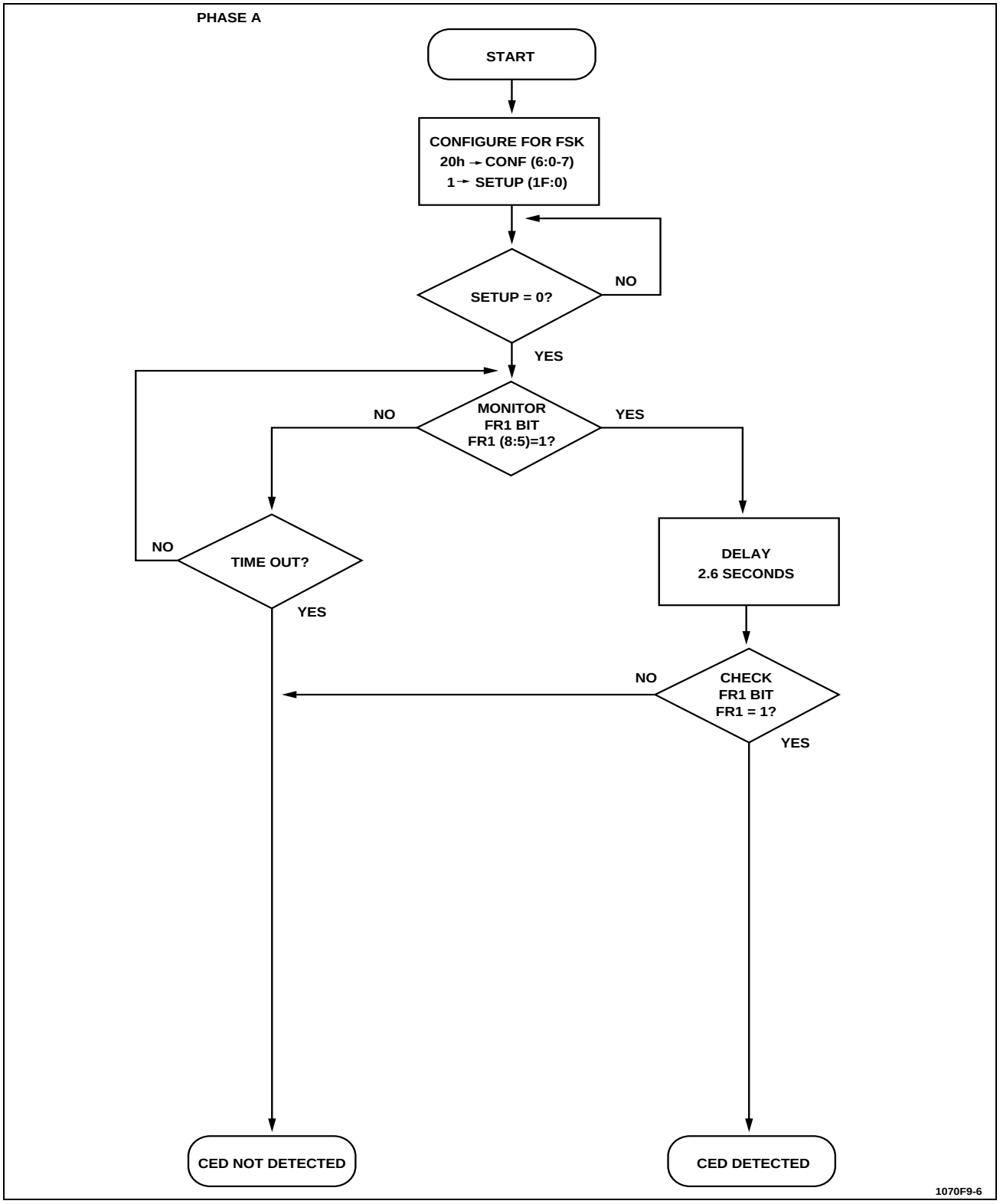


Figure 9-6. Detecting CED Tone (2100 Hz)

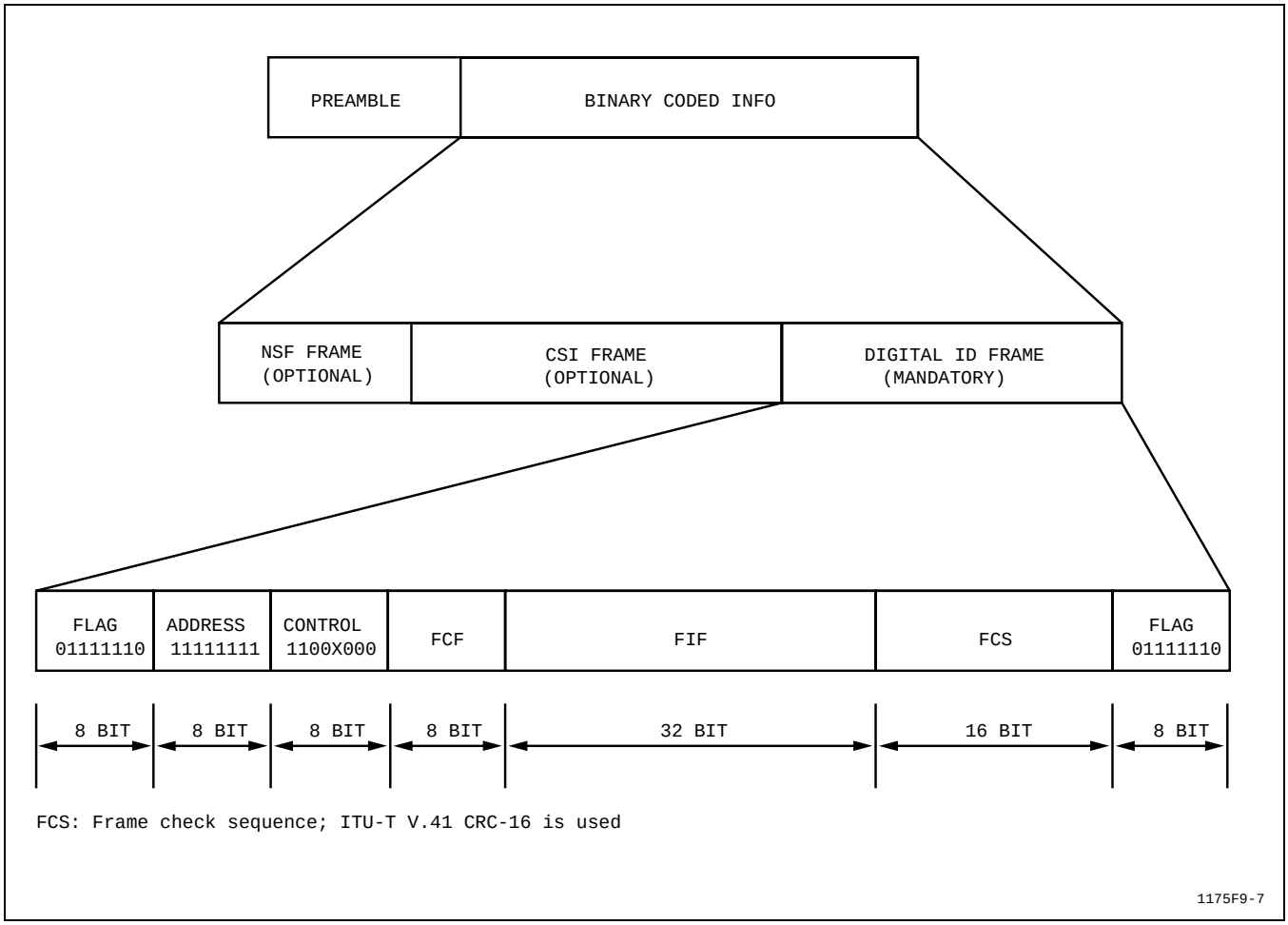


Figure 9-7. HDLC Frame Structure

After the modem has been configured for FSK, the Digital Identification Signal (DIS) is transmitted by the called unit. The DIS informs the calling unit about the called unit's capabilities such as group capability (G1, G2, G3), data rate, vertical resolution, coding scheme (Modified Huffman, Modified Read), recording width, recording length, and minimum scan line time. The calling unit then responds with a Digital Command Signal (DCS) which informs the called unit which options are chosen to complete this facsimile call.

After the DCS is transmitted, both the calling unit and the called unit set up for the high speed configuration that was chosen and transmitted via the DCS. A Training Check (TCF) is transmitted by the calling unit to verify training and give an indication of channel acceptability for the selected data rate. The TCF consists of a series of zeros for 1.5 seconds ±10%. Since the called unit knows it will be receiving 1.5 seconds of zeros, the host can make a decision whether the line is good enough at the chosen data rate or fallback to a slower speed.

After completing the TCF, the calling unit and the called unit re-configures for FSK, HDLC format. The called unit then transmits either a Confirmation to Receive (CFR) or a Failure To Train (FTT). The CFR is a response informing the calling unit of a successful pre-message procedure completion. A FTT informs the calling unit that the training signal was rejected and requests re-training. If a FTT is received by the calling unit, the fax protocol jumps back to the transition of DCS and continues until finally a CFR is received or the calling unit host decides to terminate the call.

The fallback criterion based upon the modem performance information during TCF reception, for example, may consist of monitoring the number of bit errors or EQM number. If EQM is to be used as a fallback criterion for an acceptable BER performance, the minimum metric EQM number should be used for V.17/V.33 modes and the hard decision EQM number should be used for V.29 and V.27 ter modes (see Table 4-1 for RAM access codes and Section 4 for scaling information). Refer to the EQM and BER vs. S/N charts in Section 0 for a guideline on EQM numbers. The EQM numbers shown in the charts are the decimal equivalent to the 16-bit hexadecimal numbers divided by 256.

During TCF, EQMs that represent acceptable BERs can be used to determine whether or not to fallback. If a fallback is necessary, EQM can be used to choose the appropriate fallback mode for a desired BER.

9.1.3 Phase C

Phase C occurs after both facsimile machines have set up for the high speed configuration decided upon in phase B. The T.30 Error Correction Mode is addressed in a following section. This high speed message information is usually compressed data using a Modified Huffman (MH) or Modified Read (MR) algorithm. The host processor must perform the MH or MR compression before loading the data into the modem. On the receive end, the host processor must perform the MH or MR decompression.

The start of phase C is denoted by an End Of Line (EOL) 8-bit code. The data follows this first EOL character until the end of the line. Another EOL character is transmitted to indicate a new line. A minimum transmission time of a total coded scan line is measured from the beginning of the EOL to the beginning of the following EOL. If the transmitted data requires less time than the minimum transmission time, fill bits must be transmitted. Six consecutive EOL character constitute a Return To Control (RTC) command meaning end of document transmission. Figure 9-8 illustrates the phase C format.

9.1.4 Phase D

The post-message phase D procedure uses FSK and HDLC format. The calling station will typically send an End Of Message (EOM) signal. This FCF command (EOM) informs the called station that this is the end of the page and return to Phase B. A Multi-Page Signaling (MPS) or End Of Procedure (EOP) signal may be sent instead of EOM. The MPS signal informs the called unit that there are more pages in this facsimile transmission. EOP signals the end of the facsimile transmission. Procedure Interrupt-EOM (PRI-EOM), Procedure Interrupt-MPS (PRI-MPS), and Procedure Interrupt-EOP (PRI-EOP) indicate the same as EOM, MPS, and EOP, respectively, with the additional optional capability of requesting operator intervention. If operator intervention is required, further facsimile procedures commence at the beginning of phase B.

The called station might respond to an EOM, MPS, or EOP signal with a Message Confirmation (MCF) command. This FCF command indicates to the calling unit that the complete message was received. One of the following FCF commands may be sent instead of the MCF: Re-Train Positive (RTP), Re-Train Negative (RTN), Procedure Interrupt Positive (PIP), or Procedure Interrupt Negative (PIN). RTP indicates that a complete message has been received and that additional messages may follow after retransmission of TCF and CFR. RTN indicates that the previous message has not been satisfactorily received, however, further receptions may be possible provided there is a retransmission of TCF and CFR. PIP and PIN indicate that the previous message was received satisfactorily or not satisfactorily, respectively, and operator intervention is required for further transmissions.

9.1.5 Phase E

Call Release, or phase E, occurs after the last post-message signal of the procedure or under certain conditions such as a time-out, procedural interrupt, or a Disconnect (DCN) command. The DCN command indicates the initiation of phase E. This command requires no response.

9.1.6 Flowcharts

Figure 9-9 through Figure 9-15 illustrate how to implement certain phase B procedures. The examples show how the modem can be set up using the internal HDLC framing capabilities.

Figure 9-9 describes how to transmit FSK/HDLC signals such as DIS, DCS, DTC, CFR, FTT, etc. Three subroutines are called out: the low speed configuration, the transmit preamble, and interrupt-driven transmit routine. A Programmable Interrupt set-up is required in the receiver to determine if it is the end of the frame and if the frame was received correctly. See Figure 9-10 for setup instructions. The Low Speed Configuration subroutine is shown on Figure 9-11. Since the HDLC function is being used, the parallel data mode is enabled. The Transmit Preamble routine is shown on Figure 9-12. When the modem is configured in HDLC mode by setting RTSP, the modem will automatically transmit flags. The Interrupt-Driven Transmit routine is illustrated in Figure 9-13.

The hardware IRQ1# pin must be monitored for interrupts. The IRQ1# pin will become active (go low) when the modem is ready for a byte of data. This data should be loaded into the Data Buffer Register, DBUFF. When the IRQ1# returns low, the modem is ready for the next byte of data. Alternately, IRQ2# can be used.

Figure 9-14 describes how to receive FSK/HDLC signals. The Interrupt-Driven Low Speed Receive routine is shown on Figure 9-15.

After IRQ1# is low, the Buffer 2 Available (B2A) bit is polled to determine if the next byte must be read by the host. If B2A is a 0, the Programmable Interrupt Request (PIREQ) bit is polled to determine if one of the programmable interrupt bits caused the interrupt. If Abort/Idle (ABIDL) is a 1, then an abort or idle sequence is being received. If ABIDL is a 0, then a Return from Subroutine is executed and the End of Frame bit is checked to see if it is the end of the frame. The Cyclic Redundancy Check (CRC) bit is looked at to determine if the current frame was received correctly. Figure 9-16 shows how to re-configure the modem to a high speed configuration. This procedure will be used again when entering phase C. Figure 9-17 describes how to transmit the TCF or one second of zeros. Figure 9-18 describes the High Speed Message Transmission. This procedure is similar to the Low Speed Message Transmission. The High Speed Configuration is located at Figure 9-16.

The High Speed Interrupt-Driven Transmit routine is in Figure 9-19. This is also similar to the low speed procedure.

The High Speed Message Reception procedure is illustrated in Figure 9-20. The High Speed Interrupt-Driven Receive subroutine is in Figure 9-21. Included in the High Speed Message Reception procedure is an optional Ensure Valid Train subroutine (Figure 9-22). This procedure is recommended to ensure that a valid training sequence is accomplished when noise is above the RLSD turn-on threshold.

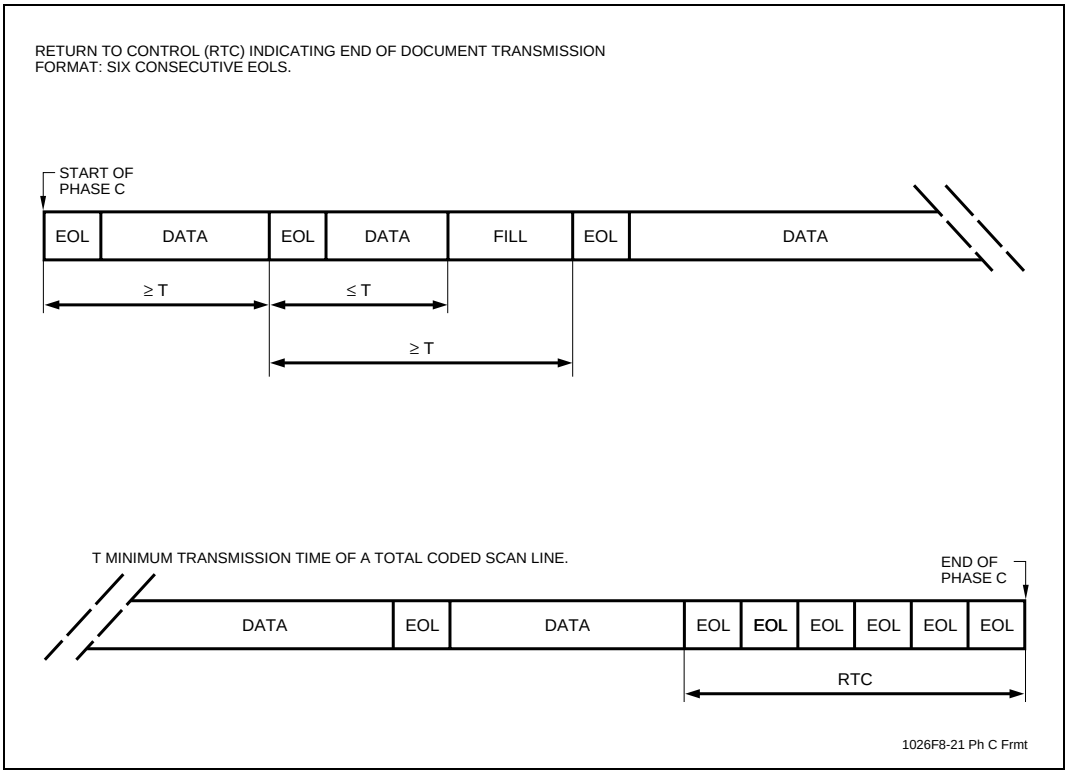


Figure 9-8. Phase C Format

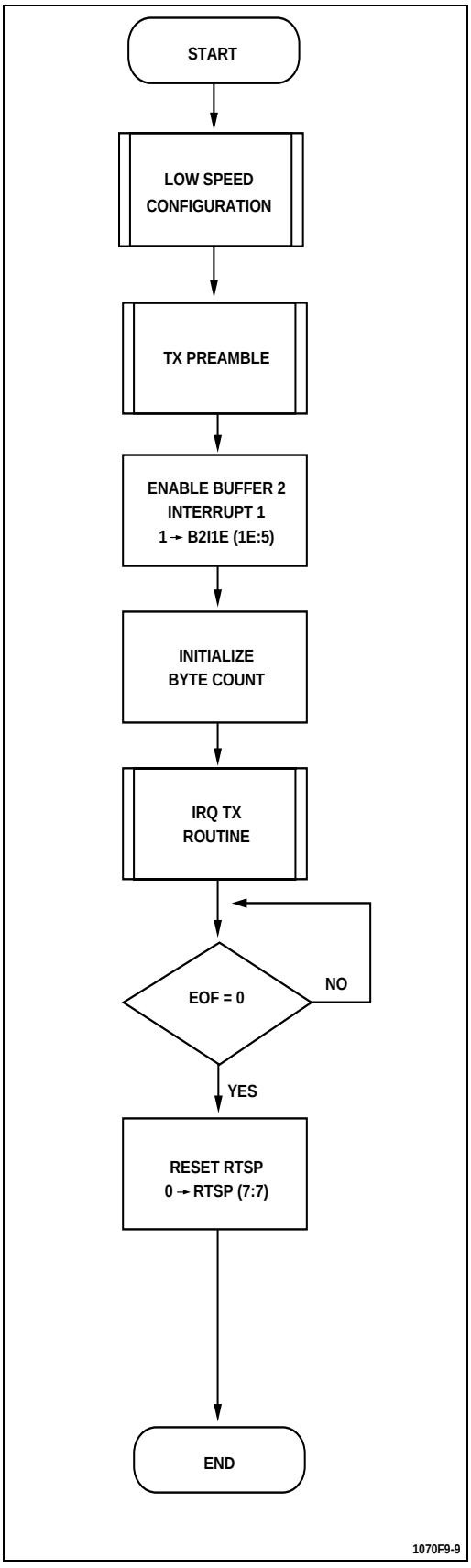


Figure 9-9. Transmit FSK/HDLC Signals

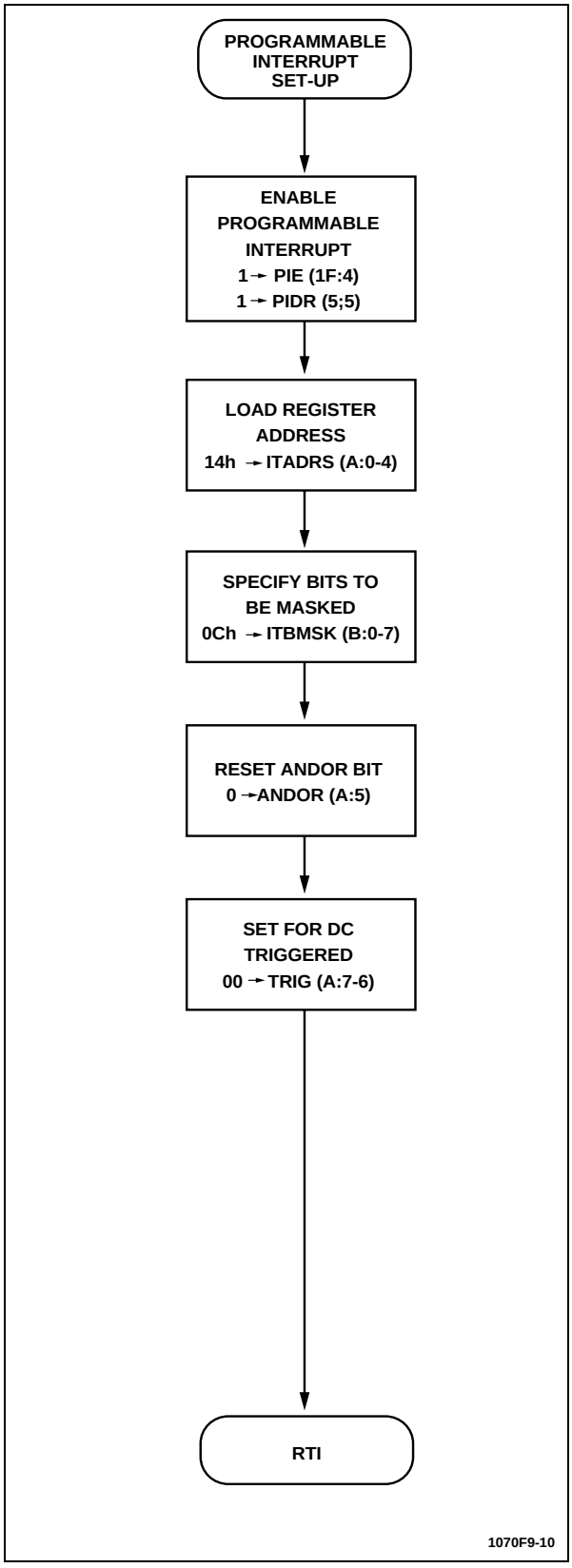


Figure 9-10. Setup for Programmable Interrupt

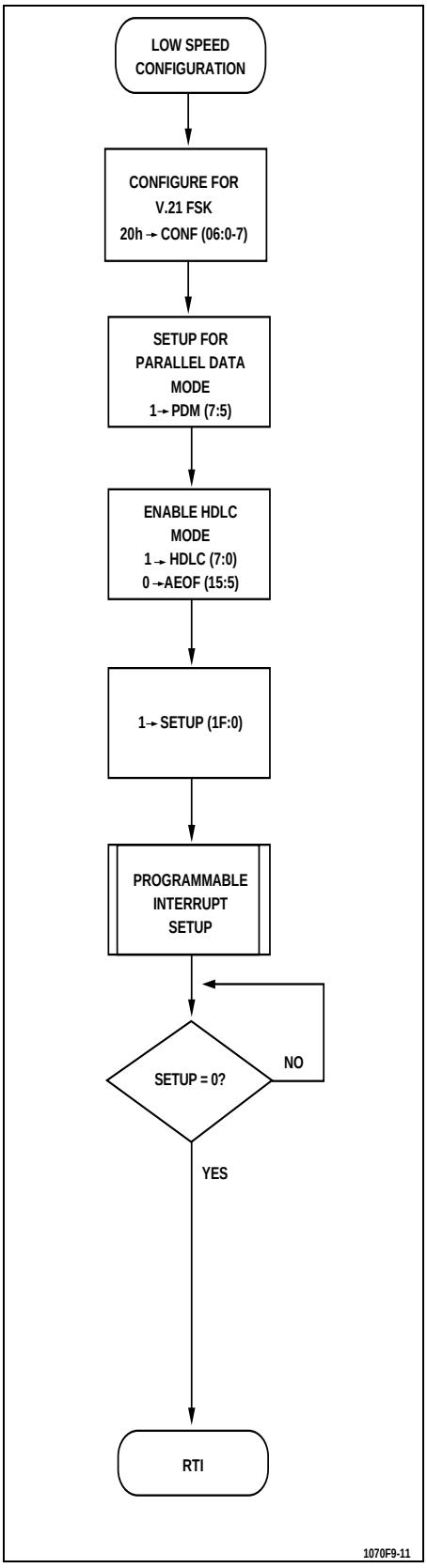


Figure 9-11. Low Speed Configuration Subroutine

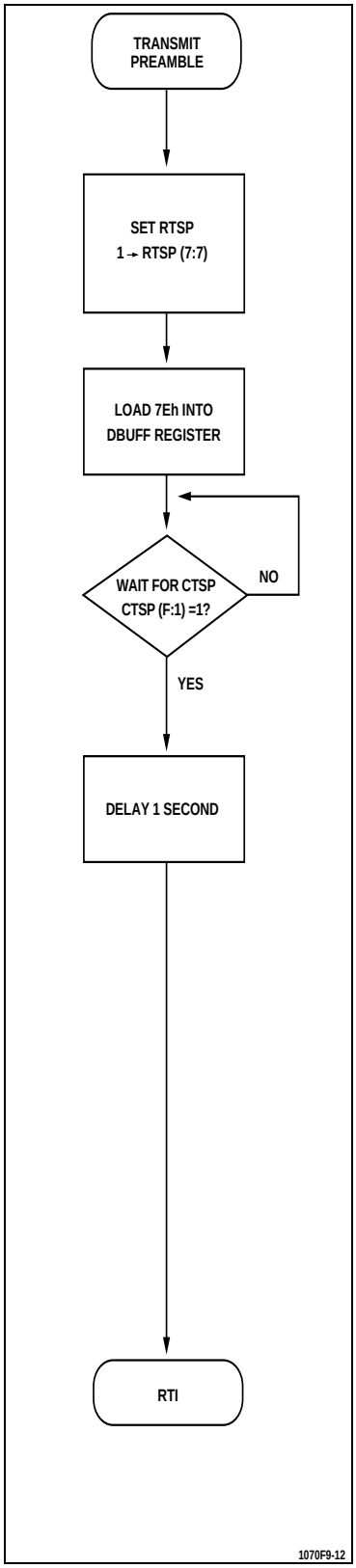


Figure 9-12. Transmit Preamble

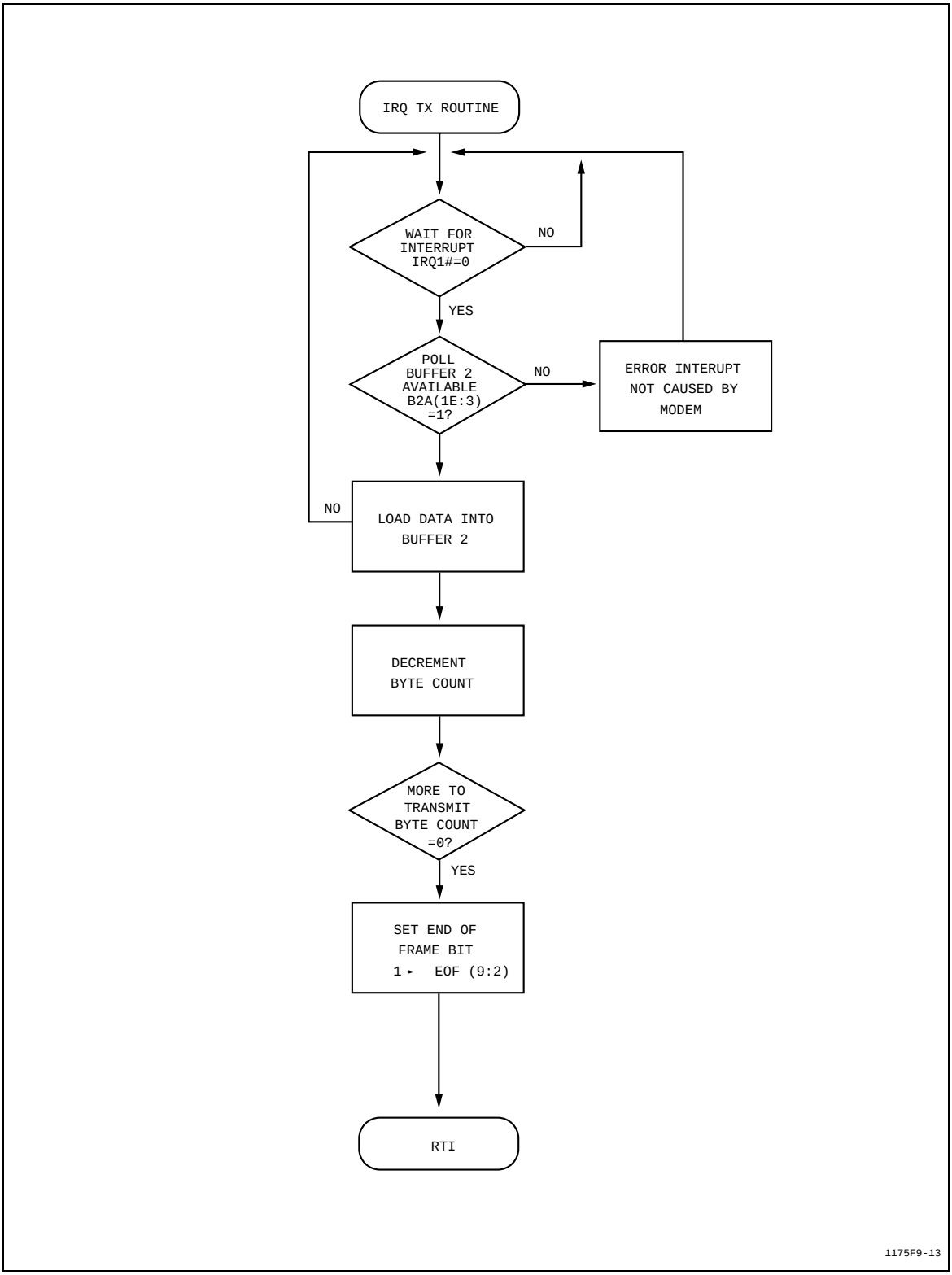


Figure 9-13. Low Speed Interrupt-Driven Transmit

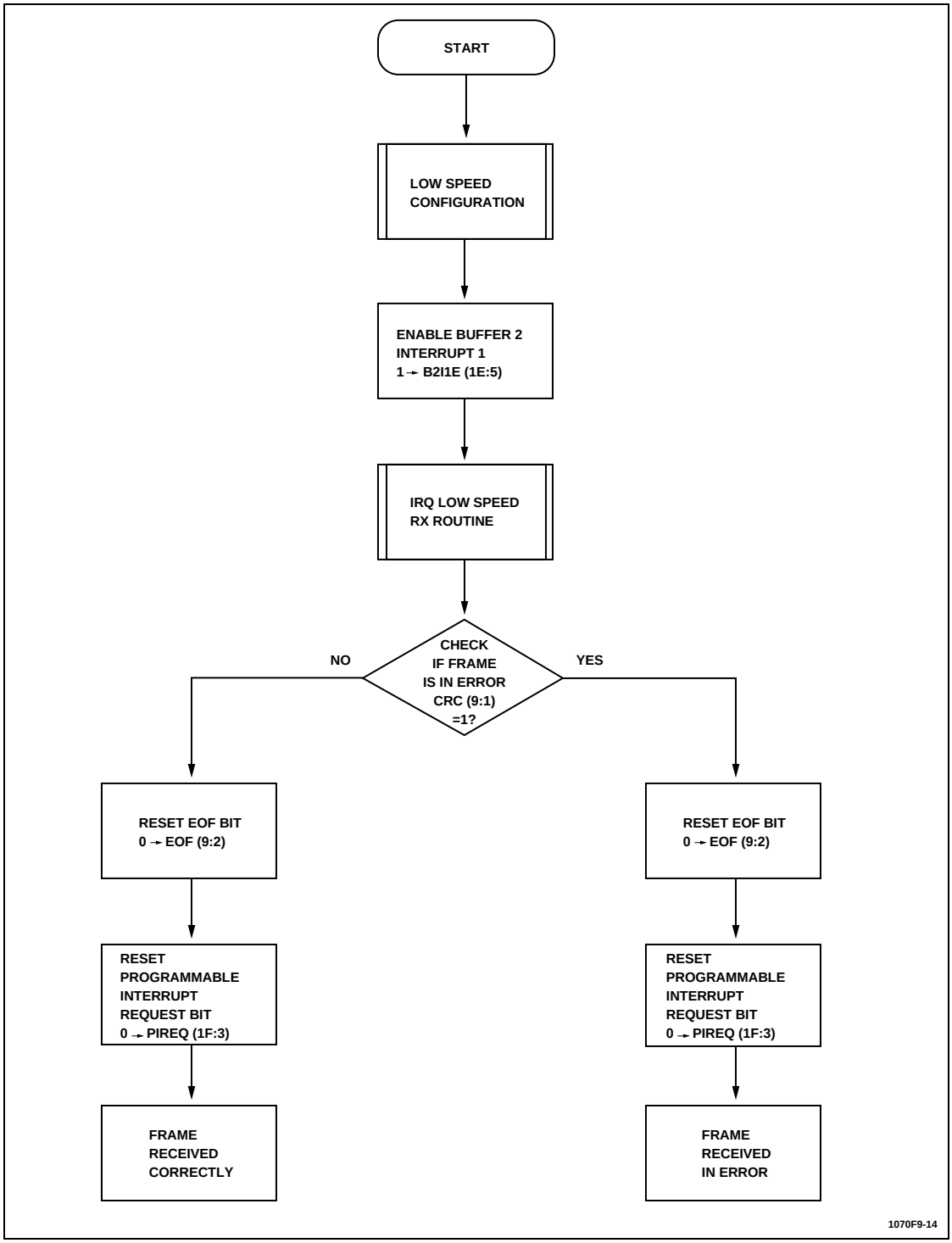


Figure 9-14. Receive FSK/HDLC Signals.

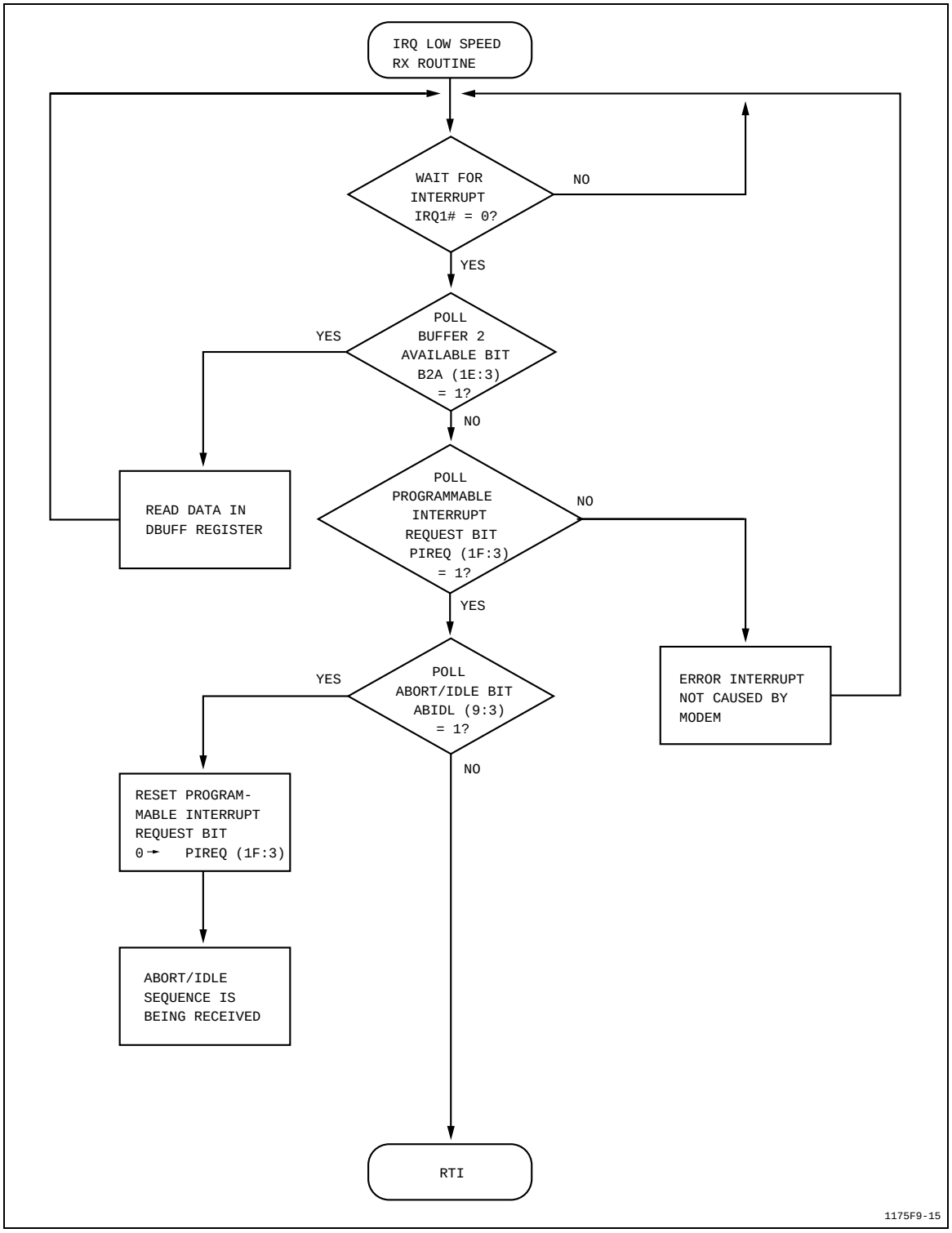


Figure 9-15. Low Speed Interrupt-Driven Receive

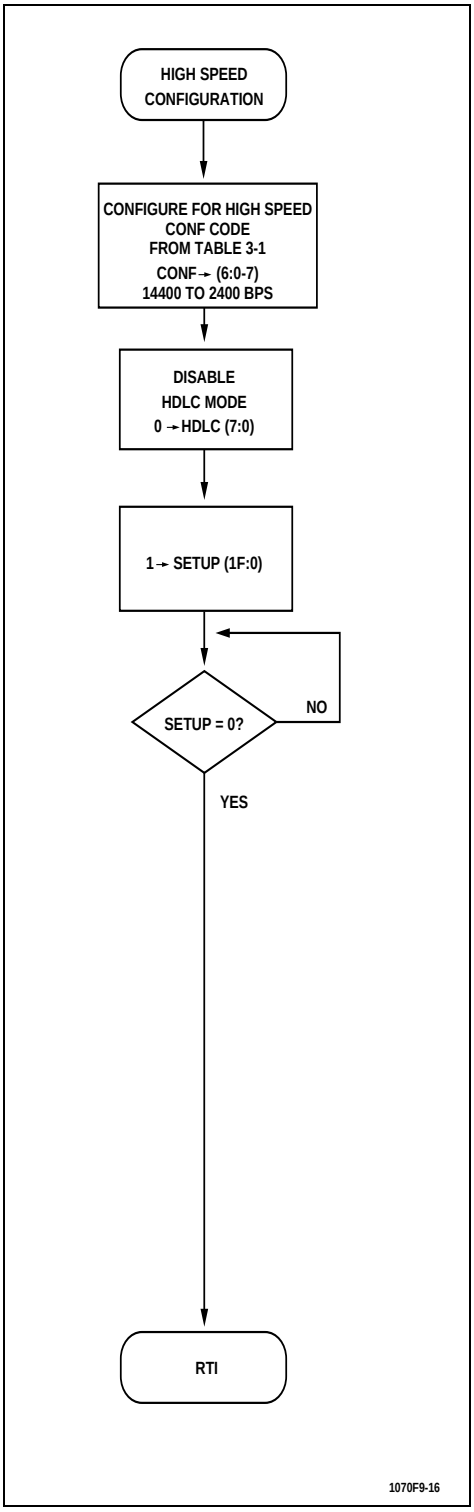


Figure 9-16. High Speed Configuration Setup

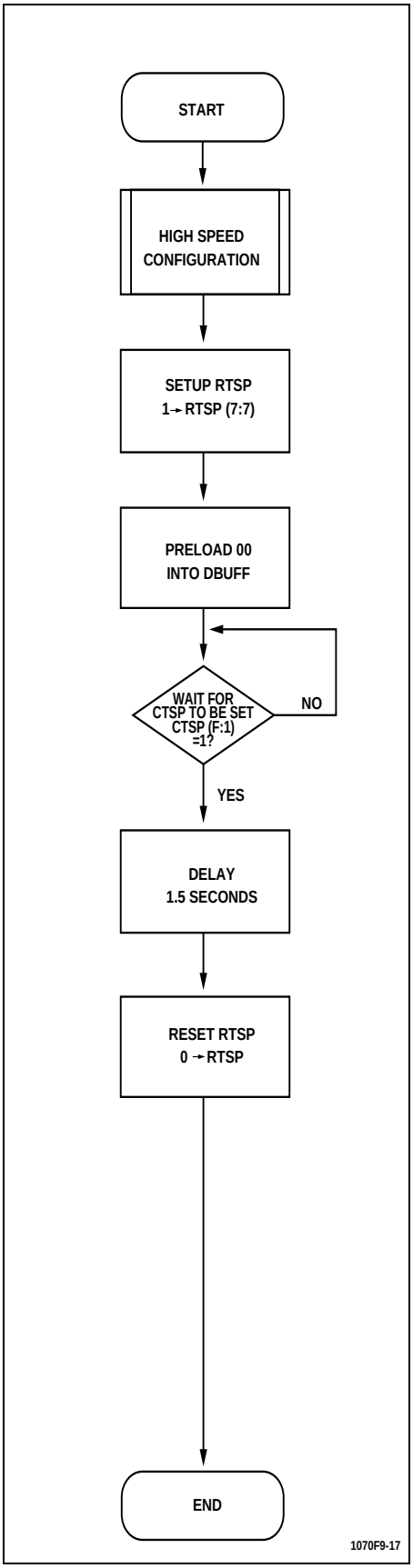


Figure 9-17. Transmitting TCF

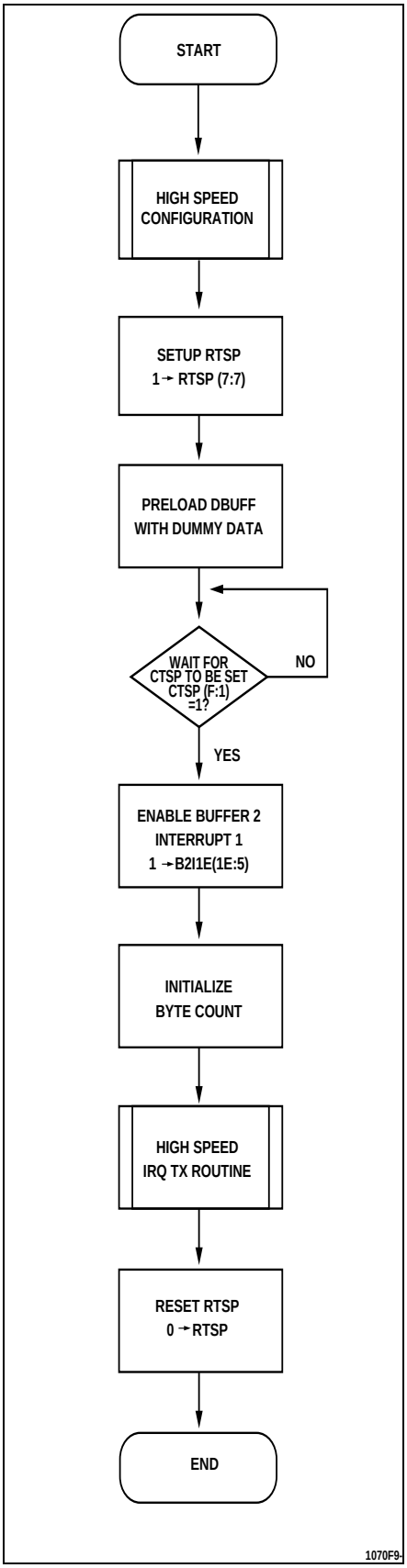


Figure 9-18. High Speed Message Transmission

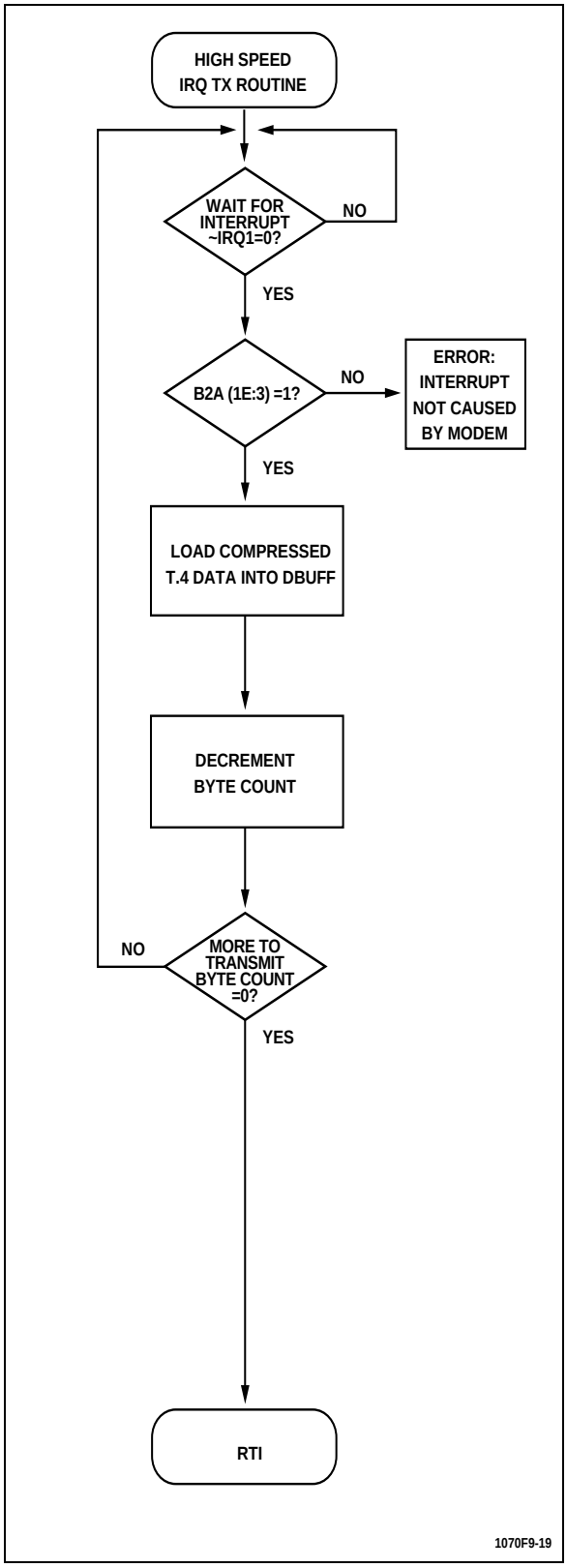


Figure 9-19. High Speed Interrupt-Driven Transmit

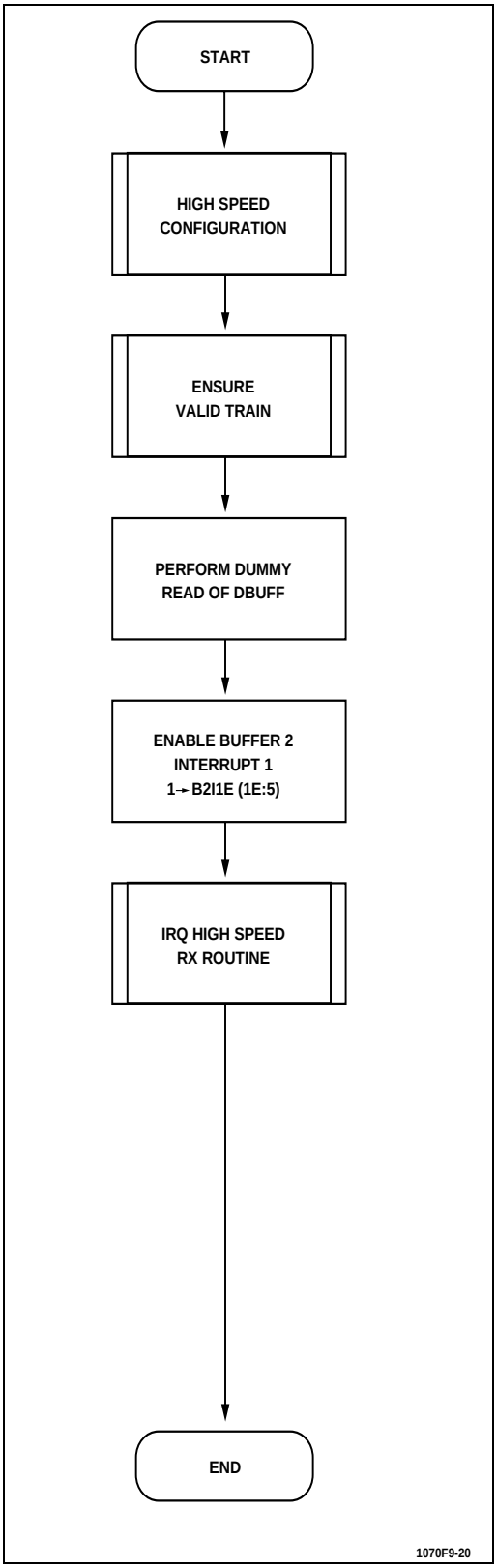


Figure 9-20. High Speed Reception Setup

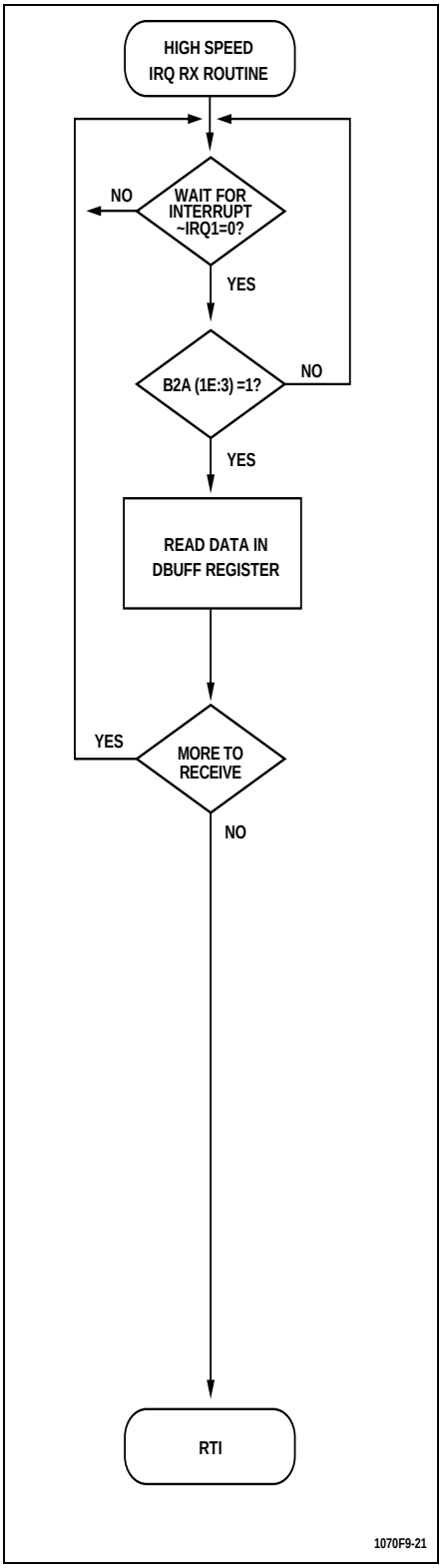


Figure 9-21. High Speed Interrupt Driven Receive

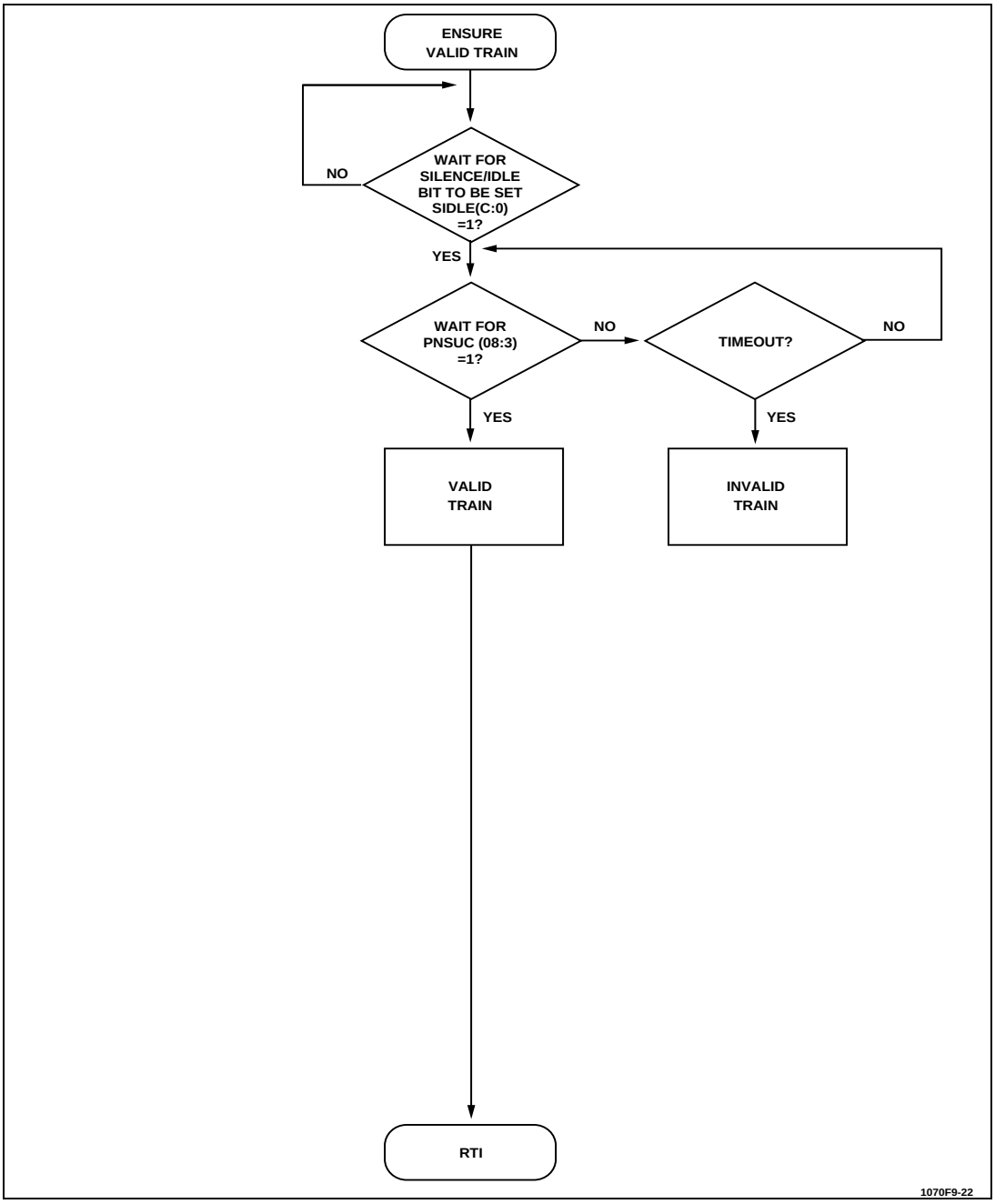


Figure 9-22. Valid Training Sequence Check

9.2 ERROR CORRECTION MODE

9.2.1 General

The revised T.30 contains an Error Correction Mode (ECM) option. The ECM allows the phase C portion of the facsimile transmission to be encoded in a HDLC framing format using a specified number of bits in the information field. The transmitted high speed message is broken up into a number of frames identified by frame numbers. If an error is detected during reception of the message, the called station records the frame number. After all the frames in the message has been received, the called station transmits the frame numbers that were received in error. The calling station then re-transmits only those frames in error. This continues until the entire message is received error free or the calling station decides not to transmit any more frames.

The error detection is performed by comparing the CRC or FCS. Using ECM, the data rate can be as fast as 14,400 bps, therefore, the host microprocessor cannot keep up implementing HDLC without the use of a serial I/O device. The modem provides HDLC features at speeds up to 14,400 bps.

9.2.2 ECM Frame Structure

In Error Correction Mode, one frame of facsimile data consists of 256 or 64 octets of data. Each page may contain 1 to 256 frames. Also, 1 to 256 pages may be transmitted. The ECM frame structure is illustrated in Figure 9-23. Following the high speed training sequence, the flag, address field, and control field is transmitted. In ECM, Flag = 7E, Address = FF, and Control = B0. The Facsimile Control Field for the Facsimile Coded Data block (FCD) is 60. The frame number follows the FCF for FCD, followed by the facsimile data. Pad bits such as EOL, Tag, and Align bits follow the facsimile data. Finally, the FCS check and the ending flag is transmitted.

After 256 frames, a Return Control for Partial page (RCP) block is transmitted three times. The RCP block consists of the same Flag, Address Field, and Control field followed by the FCF for RCP. The FCS immediately follows with the ending flag. After the third RCP, a maximum of 50 ms of flags are transmitted.

An ECM message protocol example is shown in Figure 9-24. The bold arrows are high speed transmissions and the other arrows are FSK transmissions. The example is self-explanatory. If more information is needed, refer to the T.30 ECM specification.

In this paragraph the Q refers to the NULL, EOP, MPS, or EOM Facsimile Control Field commands. The Partial Page Signals (PPS-Q) and Partial Page Request (PPR) frame structures are shown in Figure 9-25. The PPS-Q frame begins with the same Flag, Address field, and Control field. Two FCF commands follow. The first FCF transmitted is to indicate PPS. The second FCF is either NULL, EOP, MPS, or EOM. The page count followed by the block count, followed by the total number of frames in the block are transmitted next. The FCS and ending flag are finally transmitted.

The PPR frame structure also begins with the same Flag, Address, and Control field. The FCF for PPR is the next octet. The FIF consists of 256 or 64 bits depending on how many frames were transmitted. The contents of FIF is either a 0 or a 1. The bit number corresponds to the frame number and a 0 indicates the frames was received correctly and a 1 indicates an incorrect frame was received.

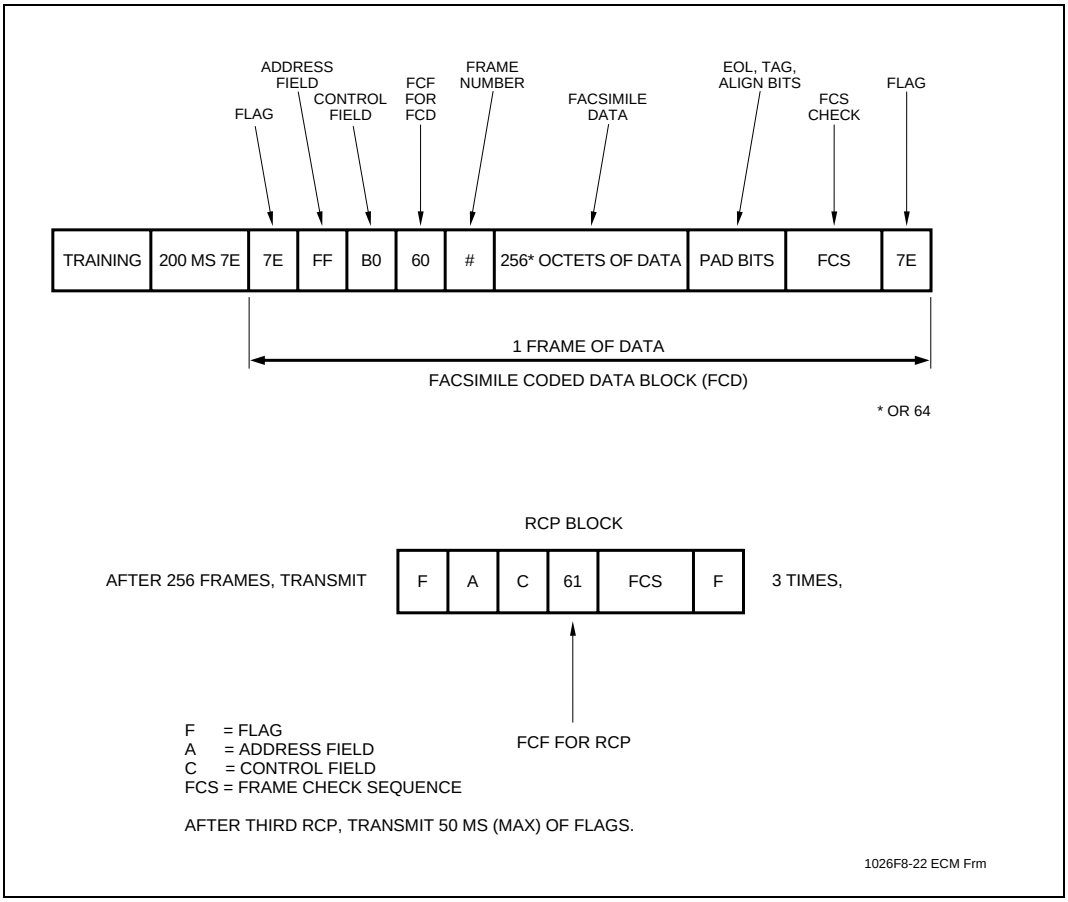


Figure 9-23. ECM Frame Structure

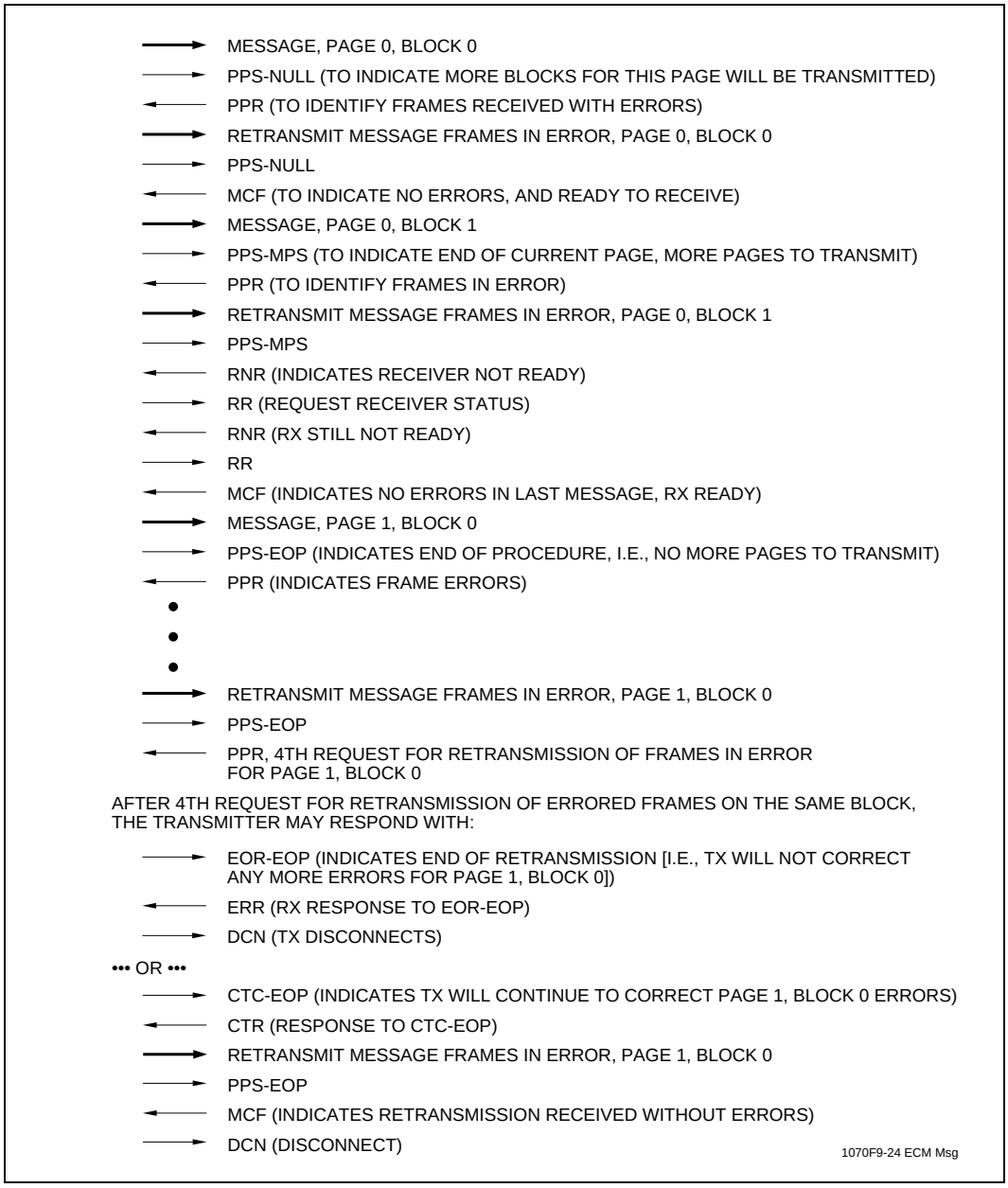


Figure 9-24. ECM Message Protocol Example

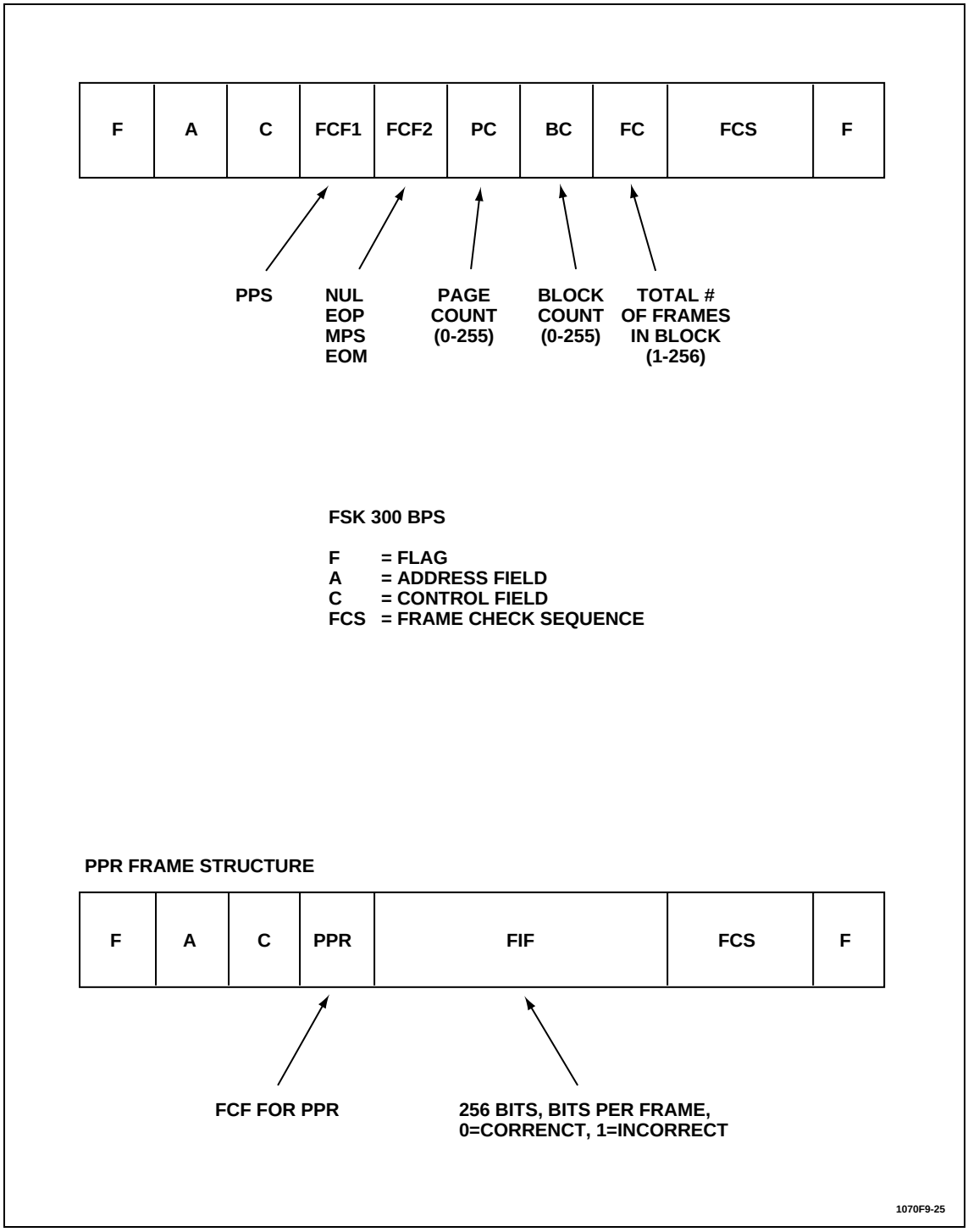


Figure 9-25. PPS and PPR Frame Structure

9.3 SIGNAL RECOGNITION ALGORITHM

9.3.1 FSK vs. High Speed

A method of determining whether a high speed message or V.21 Channel 2 FSK handshaking is being received by the modem is necessary when implementing the T.30 recommendation. When the calling unit transmitter and called unit receiver configure for V.17, V.29, or V.27 ter, sometimes the high speed message may not be received (typically due to a noisy line). In this case, the calling unit transmitter will try to send the message up to three times before re-negotiating in FSK signaling. The called unit receiver must, therefore, be able to distinguish between a high speed message and FSK handshaking. This algorithm is shown in Figure 9-26.

9.3.2 FAX vs. Voice

A method for determining whether a fax or voice message is being received is necessary for combined fax answering machines.

When configured for Voice/Audio Codec mode decoding of an outgoing message, three tone detectors are available. These detectors can be used to detect the fax 1100 Hz calling tone or the 1650 Hz fundamental energy of the FSK flags that begin some T.30 handshakes. The coefficients for FSK detection are shown in Table 9-1. The 1100 Hz calling tone detector coefficients are shown in Table 6-3.The algorithm for FSK detection in Voice Mode is shown in Figure 9-27. The algorithm for CNG detection (1100 Hz) is shown in Figure 9-28.

Table 9-1. FR3 Coefficient for 1650 Hz Detection

	RAM Access Code (Hex)[1]	Coefficient Value(Hex)[2]	Coefficient Value(Hex)[3]
α_0	31	0097	0113
α_1	32	0000	FE7B
α_2	33	FF69	0113
α'_0	34	01D0	0113
α'_1	35	0000	FE7B
α'_2	36	FE30	0113
β_1	B2	97A8	25C4
β_2	B3	C12D	C12D
β'_1	B5	9588	23F8
β'_2	B6	C120	C120
α''	B4	0145	00A3
β''	B1	7EBB	7F5C

1. AREXx = 0, BRx = 0, and CRx = 1.
2. 4000 Hz sample rate.
3. 8000 Hz sample rate.

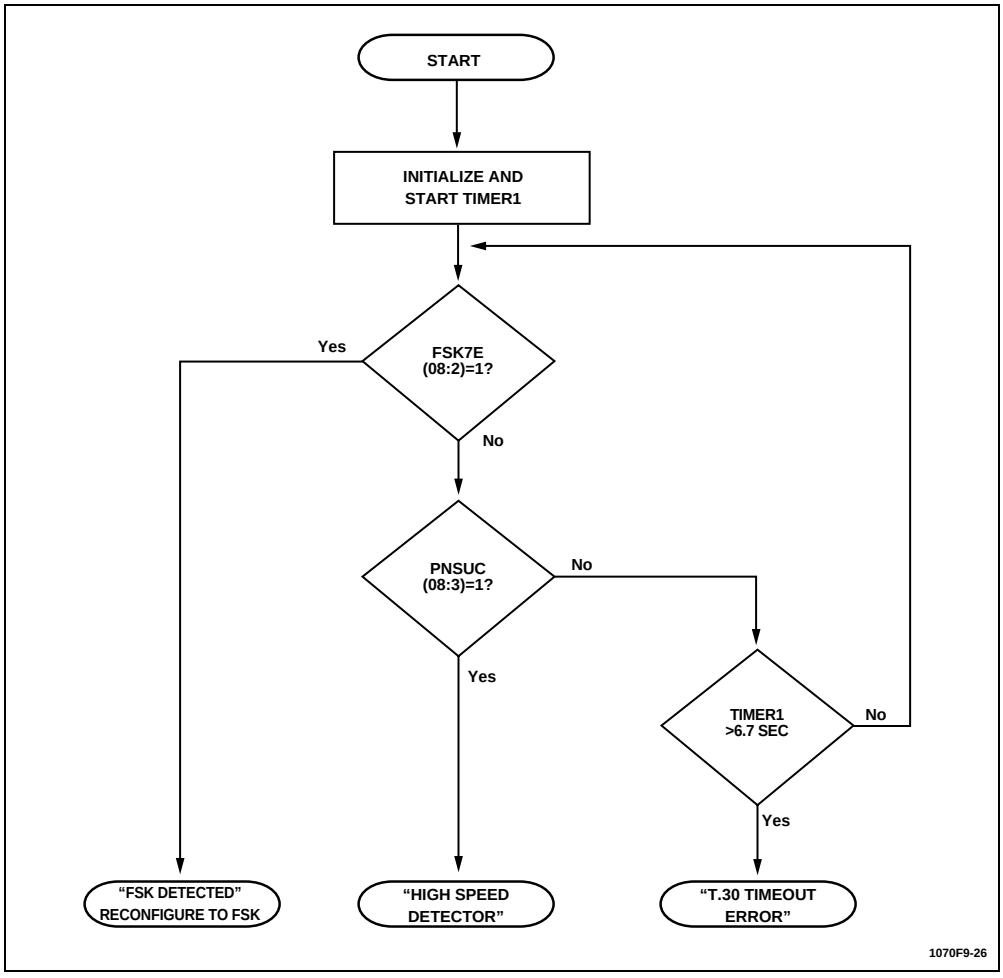


Figure 9-26. Signal Recognition Algorithm in High Speed Mode

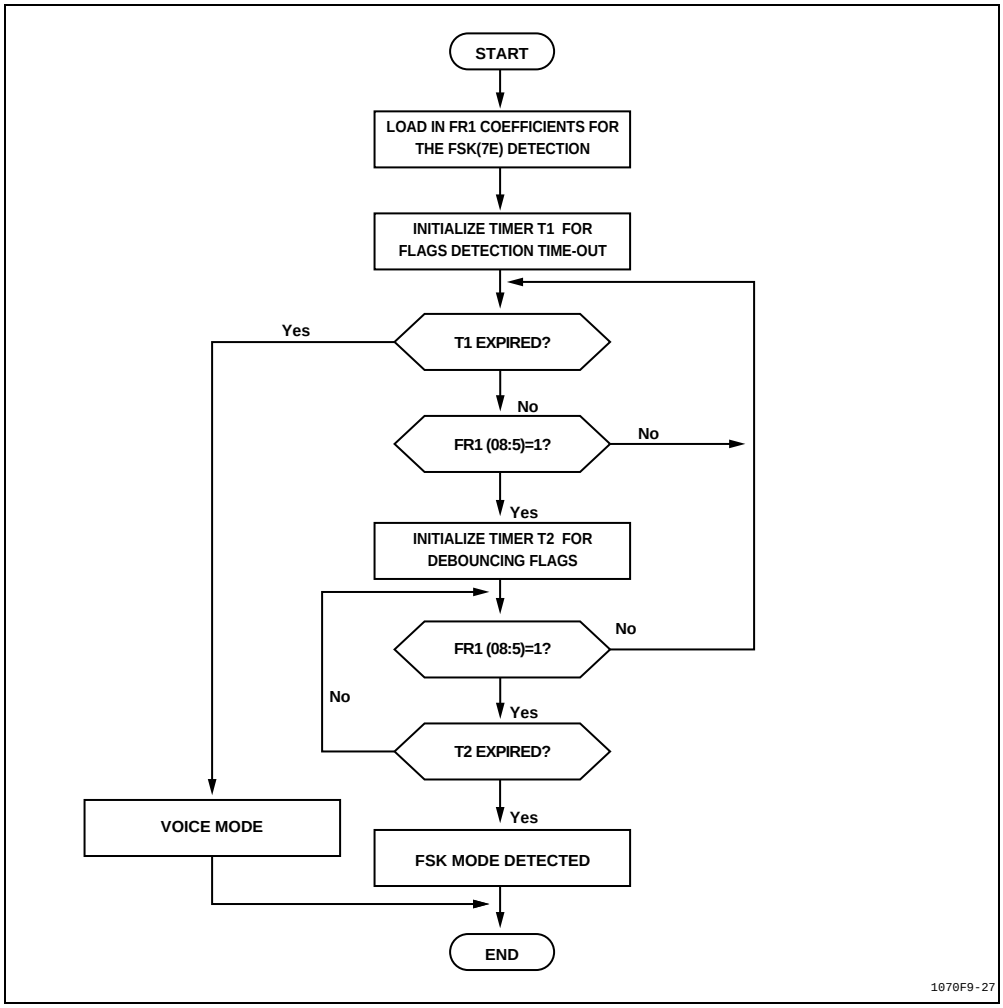


Figure 9-27. FSK Signal Detection Algorithm in Voice Mode

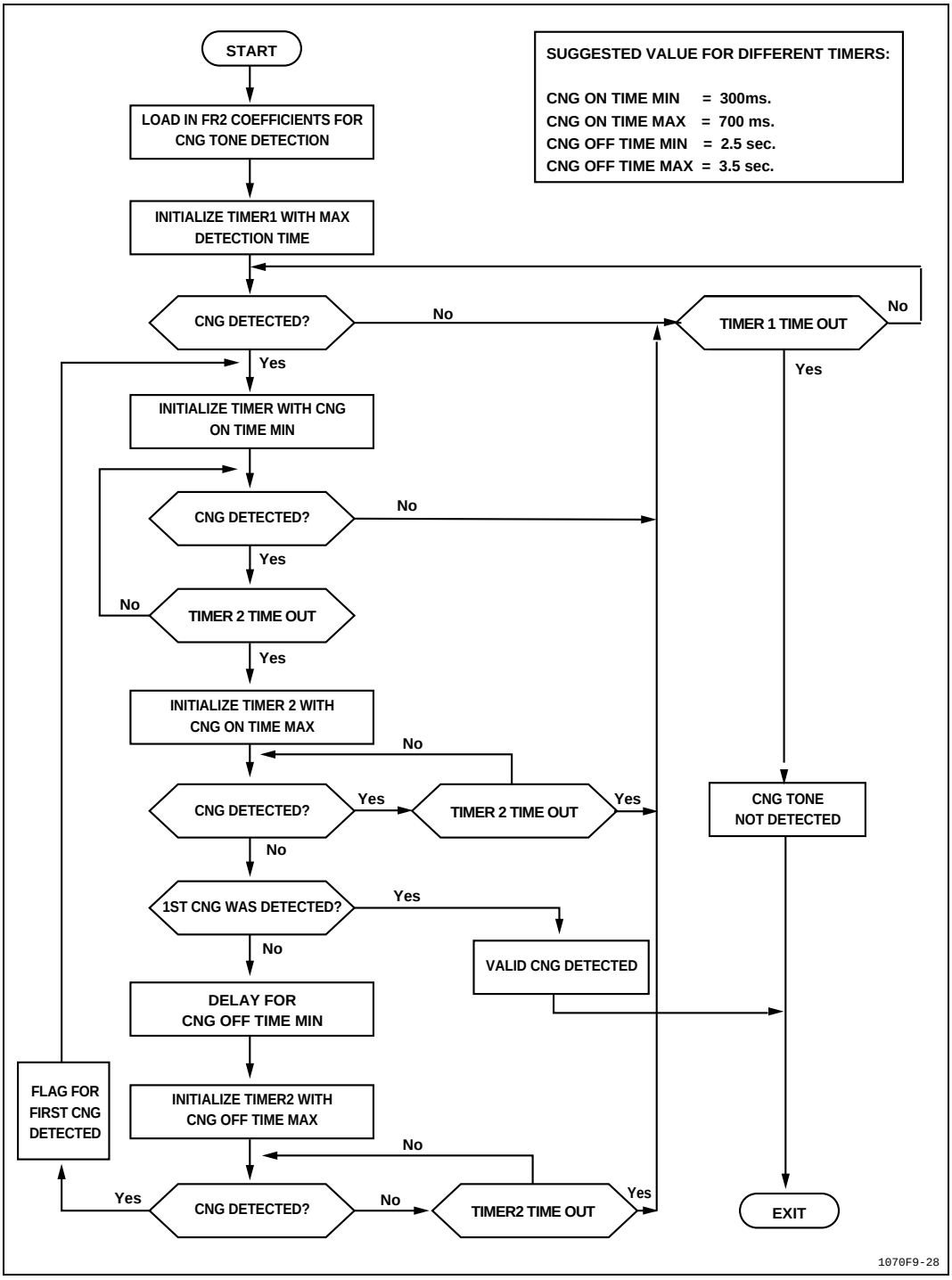


Figure 9-28. CNG Detection (1100 Hz) in Voice Mode

9.4 SHORT TRAIN EXAMPLE

An example of the host implementation of V.17 short train in T.30 is shown in Figure 9-29. The diagram shows the proper setting of control bits EQSV, EQFZ (optional), SHTR, and SETUP. The example starts at the beginning of TCF and the time line proceeds down the page from that point. It is assumed that the first TCF is successful and EQSV and EQFZ are properly reset to 0 prior to the long train V.17 reception.

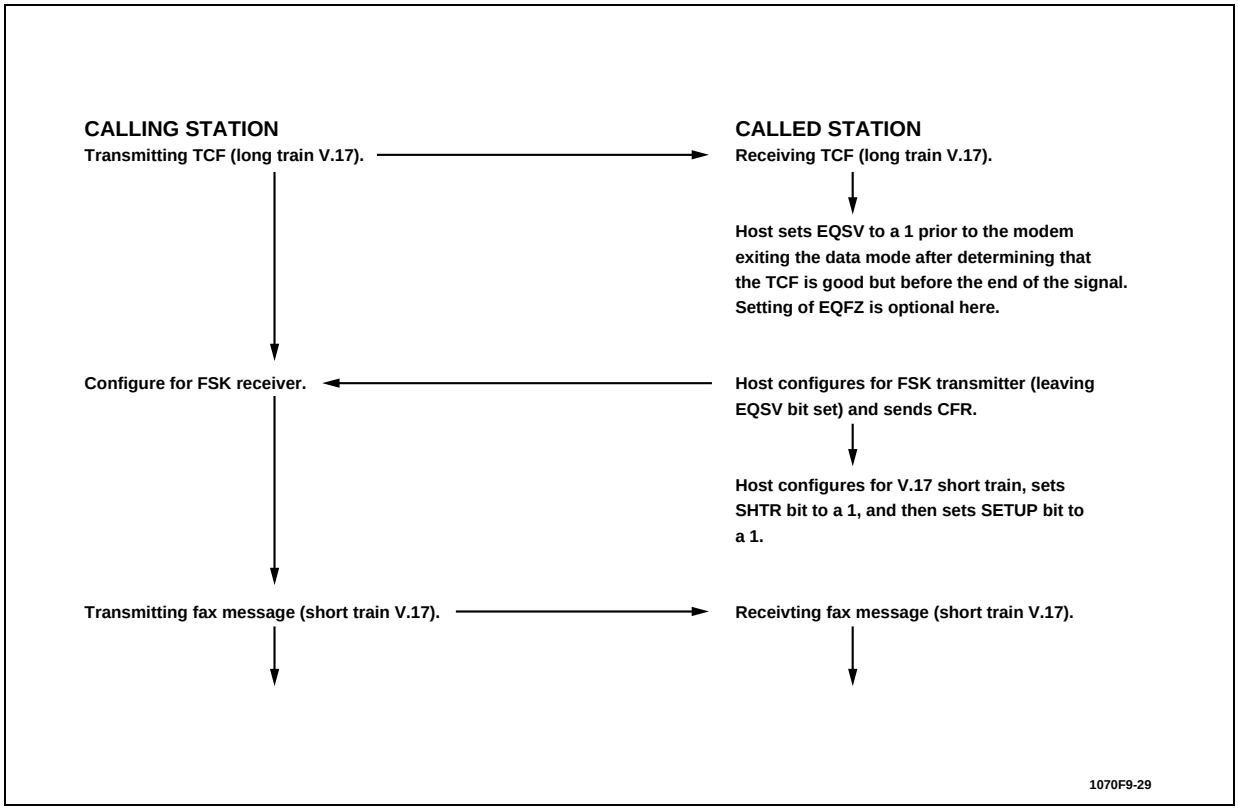


Figure 9-29. Example V.17 Short Train Time Line

10. CALLER ID

10.1 INTRODUCTION

Calling Number Delivery (CND), known as Caller ID, is a telephone service intended for residential and small business customers. It allows the called Customer Premises Equipment (CPE) to receive a calling party's directory number and the date and time of the call during the first silent interval in the ringing cycle. The customer must contact a Bellcore Client Company to initiate CND service.

10.2 CALLING NUMBER DELIVERY SPECIFICATION

All of this CND information, according to Bellcore, is sent between the first and the second ring and starts as early as 300 ms after the first ring burst and ends at least 475 ms before the second ring burst.

The following information summarizes the CND information provided by Bellcore.

10.3 PARAMETERS

The data signaling interface has the following characteristics:

Link Type:..... 2-wire, simplex

Transmission Scheme:.. Analog, phase-coherent FSK

Logical 1 (mark):..... 1200±12 Hz

Logical 0 (space):..... 2200±22 Hz

Transmission Rate: ..... 1200 bps

Transmission Level: ..... -13.5±1 dBm into 900 Ω load

10.4 PROTOCOL

The protocol uses 8-bit data words (bytes), each bounded by a start bit and a stop bit. The CND message uses the Single Data Message format shown below.

Channel Seizure Signal	Carrier Signal	Message Type Word	Message Length Word	Data Word(s)	Checksum Word

10.4.1 Channel Seizure Signal

The channel seizure signal is 30 continuous bytes of 55h (01010101). This provides a detectable alternating function to the modem.

10.4.2 Carrier Signal

The carrier signal consists of 130±25 ms of mark (1200 Hz) to condition the receiver for data.

10.4.3 Message Type Word

The message type word indicates the service and capability associated with the data message. The message type word for CND service is 04h (00000100).

10.4.4 Message Length Word

The message length word specifies the total number of data words to follow.

10.4.5 Data Words

The data words are encoded in ASCII and represent the following information:

- The first two words represent the month.
- The next two words represent the day of the month.
- The next two words represent the hour in local military time.
- The next two words represent the minute after the hour.

The calling party's directory number is represented by the remaining words in the data word field. If the calling party's directory number is not available to the terminating central office, the data word field contains an ASCII "O". If the calling party invokes the privacy capability, the data word field contains an ASCII "P".

10.4.6 Checksum Word

The Checksum word contains the twos complement of the modulo 256 sum of the other words in the data message (message type, message length, and data words). The receiving equipment may calculate the modulo 256 sum of the received words and add this sum to the received checksum word. A result of zero generally indicates that the message was correctly received. Message retransmission is not supported.

10.4.7 Example CND Single Data Message

An example of a received CND message, beginning with the message type word, follows:

04 12 30 39 33 30 31 32 32 34 36 30 39 35 35 35 31 32 31 32 51

04h = Calling number delivery information code (message type word).

12h = 18 decimal; Number of data words (date, time, and directory number words).

ASCII 30, 39 =09; September

ASCII 33, 30 = 30; 30th day

ASCII 31, 32 = 12; 12:00 PM

ASCII 32, 34 = 24; 24 minutes (12:24 PM)

ASCII 36 30 39 35 35 35 31 32 31 32 = 609-555-1212; calling party's directory number.

51h = Checksum Word.

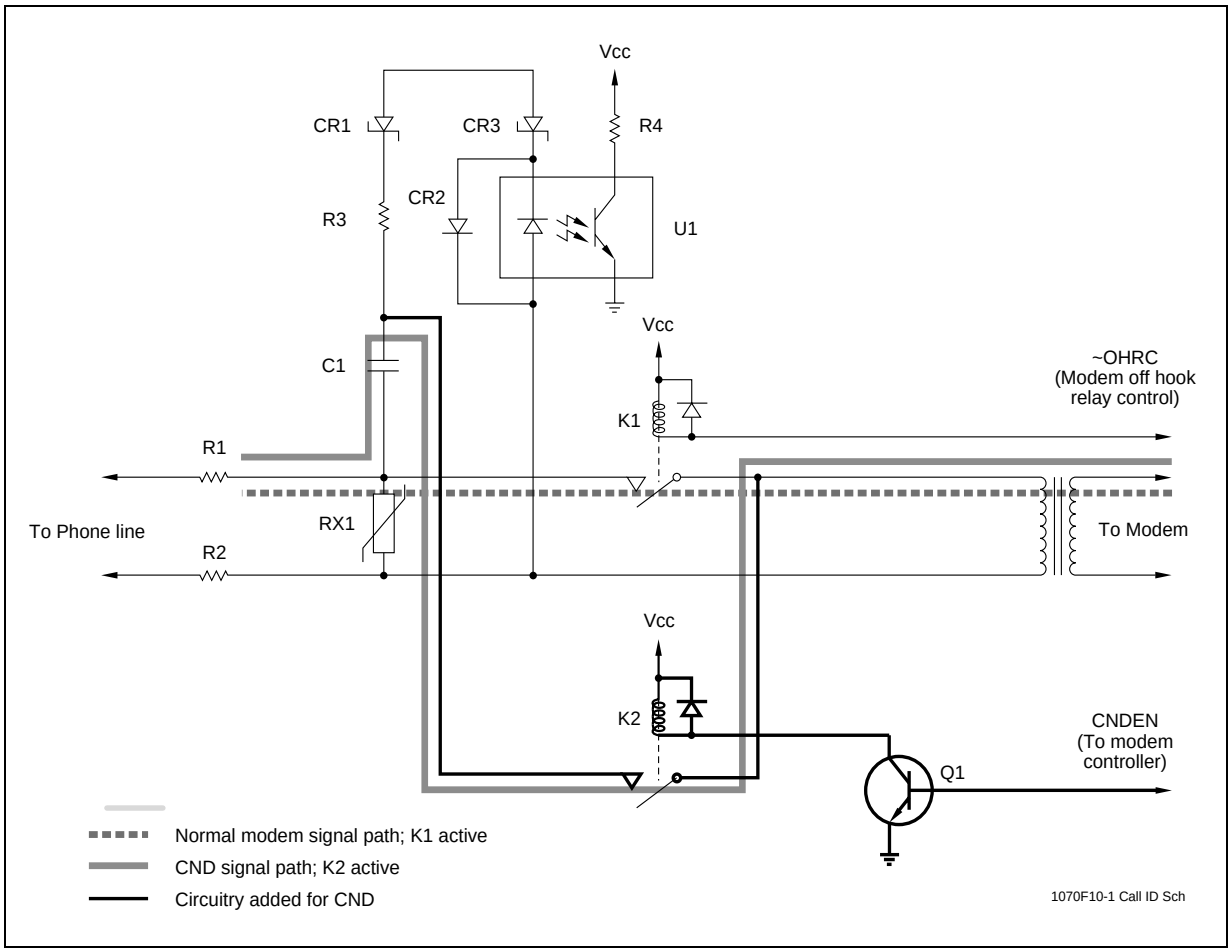


Figure 10-1. DAA Circuit Supporting CND

10.5 DAA REQUIREMENTS

To receive CND information, the modem monitors the phone line between the first and second ring bursts without causing the DAA to go off hook in the conventional sense, which would inhibit the transmission of CND information by the local central office. A simple modification to an existing DAA circuit (Figure 10-1) easily accomplishes the task.

With the addition of Q1 and K2, the DAA is AC-coupled to the phone line through the ring detect capacitor, C1, allowing the CND signal to pass to the modem while blocking DC loop current that would place the line off hook.

10.6 MODEM REQUIREMENTS

Although the data signaling interface parameters match those of a Bell 202 modem, the receiving CPE need not be a Bell 202 modem. A V.23 1200 bps modem receiver may be used to demodulate the Bell 202 signal.

The ring detection circuit, combined with a "Ring Detection" firmware routine done by the host, allows the host to activate and deactivate the CNDEN relay to monitor the telephone line for receiving the CND information.

After a valid ring is detected, the RI bit is set to indicate occurrence of the first ring burst to the host. The host waits for 250 ms of silence then activates the CNDEN line (see Figure 10-1) and configures the modem for CND reception as follows:

CONF = 22h

PDM = 1

SETUP = 1 and wait until SETUP = 0

Wait until CDET = 1

The received data is now available via DBUFF (10:0-7).

CNDEN must be deactivated by the host prior to the reception of the second ring burst.

10.7 APPLICATIONS

Flowcharts corresponding to the above process are shown in Figure 10-2.

Once CND information is received, the user may process the information in a number of ways.

1. The date, time, and calling party's directory number can be displayed.
2. Using a look-up table, the calling party's directory number can be correlated with his or her name and the name displayed.
3. CND information can also be used in additional ways such as for:
   a) Bulletin board applications,
   b) Black-listing applications,
   c) Keeping logs of system user calls, or
   d) Implementing a telemarketing data base.

10.8 REFERENCES

For more information on Calling Number Delivery (CND), refer to Bellcore publications TR-TSY-000030 and TR-TSY-000031.

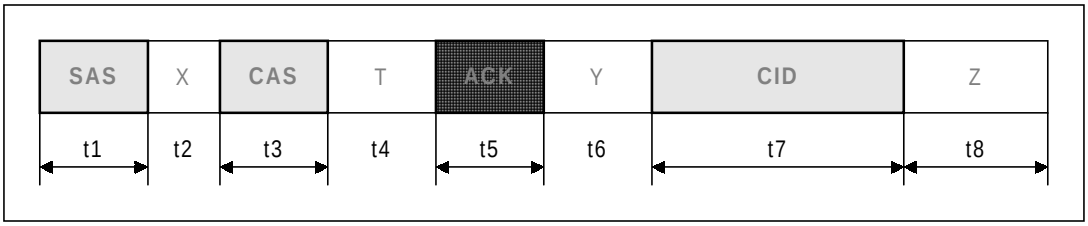
To obtain Bellcore documents, contact:

Bellcore Customer Service
60 New England Avenue, Room 1B252
Piscataway, NJ 08834-4196
(201) 699-5800

10.9 TYPE II CALLER ID

Type II Caller ID CAS detection is operational in Speakerphone, Voice Codec, and ADPCM Audio codec modes. It operates concurrently with the DTMF receiver, three tone detectors, and tone transmit. Status bit CASD (08:3) is set by the modem when the CAS dual-tone Type II Caller ID signal is detected, provided control bit CASDIS (1A:1) has not been set by the host to disable detection. After CASD is set and CAS signal detected, the host must reset status bit CASD to allow subsequent Type II Caller ID CAS signals to be detected.

Type II Caller ID provides the calling party's identity delivery when a call is waiting. This service is combined with the Call Waiting service. The following shows a typical example of Type II Caller ID signal.



SAS : Subscriber Alerting Signal

t1: 440Hz 300 ms typical (250 – 1000 ms)

CAS: CPE Alerting Signal 2130Hz/2750Hz Dual tone at -15 dBm

t3: 80-85 ms Rx is expected at -32 to -14dBm with 75 to 80 ms duration up to 6 dB twist

ACK: DTMF D (or DTMF A)

t4+t5: 155- 165 ms

t4: t4 should be less than 100ms

t5: 55 - 65 ms

t6: 0- 500ms, should be shorter than 500ms

CID: Caller ID Signal

t7: varies depend on service type.

t8: 0-50ms

The Host is responsible for sending the acknowledge signal for the CAS tone back to the phone company for Type II Caller ID reception.

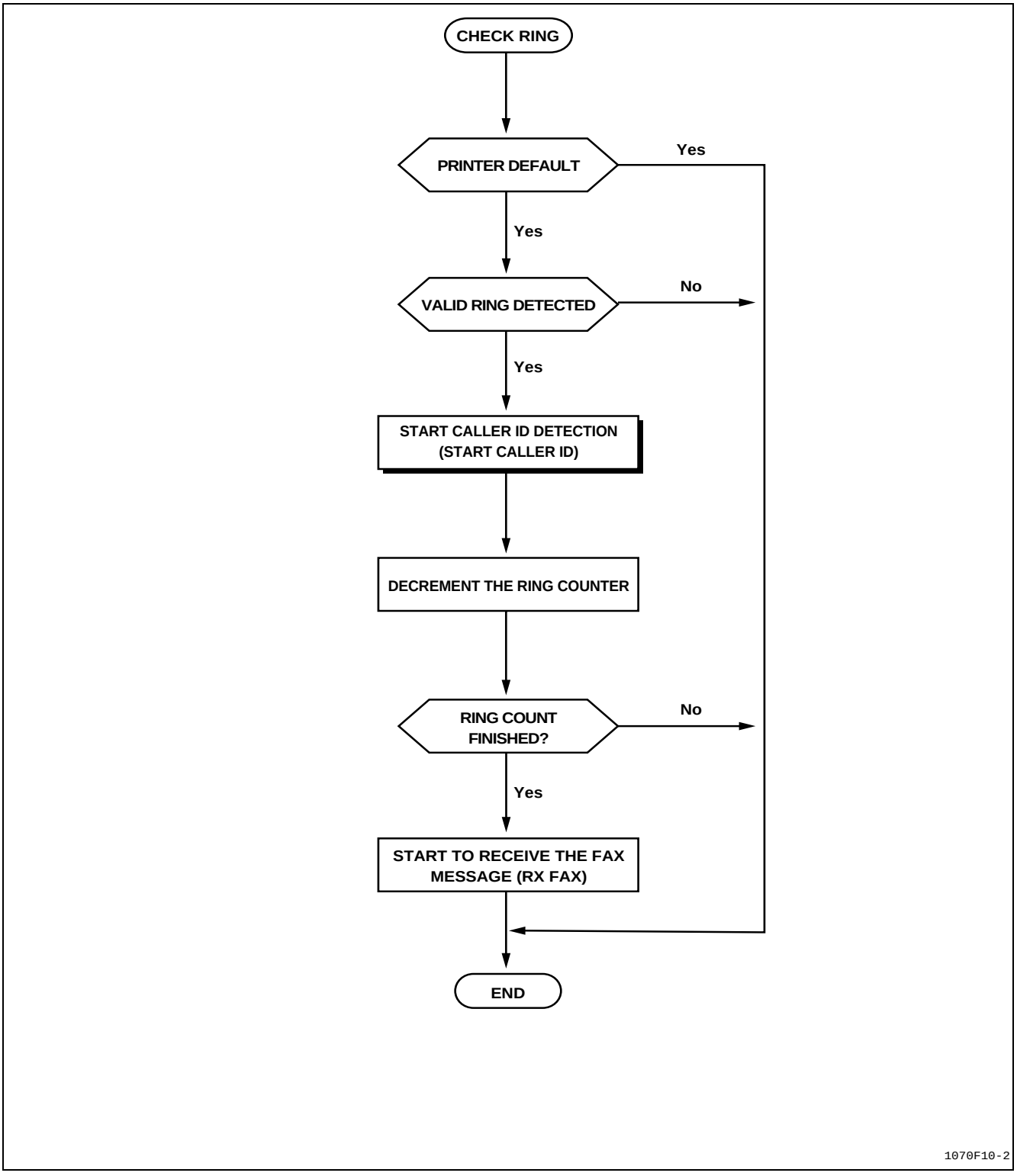


Figure 10-2. Caller ID Example Flowchart

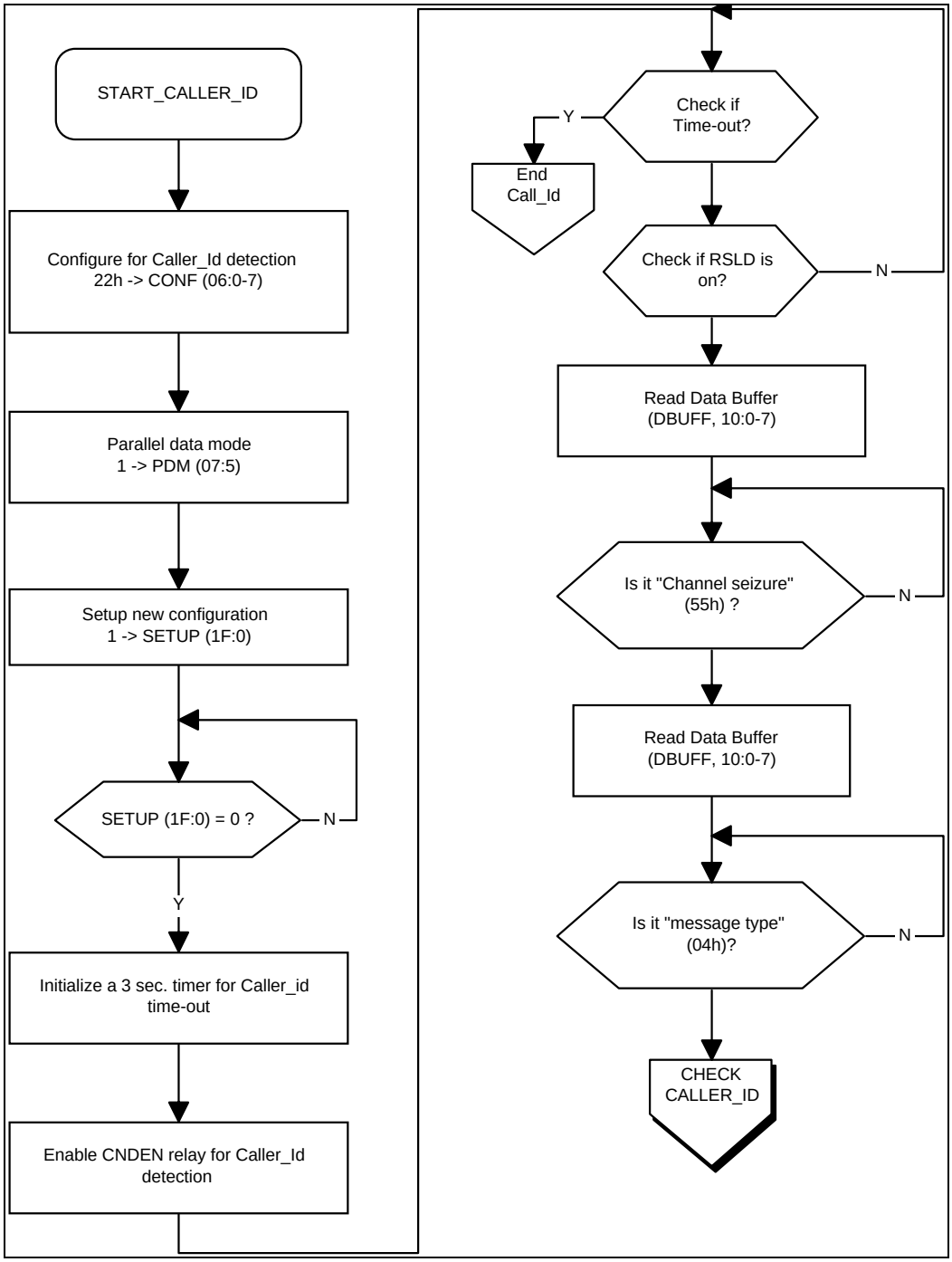


Figure 10-2. Caller ID Example Flowchart (Cont'd)

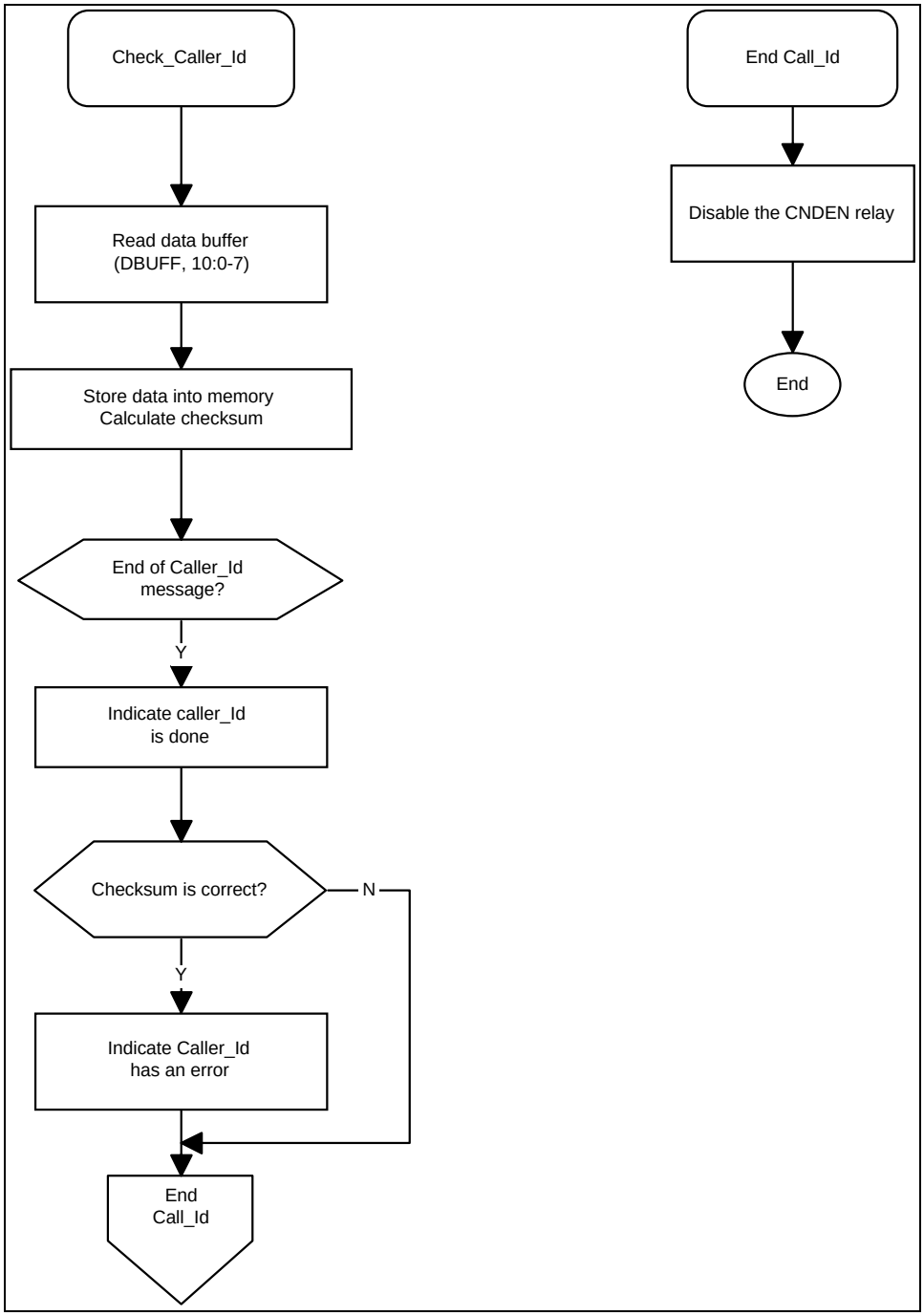


Figure 10-2. Caller ID Example Flowchart (Cont'd)

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11. DIGITAL EQUALIZATION/HIGH PASS FILTER

11.1 PROGRAMMABLE DIGITAL EQUALIZER (PDE)

A programmable digital equalizer is provided in the receiver and transmitter. The programmable digital equalizer consists of four cascaded biquads. This is similar to the tone detectors when cascaded by enabling bit 12^{TH}. The programmable digital equalizer is enabled by setting bit PDEQZ. The block diagram is shown in Figure -11-1.

11.1.1 PDE Frequency Response

The programmable digital equalizer defaults to a Japanese two link delay equalizer, with 1.1 dB gain at 2700 Hz. The frequency response curves are shown in Figure 11-2.

11.1.2 PDE Coefficients

The equation to calculate the hex coefficients is:

$$Coefficient_{16} = Coefficient * 32768$$

The format is 16 bits, signed, twos complement. The coefficient range is from -1 (8000h) to +1 minus 1 least significant bit (7FFFh).

The poles and zeros are shown in Table 11-1.

The programmable digital equalizer RAM access codes are shown in Table 11-2.

Note: The default filter coefficients are written by the modem at power-on and when the modem changes configurations from a configuration having a 8000 Hz sample rate to having a 9600 Hz sample rate.

11.2 FIXED DIGITAL CABLE COMPROMISE EQUALIZER

An optional fixed cable compromise equalizer (in the receiver/transmitter) is enabled by setting bit DCABLE. The digital cable equalizer frequency response is shown in Figure 11-3.

11.3 HIGH PASS FILTER

An optional receiver digital high pass filter (HPF) is enabled by setting bit HPFEN. Figure 11-4 and Figure 11-5 show the modem response with and without the high pass filter enabled, respectively.

Note: This filter response is only valid in the 8000 Hz sample rate modes. For the 9600 Hz sample rate modes, the response is shifted such that the notch is at 72 Hz.

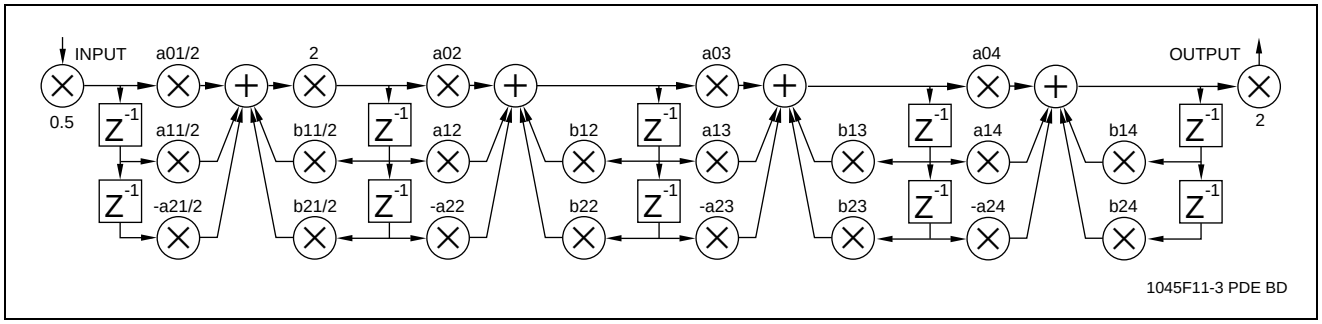

Figure -11-1. PDE Block Diagram

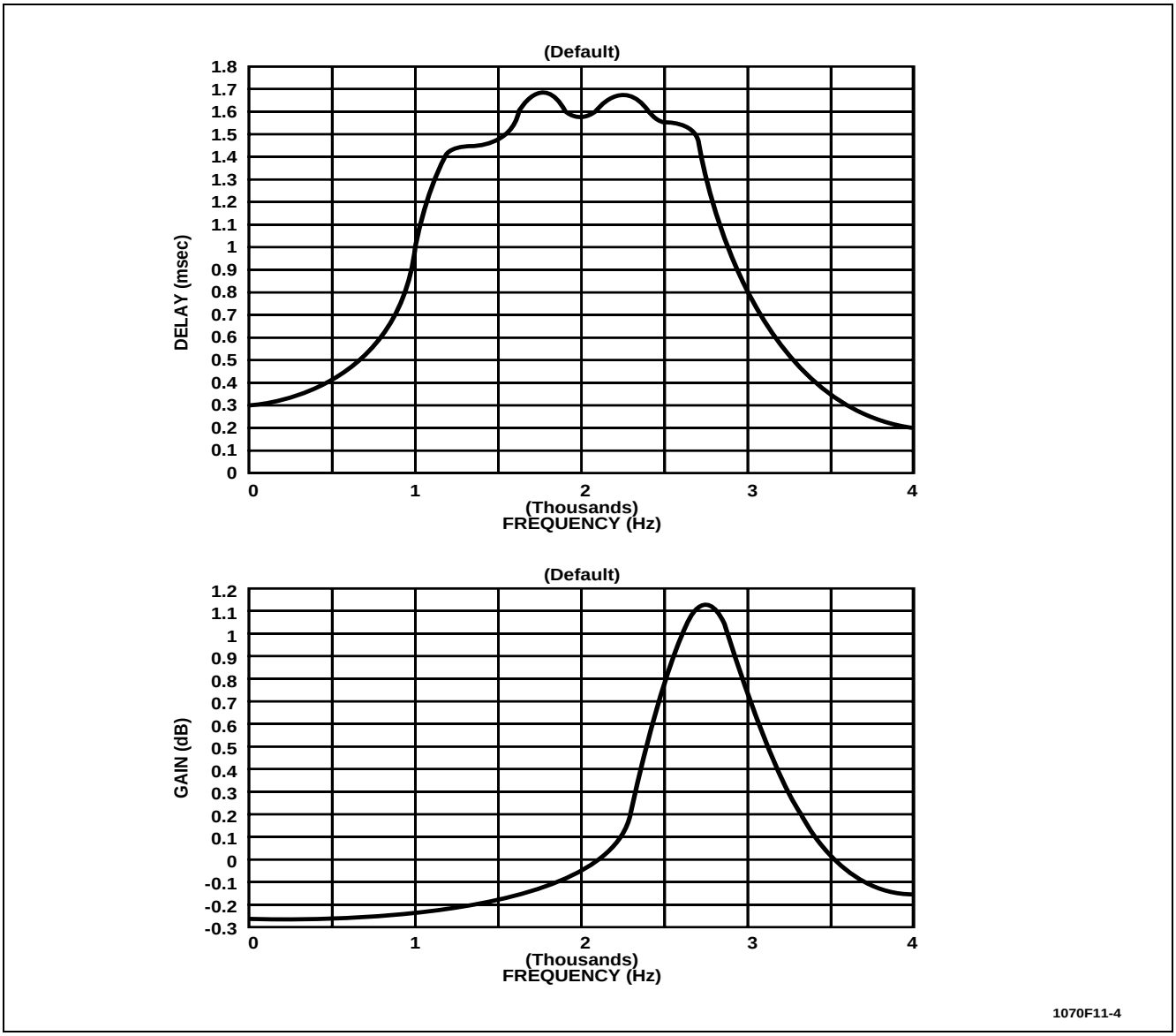

Figure 11-2. PDE Response

Table 11-1. PDE Poles and Zeros

Section Number	Poles	Zeros
1	0.794 @ 1215 Hz	1.26 @ 1215 Hz
2	0.798 @ 1728 Hz	1.25 @ 1728 Hz
3	0.793 @ 2241 Hz	1.26 @ 2241 Hz
4	0.830 @ 2713 Hz	1.27 @ 2713 Hz

Table 11-2. PDE PRAM Access Codes

Parameter	AREXx	BRx	CRx	IOx	ADDx	Read Reg. No.	Default Value (Hex)	Default Value (Dec)
a01/2	0	0	0	0	C6	0, 1	285C	0.31531771
a02	0	0	0	0	C8	0, 1	516C	0.63611724
a03	0	0	0	0	CA	0, 1	50A5	0.63002045
a04	0	0	0	0	CC	0, 1	4FB4	0.62269083
a11/2	0	0	1	0	46	2, 3	B8D1	-0.55611875
a21/2	0	0	1	0	47	2, 3	C000	-0.50000000
a12	0	0	1	0	48	2, 3	A8FF	-0.67972752
a22	0	0	1	0	49	2, 3	8000	-1.00000000
a13	0	0	1	0	4A	2, 3	EAD7	-0.16531356
a23	0	0	1	0	4B	2, 3	8000	-1.00000000
a14	0	0	1	0	4C	2, 3	291D	0.32118352
a24	0	0	1	0	4D	2, 3	8000	-1.00000000
b11/2	0	0	1	0	C8	0, 1	472F	0.55611875
b21/2	0	0	1	0	C9	0, 1	D7A4	-0.31531771
b12	0	0	1	0	CA	0, 1	5701	0.67972752
b22	0	0	1	0	CB	0, 1	AE94	-0.63611724
b13	0	0	1	0	CC	0, 1	1529	0.16531356
b23	0	0	1	0	CD	0, 1	AF5B	-0.63002045
b14	0	0	1	0	CE	0, 1	D4EA	-0.33660000
b24	0	0	1	0	CF	0, 1	AA61	-0.66890000

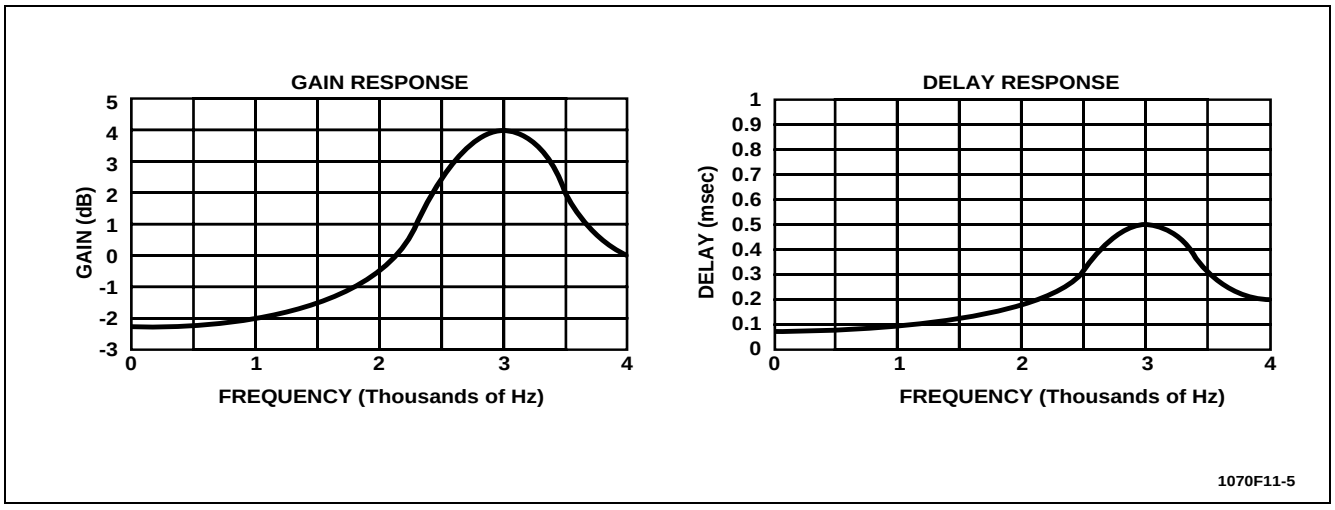

Figure 11-3. Digital Cable Equalizer Frequency Response

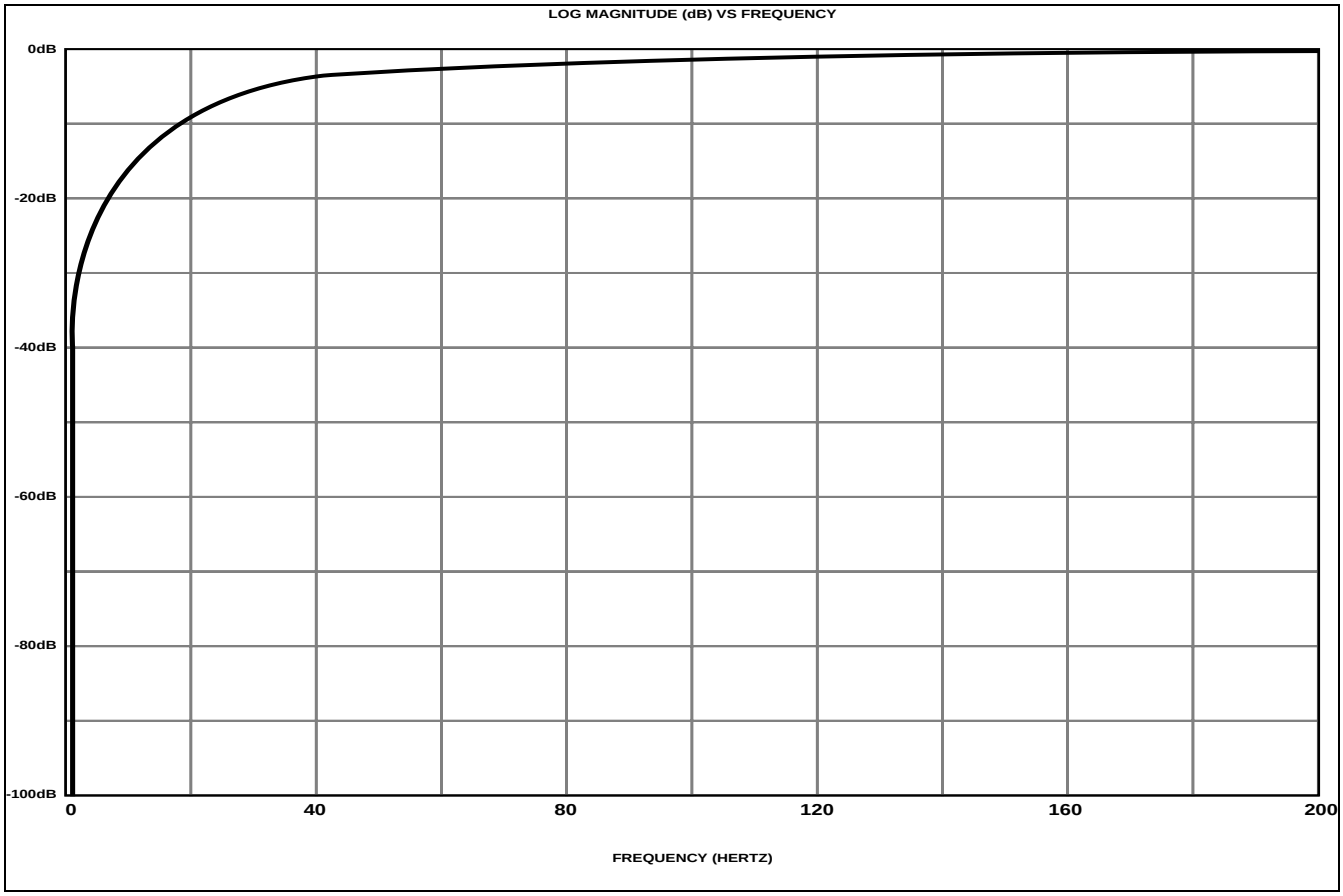

Figure 11-4. Receive Path Frequency Response without HPF

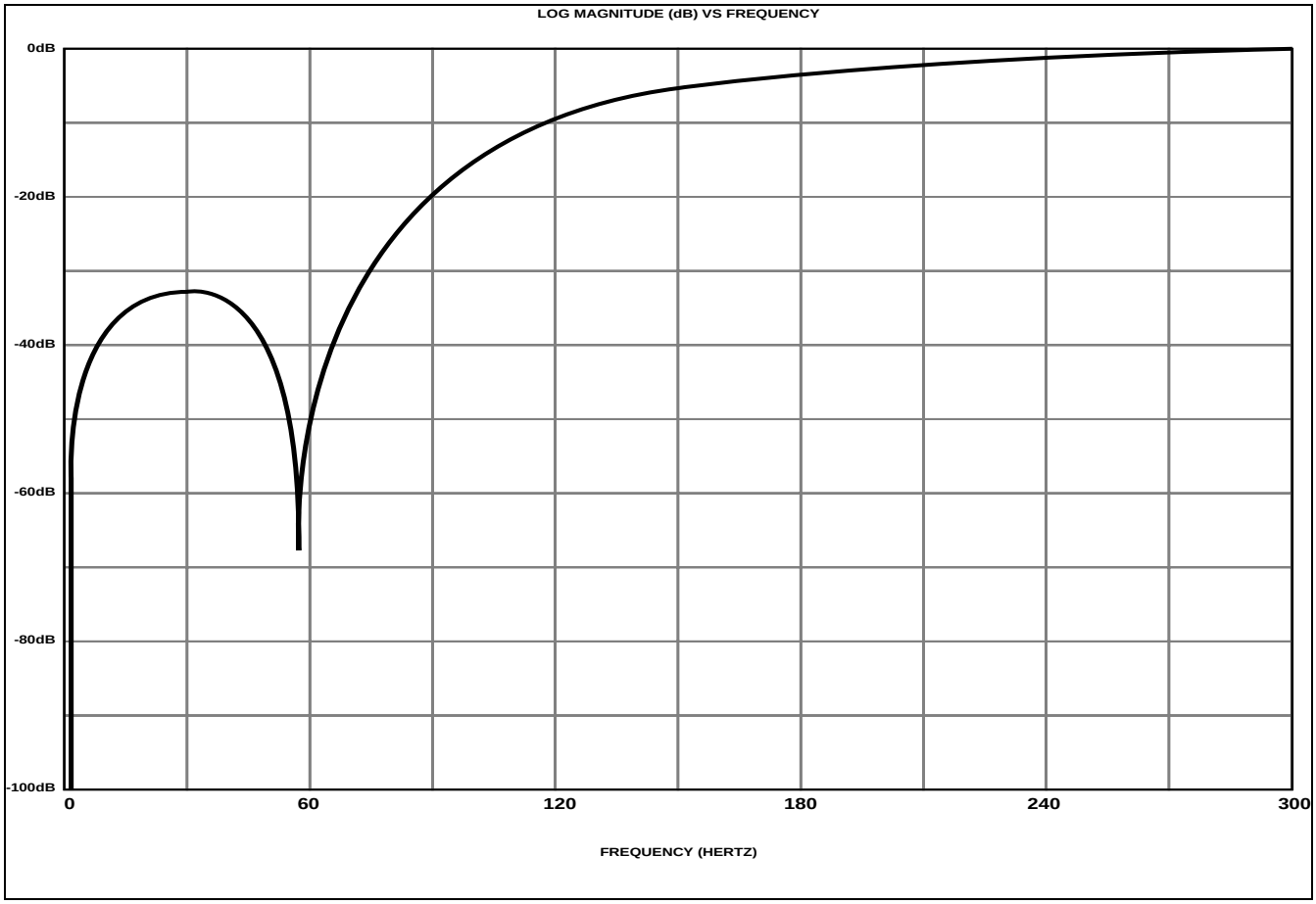

Figure 11-5. Receive Path Frequency Response with HPF

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12. SPEAKERPHONE

12.1 INTRODUCTION

A full-duplex (FDX) speakerphone is a hands-free telephone which allows incoming and outgoing voice to flow simultaneously without clipping and other distortion. A half-duplex(HDX) speakerphone allows voice transmission in one direction at a time.

A separate microphone and separate loudspeaker are used instead of a handset. Since the microphone and speaker are located away from the user's head, a loss in voice pick-up is introduced. Microphone gain must be added in order to transmit the outgoing voice at a desirable level and a speaker gain must be added for listening to the incoming voice comfortably. The FDX Speakerphone maintains "balanced" gain settings between the microphone and speaker channels to keep both channels open. The total amount of gain must be limited to prevent feedback instability (ringing). This limitation makes a FDX speakerphone design impossible without the application of echo cancellation technology. In HDX speakerphone mode, gain balancing is not a concern since voice transmission is allowed in one direction at a time preventing feedback instability. Consequently, the total amount of gain may be significantly greater.

A FDX speakerphone must deal with two echo paths, one caused by the impedance mismatch in the electronic hybrid (line echo), and one caused by the acoustic coupling from the loudspeaker to the microphone (room echo). Echo in the system can distort the voice signal as well as make the system unstable. Both an acoustic echo canceller (AEC) and a line echo canceller (LEC) are included to minimize the echo levels so voice data is clean and system gain is optimized. In FDX Intercom support mode, LEC tap length can be programmed to max of 508 taps to perform as a second AEC. In HDX Intercom support mode, AEC and LEC are bypassed.

Automatic Gain Control (AGC) for both the microphone and the loudspeaker circuits are important speakerphone design elements. Microphone TX AGC helps keep the transmit output at a desired level when the talker moves around the room. The Speaker RX AGC copes with variations in attenuation characteristics in the telephone system to minimize the user's need to adjust the speaker volume. Other host programmable fixed transmit and receive path scalars are provided.

Programmable biquad filters are available for the microphone and speaker circuits.

Conversation recording is supported by ADPCM Audio and Voice codecs. This allows the user to have a record of the voice conversation. Message playback during conversation is also supported without interruption to conversation.

In addition to the voice functions, a speakerphone has to be able to dial DTMF digits, generate variety of ring-tones, and detect some call-progress signaling tones such as dial tone, DTMF detection, and Type II Caller ID CAS detection. Two programmable dual-tone transmitters, three tone detectors, a DTMF receiver, and a Type II Caller ID CAS detector are supplied for this purpose. Table 12-1 lists the corresponding RAM Access Codes.

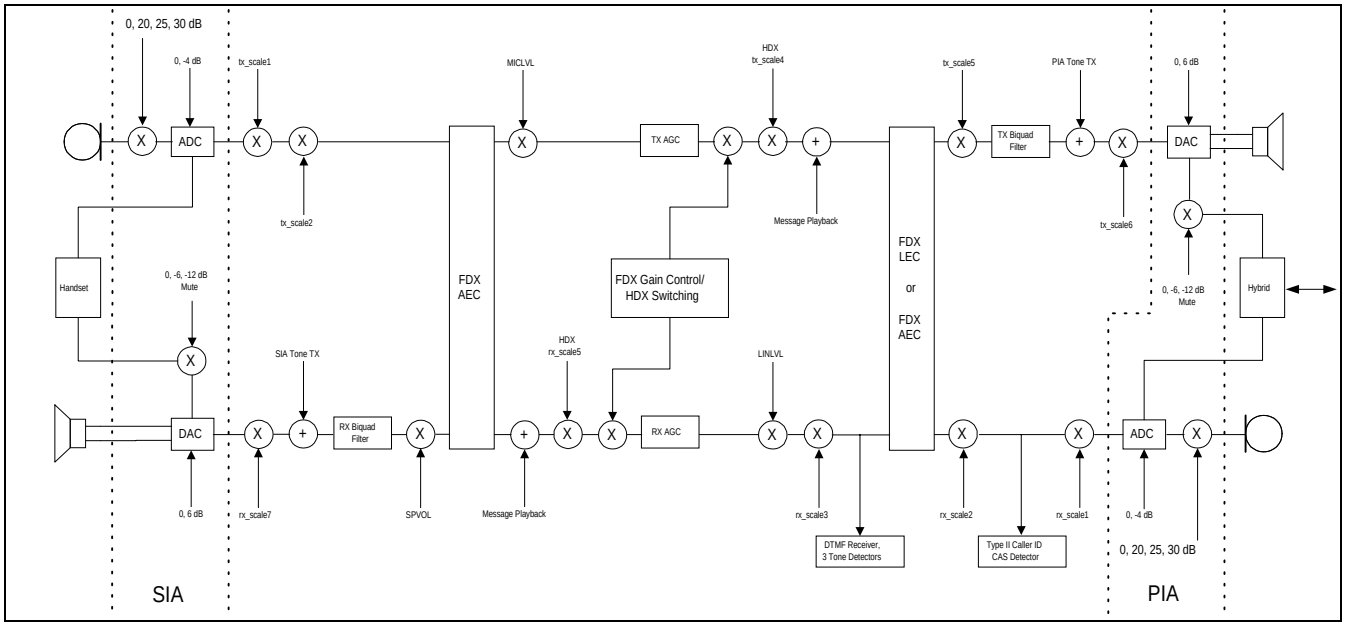

Figure 12-1. Speakerphone Diagram

12.2 SPEAKERPHONE RAM ACCESS

Table 12-1. Speakerphone RAM Access Codes - SBRAM

No.[1]	Function	SBRAMx	BRx	CRx	IOx	AREXx	ADDx	SBADxM	SBADxL	Read Reg. No.
1	Speakerphone Line Echo Suppressor	1	0	0	0	0	N/A	0C	A5	0,1
2	Speakerphone Transmit AGC Reference Level	1	0	0	0	0	N/A	0C	CC	0,1
3	Speakerphone Transmit AGC Slew Rate	1	0	0	0	0	N/A	0D	25	0,1
4	Speakerphone Receive AGC Reference Level	1	0	0	0	0	N/A	0C	E7	0,1
5	Speakerphone Receive AGC Slew Rate	1	0	0	0	0	N/A	0D	26	0,1
6	Speakerphone Transmit Speech Hangover	1	0	0	0	0	N/A	0D	0F	0,1
7	Speakerphone Receive Speech Hangover	1	0	0	0	0	N/A	0D	1E	0,1
8	Speakerphone Volume Range	1	0	0	0	0	N/A	0C	98	0,1
9	Speakerphone Line Volume Control	1	0	0	0	0	N/A	0C	A9	0,1
10	AEC Tap Length	1	0	0	0	0	N/A	0C	48	0,1
11	LEC Tap Length	1	0	0	0	0	N/A	0C	0E	0,1
12	Transmit AGC Gain (Programmable when AGC disabled)	1	0	0	0	0	N/A	0C	D5	0,1
13	Receive AGC Gain (Programmable when AGC disabled)	1	0	0	0	0	N/A	0C	F0	0,1
14	PIA Tone 1 Frequency	1	0	0	0	0	N/A	0C	1B	0,1
15	SIA Tone 1 Frequency	1	0	0	0	0	N/A	0C	22	0,1
16	PIA Tone 2 Frequency	1	0	0	0	0	N/A	0C	1C	0,1
17	SIA Tone 2 Frequency	1	0	0	0	0	N/A	0C	23	0,1
18	PIA Tone 1 Transmit Level	1	0	0	0	0	N/A	0C	19	0,1
19	SIA Tone 1 Transmit Level	1	0	0	0	0	N/A	0C	20	0,1
20	PIA Tone 2 Transmit Level	1	0	0	0	0	N/A	0C	1A	0,1
21	SIA Tone 2 Transmit Level	1	0	0	0	0	N/A	0C	21	0,1
22	PIA Conversation Recording Scale (PIASCF)	1	0	0	0	0	N/A	0C	29	0,1
23	SIA Conversation Recording Scale (SIASCF)	1	0	0	0	0	N/A	0C	2A	0,1
24	tx-scale1	0	0	1	0	0	96	N/A	N/A	0,1
25	tx_scale2	1	0	0	0	0	N/A	0C	BC	0,1
26	tx_scale4	1	0	0	0	0	N/A	0C	B1	0,1
27	tx_scale5	1	0	0	0	0	N/A	0C	16	0,1
28	tx_scale6	1	0	0	0	0	N/A	0C	1F	0,1
29	rx_scale1	0	0	1	0	0	0	N/A	N/A	2,3
30	rx_scale2	1	0	0	0	0	N/A	0C	0F	0,1
31	rs_scale3	1	0	0	0	0	N/A	0C	14	0,1
32	rx_scale5	1	0	0	0	0	N/A	0C	B2	0.1
33	rx_scale7	1	0	0	0	0	N/A	0C	26	0,1

Notes:

1. For all accesses, DRx = 0.
2. Read Reg. No. column only shows the registers to use when x = 1. When x = 2, the Read Reg. No. column value must be added to 10h.

No. 1 Speakerphone Line Echo Suppresser

Speakerphone line echo suppresser is a switching loss inserted in the receive (speaker) path and is enabled only in the transmit mode (TXH (18:4) = 1, RXH (18:3) = 0). The loss should be adjusted so the hybrid residual echo will not be heard at maximum speaker volume control setting. The setting of this parameter is purely subjective and will not affect any other parts of the speakerphone. The default value is loaded each time the modem is configured to Speakerphone Mode (CONF = 91h,93h,95h,99h.)

Format: 16 bits, positive, two's complement

Equation: Loss = $(10^{[x/20]})(32767)$

Where: x = desired loss in dB.

Range: 07FFh - 7FFFh

Default Value: 2000h (-12 dB)

No. 2 Speakerphone Transmit AGC Reference Level

Energy reference level for microphone AGC in speakerphone operation. When microphone signal energy is below the AGC reference level, a gain will be added till the signal energy after AGC reaches the reference level. When microphone signal energy is greater than the AGC reference level, a loss will be inserted until the signal energy after AGC drops to the reference level. The default value is loaded each time the modem is configured to Speakerphone Mode (CONF = 91h,93h,95h,99h.)

Format: 16 bits, positive, two's complement

Equation: Level = $(10^{[x//20]})(32767)$

Where: x = desired level in dB.

Range: 040Ch - 16C3h (-30 dB to -15 dB) referenced to maximum digital signal (7FFFh)

Default Value: 16C3h (-15 dB)

No. 3 Speakerphone Transmit AGC Slew Rate

The AGC slew rate determines how rapidly the AGC algorithm tracks the microphone input voice signal. Larger/smaller slew rate values correspond to faster/slower average energy convergence to the AGC reference level. The default value is loaded each time the modem is configured to Speakerphone Mode (CONF = 91h,93h,95h,99h.)

Format: 16 bits, positive, two's complement

Equation: Signal = Signal $1+\left(\frac{512}{32767}\right)$

Range: 100h-400h

Default Value: 200h

No. 4 Speakerphone Receive AGC Reference Level

Averaged energy reference level for speaker AGC in speakerphone operation. When line input signal energy is below its AGC reference level, a gain will be added till the signal energy after AGC reaches the reference level. When line input signal energy is greater than its AGC reference level, a loss will be inserted until the signal energy after AGC drops to the reference level. The default value is loaded each time the modem is configured to Speakerphone Mode (CONF = 91h,93h,95h,99h.)

Equation: Level = $(10^{[x /20]})(32767)$

Where: x = desired level in dB.

Range: 040Ch - 16C3h (-30 dB to -15 dB) referenced to maximum digital signal (7FFFh)

Default Value: 813h (-24 dB)

No. 5 Speakerphone Receive AGC Slew Rate

The AGC slew rate determines how rapidly the AGC algorithm tracks the line input voice signal. Larger/smaller slew rate values correspond to faster/slower average energy convergence to the AGC reference level. The default value is loaded each time the modem is configured to Speakerphone Mode (CONF = 91h,93h,95h,99h.)

Format: 16 bits, positive, two's complement

Equation: Signal = Signal * $1+\left(\frac{512}{32767}\right)$

Range: 100h - 400h

Default Value: 200h

No. 6 Speakerphone Transmit Speech Hangover

In order to avoid choppy sounds for weak voice signals whose energy is not much different from the noise floor, a minimum on-time (hangover) is usually added to the speech detector. When transmit speech is gone, the hangover will gradually decrement to 0 and TXH (18:4) set to 0. The default value is loaded each time the modem is configured to Speakerphone Mode (CONF=91h,93h,95h,99h.)

Format: 16 bits, positive, two's complement

Equation: Hangover = 8 * x

Where: x = desired hangover time in ms.

Range: 0001h - 0FA0h

Default Value: 0640h (200 ms)

No. 7 Speakerphone Receive Speech Hangover

In order to avoid choppy sounds for weak voice signals whose energy is not much different from the noise floor, a minimum on-time (hangover) is usually added to the speech detector. When receive speech is gone, the hangover will gradually decrement to 0 and RXH (18:3) set to 0. The default value is loaded each time the modem is configured to Speakerphone Mode (CONF=91h,93h,95h,99h.)

Format: 16 bits, positive, two's complement

Equation: Hangover = 8 * x

Where: x = desired hangover time in ms.

Range: 0001h - 0FA0h

Default Value: 0640h (200 ms)

No. 8 Speakerphone Volume Range

The volume control provides a 2 dB loss to the SIA DAC output each time control bit VOLDWN (OE:5) is set. The speakerphone volume range parameter limits the maximum loss.

Format: 16 bits, positive, two's complement

Equation: $(10^{[(x+1)/20]})(32768)$

Where: x = lower range limit in dB

Range: 0004h - 7FFFh

Default Value: 048Bh (-30 dB)

No. 9 Speakerphone Line Volume Control

Allows the host to change the transmit output level of the PIA DAC without causing instability in the speakerphone algorithm's gain balance.

Format: 16 bits, positive, two's complement

Equation: Loss = $(10^{[x/20]})(32767)$

Where: x = desired loss in dB.

Range: 0000h - 7FFFh

Default Value: 0800h (-24 dB)

No. 10 AEC Tap Length

Acoustic Echo Canceller tap length. Could be used in intercom support mode if a decrease in tap length is desired.

Format: 8 bits

Equation: tap length = (x+1)*2

Range 0000h-00FFh

Default Value: 00FFh(max, 512 taps)

No. 11 LEC Tap Length

Line Echo Canceller tap length. Used in intercom support mode to increase the length of LEC for the LEC to act as a second AEC.

Format: 8 bits

Equation: tap length = (x+1)*2

Range 0000h-00FDh

Default Value: 0054h(170 taps)

No. 12 Transmit AGC Gain (Programmable when AGC disabled)

Provides constant transmit gain when transmit AGC is disabled.

Format: 8 most significant bits integer. 8 least significant bits fractional.

Equation: Gain = $\left(\frac{x}{256}\right)$

Range: 0100h-1000h (0 dB - 24 dB)

Default 0100h (0 dB)

No. 13 Receive AGC Gain (Programmable when AGC disabled)

Provides constant receive gain when receive AGC is disabled.

Equation: Gain = $\left(\frac{x}{256}\right)$

Range: 0100h-1000h (0 dB - 24 dB)

Default 0100h (0 dB)

No. 14 PIA Tone 1 Frequency
No. 15 SIA Tone 1 Frequency
No. 16 PIA Tone 2 Frequency
No. 17 SIA Tone 2 Frequency

Format: 16 bits, unsigned

Equation: N = 8.192 x Frequency (in Hz)

Convert N to hexadecimal then store in RAM.

No. 18 PIA Tone 1 Transmit Level
No. 19 SIA Tone 1 Transmit Level
No. 20 PIA Tone 2 Transmit Level
No. 21 SIA Tone 2 Transmit Level

Format: 16-bits, positive, twos complement

Range: 0000h-7FFFh

Calculate the transmit output level (power) of each tone independently by using the equation for Transmit Output Level. See Section 4.

No. 22 PIA Conversation Recording Scale (PIASCF)

The microphone output to line is scaled by PIASCF for conversation recording.

Format: 16 bits, positive, two's complement

Range: 0000h - 7FFFh

Default $4000 (-6 dB)

No. 23 SIA Conversation Recording Scaler (SIASCF)

The speaker output to line is scaled by SIASCF for conversation recording

Format: 16 bits, positive, two's complement

Range: 0000h - 7FFFh

Default $4000 (-6 dB)

No. 24 tx-scale1-microphone input scaler

Allows the microphone input signal to be scaled down before AEC.

Format: 16 bits, positive, two's complement

Range: 0000h - 7FFFh

Default Value: $7FFF (0 dB)

No. 25 tx_scale2-microphone input scaler

Allows the microphone input signal to be scaled up or down before AEC.

Format: 8 most significant bits(msb) integer, 8 least significant bits(lsb) fractional

Equation: Gain = $\left(\frac{x}{256}\right)$

Range: 0000h-7FFFh

Default Value: $0100 (0 dB)

No. 26 tx_scale4-transmit scaler for HDX speakerphone mode

Allows more transmit gain or loss to be added for HDX speakerphone mode.

Format: 9 msb integer, 7 lsb fractional

Equation: Gain = $\left(\frac{x}{128}\right)$

Range: 0000h-7FFFh

Default Value: $0080 (0 dB)

No. 27 tx_scale5-transmit scaler

Allows transmit signal after LEC to be scaled down.

Format: 16 bits, positive, two's complement

Range: 0000h-7FFFh

Default: $7FFF (0 dB)

No. 28 tx_scale6 -transmit scaler

Allows transmit signal before DAC to be scaled down.

Format: 16 bits, positive, two’s complement

Range: 0000h-7FFFh

Default: $0F2C (-18.5 dB)

No. 29 rx_scale1-line input scaler

Allows line input to be scaled down before LEC.

Format: 16 bits, positive, two’s complement

Range: 0000h-7FFFh

Default: $3855 (-7.13 dB)

No. 30 rx_scale2-line input scaler

Allows gain or loss to the line input before LEC.

Format: 8 msb integer, 8 lsb fractional

Range: 0000h-7FFFh

Default: $7FFF (0 dB)

No. 31 rx_scale3 receive scaler

Allows Line Echo Canceller output signal to be attenuated.

Format: 16 bits, positive, two’s complement

Range: 0000h-7FFFh

Default: $7FFF (0 dB)

No. 32 rx_scale5 receive scaler for HDX speakerphone mode

Allows more receive gain or loss to be added for HDX speakerphone.

Format: 9 msb integer, 7 lsb fractional

Range: 0000h-7FFFh

Default: $0080 (0 dB)

No. 33 rx-scale7 receiver scaler

Allows receive signal to be scale down before DAC.

Format: 16 bits, positive, 2’s compliment

Range: 0000h-7FFFh

Default: $0F2C (-18.5 dB)

12.3 SPEAKERPHONE DESIGN ISSUES

A speakerphone design includes the speakerphone hardware design and the software control to make the speakerphone functional. The FDX speakerphone is "gain-balanced"—echo cancellers are used to provide necessary microphone and speaker gain without feedback. Therefore, the following conditions must be satisfied in the FDX speakerphone operating environment.

Note: The speakerphone will not become full-duplex until the convergence process of its echo cancellers is in progress.

1. The line echo canceller requires that hybrid echo return loss, measured from the receive signal before the LEC to the transmit signal after the LEC (see Figure 12-1) to be less than –6 dB at all pass-band frequencies and gain settings.
2. After the placements of the microphone and speaker are fixed in the product under design, the acoustic echo canceller requires the acoustic echo return loss, measured from the transmit signal before the AEC to the receive signal after the AEC (see Figure 12-1) to be less than -6dB at all pass-band frequencies and gain settings.
3. A directional electret condenser microphone that provides more acoustic decoupling from speaker to microphone, better noise immunity, and flatter spectrum characteristics, is strongly recommended in the design. Better acoustic decoupling allows higher maximum speaker volume. Moreover, the analog codecs must not be overshot or overloaded by echoes in order to maintain system linearity. This is important for the echo cancellers to function properly.

A unique feature of the FDX Speakerphone is that gain balancing is fully automatic. Depending on the design and real-time operating conditions, the speakerphone can automatically fall back to pseudo-duplex operation. When the host reconfigures the speakerphone or changes any parameters in real time, the speakerphone algorithm readjusts internal variables to deliver the best performance.

12.3.1 Microphone/Speaker Placements

In most product designs, orienting the microphone and speaker in opposite directions and maximizing the distance in between them will help minimize acoustic coupling from the speaker to the microphone. For example, the microphone can be placed in the right-front corner facing forward and speaker can be placed at the left-back corner facing up or backward. A sophisticated placement configuration can increase the maximum allowable speaker loudness typically by 10-20 dB.

12.3.2 Microphone and Speaker Gains

When the placements of the microphone and speaker are fixed, the coupling characteristics through open air is basically determined. The analog pre-amplification gain for the selected microphone element must be determined so that the input signal falls within the normal input range of the codec when talking loud at one foot distance from the microphone. Two clamping diodes should be used on the microphone output signal before the DC-blocking (see Figure 14-4).

Minimum comfortable speaker loudness for a specific application determines the minimum amplification gain in the speaker driver. This gain can be increased as long as condition (2) stated above is met. If the gain for the minimum desired loudness violates the condition, the microphone pre-amplification gain must be reduced and then compensated through the software microphone volume control. Each time a gain is added in the software, the speakerphone becomes more switching depending on the other operating conditions. This is the penalty caused by a poor acoustic separation.

12.3.3 Hybrid Interface

In order for the line echo canceller to function properly, the hybrid interface must be linear and condition (1) stated above must be met. It is recommended that the same gain factor and frequency response be used as used in Figure 14-3 for normal 2-wire telephone interface.

12.4 SPEAKERPHONE MODES

12.4.1 FDX Speakerphone Mode

After the CONF control bits (06:0-7) are loaded with 91h, 93h, 95h, or 99h and the SETUP bit (1F:0) is set, the speakerphone defaults to the following:

SP/HS = 1; FDX Speakerphone Mode.

MICLVL = 01; Microphone volume level = +6 dB.

MUTES = 1; Microphone muted for dial-tone passing through un-switched.

MUTEP = 0; Speaker voice channel activated.

VOLDWN = 0; No speaker volume decrement. Speaker gain setting defaults to -10 dB

VOLUP = 0; No speaker volume increment.

TXAGC = 1; Microphone AGC enabled.

RXAGC = 1; Speaker AGC enabled.

TTONEE = 0; Tone transmit mode disabled.

LINLVL = 00; Line volume level = 0 dB.

INTRCM = 0; Intercom disabled.

RXH = 0; No receive signal detected.

TXH = 0; No transmit signal detected.

TXSEN = 0; Transmit detector sensitivity during double talk not more sensitive.

SIA = 0; SIA configured to linein, lineout pair for input, output

HDSPK = 0; Half duplex speakerphone mode disabled.

TXBQ = 0; Transmit or microphone Biquad filter disabled.

RXBQ = 0; Receive or line Biquad filter disabled.

TONESE = 0; Speaker tone transmit disabled.

TONEPE = 0; Microphone tone transmit disabled.

Setting SP/HS control bit to a 1 configures the FDX Speakerphone Mode. In this mode, the microphone volume is controlled by the MICLVL bits; the line volume is controlled by the LINLVL bits; the speaker volume is controlled by the VOLUP and VOLDWN bits; the speaker and microphone channels can be muted by setting the MUTEP and MUTES bits to a 1, respectively; and their AGC functions can be enabled by setting the AGCPE and AGCSE bits to a 1, respectively. The TTONEE bit should remain at a 0 in this mode.

As soon as the speakerphone connects through to the dialed party for FDX speakerphone operation, the MUTES bit must be reset to a 0 to activate the microphone voice channel. Tx_scale4 and tx_scale5 are not designed to be used in the FDX mode. They are used only for HDX mode for high volume.

12.4.2 Half Duplex Speakerphone Mode

Setting HDSPK control bit to a 1 configures the HDX Speakerphone Mode. In Half Duplex Speakerphone mode, both the AEC and LEC are bypassed. HDX speakerphone transmits in one direction at a time, transmit or receive. Whoever talks first has their voice passed (near-end talker or far-end talker). However if there is a silence gap in the person's (who has the passing channel) speech, the other channel may be able to interrupt and cut in. If easier interruption is desired, the hangover counters for both the transmit and receive detectors should be decreased to allow more silence gaps and vice versa. The mode should be used if high volume voice transmission is desired. Tx_scale4 and tx_scale5 are used to increase gain.

12.4.3 FDX and HDX Intercom Support Modes

Setting INTRCM control bit to a 1 configures the Intercom Speakerphone Mode. In Intercom mode, AEC and LEC tap length are programmable with maximum AEC tap length of 512 and maximum LEC (now acting as an AEC) length of 508. For the intercom feature, the original LEC acts as another AEC for room echo cancellation. HDX intercom mode is used if high volume voice transmission is desired.

12.4.4 Tone Transmit Mode

While operating in the Speakerphone Modes, tone transmission is available to either the line and/or speaker at the same time. There are two tone transmitters, one for the line, and one for the speaker. Different tones can be played on each channel and each channel tone can be a single-tone, dual-tone, or melody ring-tone. Frequency and output level information for each desired tone from the PIA or SIA must be programmed prior to activation.

First, the TTONEE control bit must be set to a 1 to inform the modem that speakerphone tone transmit mode is engaged. The modem will freeze the adaptation of the echo cancellers and start to check the TONEIE and TONEXE bits. Tone is transmitted to the line and/or speaker as long as the respective TONEIE and/or TONEXE bit stays at a 1. Keeping the TTONEE bit to a 1 and toggling the TONEIE and/or TONEXE bit will generate the on and off periods of the tone. Setting any of these two bits to a 1 will silence the corresponding voice channel until the TTONEE bit is reset to a 0.

For example, if you select the TONEIE bit first, then turn on the TONEXE bit, the microphone and speaker voice will be both disabled. When you finish transmitting tones, you must reset the TTONEE bit to enable both microphone and speaker voices, or reset-then-set the TTONEE bit to enable one voice and continue tone transmit on the other channel depending on the status of the TONEIE and TONEXE bits.

The two separate dual-tone transmitters should be programmed to their desired frequencies and levels. Each transmitter has four parameters: tone 1 frequency, tone 1 transmit output level, tone 2 frequency, and tone 2 transmit output level (see Table 12-1).

12.4.5 Handset Mode

The Handset Mode provides a private means of conversation which may be necessary in some occasions. Resetting SP/HS control bit to a 0 configures the Handset Mode. In this mode, a regular handset in place of the microphone and speaker arrangement is assumed. All the AGC adaptation processes are frozen at their previous gain factors and the microphone AGC is bypassed. If the speaker AGC is enabled, it will keep using the latest gain factor determined in the FDX Speakerphone Mode, otherwise the AGC gain will be forced to unity. Muting, tone generation, and volume level controls for both microphone and speaker channels are available, just as in the FDX Speakerphone Mode.

The acoustic echo canceller is bypassed in the handset mode. However, the coefficients of the canceller are maintained in order for the canceller to resume functioning quickly when configured back to the FDX Speakerphone Mode.

A side-tone simulator is provided which takes the mouth-piece signal through an attenuator and mixes the attenuated signal with the far-end signal before sending it to the ear-piece. The attenuation level is controlled by the ECHOAT bits (0F:0-1):

Bit 1	Bit 0	Attenuation
0	0	∞ dB (default)
0	1	18 dB
1	0	12 dB
1	1	6 dB

12.4.6 Speakerphone Modes and Active Bits

The active bits in different speakerphone modes are listed in Table 12-1.

Table 12-2. Register Location 0E Use

	Bit							
	TTONEE	VOLUP	VOLDWN	SP/HS	MUTEI	MUTEX	MICLVL	
Mode	7	6	5	4	3	2	1	0
FDX Speakerphone /Intercom Support	x	x	x	x	x	x	x	x
HDX Speakerphone /Intercom Support	x	x	x	x	x	x	x	x
Conversation Recording	x	x	x	x	x	x	x	x
Handset	x	x	x	x	x	x	x	x
Microphone Mute	x	x	x	x	x	x		
Speaker Mute	x			x	x	x	x	x

Note:

1. "x" = the corresponding bit is active.

Table 12-3. Register Location 0F Use

	Bit							
	-	-	-	AGCIE	AGCXE	-	ECHOAT	
Mode	7	6	5	4	3	2	1	0
FDX Speakerphone /Intercom Support				x	x			
HDX Speakerphone /Intercom Support				x	x			
Conversation Recording				x	x			
Tone Transmit								
Handset				x			x	x
Microphone Mute				x				
Speaker Mute					x			

Note:

1. "x" means that the corresponding bit is active.

Table 12-4. Register Location 18 Use

Mode	Bit							
	HDSPK	SIAHND	TXSEN	TXH	RXH	INTRCM	LINLVL	
	7	6	5	4	3	2	1	0
FDX Speakerphone /Intercom Support	x		x	x	x	x	x	x
HDX Speakerphone /Intercom Support	x	x	x	x	x	x	x	x
Conversation Recording	x	x	x	x	x	x	x	x
Tone Transmit		x						
Handset	x	x	x	x	x	x	x	x
Microphone Mute	x				x	x	x	x
Speaker Mute				x		x		

Note:

1. "x" means that the corresponding bit is active.

Table 12-5. Register Location 19 Use

Mode	Bit							
	-	TONEPE	TONESE	-	-	-	RXBQ	TXBQ
	7	6	5	4	3	2	1	0
FDX Speakerphone /Intercom Support							x	x
HDX Speakerphone /Intercom Support							x	x
Conversation Recording							x	x
Tone Transmit		x	x					
Handset							x	x
Microphone Mute							x	x
Speaker Mute							x	x

Note:

1. Corresponding bit is active.

12.5 SPEAKERPHONE CONTROL

While in configuration 91h, 93h, 95h, and 99h the speakerphone control bits at interface register locations 0Eh, 0Fh, 18h, and 19h can be used for most common speakerphone function controls in real time. Overwriting these registers with different control values will either alter the operating parameters or reconfigure the speakerphone into different operation modes. These include mode select, volume control, muting, tone transmit, AGC enable/disable and handset operation. Other advanced features are also provided allowing more controls over the speakerphone voice processing.

12.5.1 Speakerphone Interface Control Registers

Interface Register 0Eh (Default = 15h):

Bit 0-1 MICLVL (Microphone Volume Level).
These two bits control the microphone volume level.

Bit 2 MUTES (Mute SIA ADC).
When set, the microphone is muted.

Bit 3 MUTEP (Mute PIA ADC).
When set, the speaker is muted.

Bit 4 SP/HS (Speakerphone/Handset Switch).
1 = speakerphone
0 = handset (replacing speaker/microphone setup.)

Bit 5 VOLDWN (Volume Down).
When set, the speaker volume is decreased by 2 dB.

Bit 6 VOLUP (Volume Up).
When set, the speaker volume is increased by 2 dB.

Bit 7 TTONEE (Tone Transmit Enable).
When set, tone transmit mode is enabled.

Before switching out of Speakerphone Mode, set both MUTES and MUTEP bits for at least 10 ms. This will allow the modem to clear out any left-over samples in the analog codec interface processing.

Interface Register 0Fh (Default = 18h):

Bit 0-2 N/A (Reserved).

Bit 3 TXAGC (AGC in SIA ADC Enable).
When set, the microphone AGC is enabled.

Bit 4 RXAGC (AGC in PIA ADC Enable).
When set, the speaker AGC is enabled.

Bit 5-7 N/A (Reserved).

Interface Register 18h (default = 0h):

Bit 0-1 LINLVL (Line Volume Level)

These two bits controls line (input) volume level.

Bit 2 INTRCM (Intercom support on)

When set, intercom mode is on

Bit 3 RXH (Receive speech on with hangover)

When set, the receive speech detector is detecting speech.

Bit 4 TXH (Transmit speech on with hangover)

When set, the transmit speech detector is detecting speech.

Bit 5 TXSEN (Transmit detector sensitivity during double talk)

When set, the transmit speech detector is more sensitive lower/softer voice levels

Bit 6 SIAHND (SIA handset mode setting)

When set, SIA uses mic, spk pair for input output

else, it uses linein, lineout pair. Can be used in handset mode.

Bit 7 HDSPK (Half duplex speakerphone enable)

When set, half duplex speakerphone mode is enabled

Interface Register 19h (default=0h):

Bit 0 TXBQ (Transmit Biquad filter enable)

When set, transmit or microphone Biquad filter is enabled.

Bit 1 RXBQ (Receive Biquad filter enabled)

When set, receive or speaker Biquad filter is enabled.

Bit 2-4 N/A (Reserved)

Bit 5 TONESE (Tone transmit to speaker enable)

When set, tone is transmitted to speaker.

Bit 6 TONEPE (Tone transmit to line enable)

When set, tone is transmitted to line.

Bit 7 N/A (Reserved)

12.5.2 Biquad Filters

Host programmable transmit and receive biquad filters are provided at line output and speaker output. (See Figure 12-1.) For more information, refer to Section 8.6.

12.5.3 Microphone Volume Control

The microphone volume control can be used either as a software compensator for the acoustic decoupling design or as a true four-level volume control. Microphone volume control (compensation gain) is added to the digital signal before the microphone AGC process. This prevents the possibility of digital overflow in the event of large microphone compensation on top of high AGC output level. The microphone volume control bits MICLVL (0E:0-1) can be adjusted at any time.

Bit 1	Bit 0	Gain	Level
0	0	0 dB	Low
0	1	+6 dB	Medium (default)
1	0	+9.5 dB	Medium-High
1	1	+12 dB	High

An internal software limiter is attached to this volume control. If signal overflow or underflow situation occurs after applying the volume control gain, the signal will be limited to 7FFFh or 8000h in the modem depending on the signal polarity. The default microphone volume level is "Medium" (+6 dB).

12.5.4 Line Volume Control

The line volume is used either as a software compensator for the acoustic decoupling design, or as a true four-level volume control. Line volume control (compensation gain) is added to the digital signal before the AGC process. This prevents the possibility of digital overflow in the event of large line compensation on top of high AGC output level. The line volume control bits LINLVL (0E:0-1) can be adjusted at any time.

Bit 1	Bit 0	Gain	Level
0	0	0 dB	Low
0	1	+6 dB	Medium (default)
1	0	+9.5 dB	Medium-High
1	1	+12 dB	High

An internal software limiter is attached to this control. If signal overflow or underflow occurs after applying the volume control gain, the signal will be limited to 7FFFh or 8000h in the modem depending on the signal polarity. The default line volume level is "Low" (0 dB).

12.5.5 Speaker Volume Control

The digital speaker volume control, instead of a traditional analog potentiometer, should be used all the time in the Speakerphone Mode. Each time the speaker volume control level is changed, the acoustic echo level is changed accordingly. Therefore, the coefficients of the acoustic echo canceller must be scaled to reflect the echo change. Otherwise, the acoustic echo canceller will lose tracking of the echo change and must re-adjust all the coefficients again. The full-duplexity is degraded until the canceller can reconverge. Changing analog potentiometer setting will most likely cause the acoustic echo canceller to go through the convergence process again.

The digital speaker volume is controlled through the VOLUP and VOLDWN bits. Each time the VOLUP bit is set to a 1, the volume increases by 2 dB. Accordingly, each time the VOLDWN bit is set to a 1, the volume decreases by 2 dB. There are fifteen 2 dB increment and decrement steps representing 30 dB volume control range. Volume control range is programmable. The VOLUP and VOLDWN control bits are automatically reset to a 0 after the volume has been adjusted.

VOLUP	VOLDWN	Volume
0	0	No change (default)
0	1	Down by 2 dB
1	0	Up by 2 dB
1	1	No change

The default speaker volume control is -10 dB. It is advised to check the dial-tone loudness at this setting. Adjust the volume control, if necessary, to make sure its loudness is at the right level. Disabling the speaker AGC function may be considered during the dial-tone reception. At the end of dial-tone, selecting Speakerphone Mode will reinitiate the AGC parameters. The microphone channel should be muted during the dial-tone reception.

12.5.6 Microphone and Speaker Muting

The muting function is available in both the Speakerphone Mode and the Handset Mode. Muting does not affect the use of tone transmit function or message playback. AGC functions can be left either enabled or disabled.

The muting function overwrites the output of the corresponding voice channel with zero, silencing the voice output. The rest of the muted voice channel still functions on the channel's voice input, keeping the echo canceller active, speech detector active, loop gain calculation active, and so on. The AGC update, if enabled, is active only if the other channel is not muted.

The channel not being muted is fully open with a fixed AGC (if enabled) gain determined prior to the muting of the other channel. Disabling the AGC function forces the AGC gain to unity. The channel's volume control can still be used to adjust the voice output level.

The host sets or releases the muting function through the MUTEP and MUTES bits.

MUTEP	MUTES	Action
0	0	No muting
0	1	Microphone muted (default)
1	0	Speaker muted
1	1	Both channels muted

12.5.7 Microphone and Speaker AGC

The microphone and speaker voice AGC algorithms are designed to raise or lower the channel's voice energy to a desired level. The AGCs can be enabled (set to a 1) or disabled (reset to a 0) through the AGCPE and AGCSE control bits. When enabled, the AGC involvement is controlled by the speech detector. When the talker is silent, the AGC is turned off to avoid amplification of noise. When speech is detected, the AGC process is activated in a fast-attack and slow-decay fashion, so that the AGC gain is applied to the signal appropriately.

The AGC gain adaptation, on the other hand, is a slow-rise and fast-drop process. The gain's rise time is controlled by the AGC slew rate. The long-term sample by sample, averaged signal energy after the AGC is calculated and compared with the AGC's reference level. When the signal energy is below its AGC reference level, the AGC gain will be increased till the signal energy reaches the reference level. When the signal energy is greater than its AGC reference level, the AGC gain will be decreased until the signal energy drops to the reference level. The maximum AGC gain is programmable in each voice channel. There is no low limit for the AGC compression loss.

Initially the AGC gain is set at its default maximum 18 dB in both the microphone and speaker channels. Due to the fast-drop nature of the algorithm, the convergence process of the AGC gain quickly settles down to reach the reference level. Each time the AGC function is disabled, the AGC gain is programmable.

The AGC slew rate and the reference level are separate parameters. But to tune up the slew rate, one should set the reference level first so that the slew rate can be adjusted accurately. Increasing the slew rate value linearly increases the AGC convergence speed.

When AGCs are disabled, a fixed programmable gain can be applied. The maximum programmable is limited to +24 dB. See Section 12.2 for more information.

12.5.8 Speech Detectors

Two speech detectors work together in the speakerphone. They are fully adaptive with room and line noise floors, and can distinguish true talkers from noise and echo feedback. The room speech detector detects the talker activities in the local room while the line speech detector detects the talker activities at the remote site.

Speech detectors activate or deactivate the AGCs depending on talker activity. When the talker is silent, the AGC is turned off to avoid noise amplifications. When speech is detected, the AGC process is activated. A minimum on-time is inserted in the speech detector to smooth the switching effect over weak sounds, especially for consonants at the end of a word or sound level very close to the noise floor.

Note: The switching here is different from that in half-duplex speakerphones where the voice channel is gated. In the FDX Speakerphone Mode, the voice channel gain is always maintained except for the AGC gain. Transmit speech hangover and receive speech hangover values can be optimized to each design.

Minimum On Time (ms) = Speech_hangover / 8.

When the local speech is detected, the transmit speech active bit TXH (18:4) is set to 1. When the far-end speech is detected, the receive speech active bit RXH (18:3) is set to 1. Each bit is reset to 0, respectively, when speech is not present.

12.5.9 Scaling of Transmit Output to Line

Transmit scale factors (tx_scale1 and tx_scale2) provide scaling of the SIA microphone input signal before the AEC. Transmit scale factors (tx_scale5 and tx_scale_6) provide scaling of the PIA line/speaker output signal after the LEC. Transmit scale factor tx_scale4 after the transmit AGC provides additional gain for HDX speakerphone.

Analog gains of 0, 20, 25, and 30 dB are provided at the SIA microphone input. Analog gains of 0, -6 or –12 dB are provided at the PIA line output (see Section 4-3).

12.5.10 Scaling of Receive Input to Speaker

Receive scale factors (rx_scale1 and rx_scale2) provide scaling of the PIA line/microphone input signal before the LEC and rx_scale3 provides scaling after the LEC. Receive scale factor rx_scale_7 provides scaling of the SIA speaker output signal after the AEC. Receive scale factor rx_scale5 after the receive AGC provides additional gain for HDX speakerphone.

12.6 CONVERSATION RECORDING AND MESSAGE PLAYBACK

When the ADPCM audio or Voice coder is enabled, conversation recording is enabled and transmit/receive samples before tx_scale6/rx_scale7 scale factors are summed together and recorded. When the decoder is enabled, conversation or messages recorded earlier can be played back and added to the transmit/receive signals after the application of tx_scale4/rx_scale5 scale factors without interruption during ongoing conversation. (See Figure 12-1.) Conversation recording provides volume control capabilities as follows:

Formula: Coder input = signal before tx_scale6 * PIASCF + signal before rx_scale7 * SIASCF where the default values for PIASCF and SIASCF are 4000h. PIASCF and SIASCF can be programmed for volume adjustments. (See Table 12-1). Decoder output scaling is provided by the Transmit Output Level/Scaling parameter (see Table 4-1).

12.7 TONE, DTMF, AND TYPE II CALLER ID CAS DETECTION

Three tone detectors operate with 8000 Hz sample rate. See Section 6.

The DTMF receiver is described in Section 3.2.

The Type II Caller ID CAS detector is described in Section 10.9.

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13. PERFORMANCE

13.1 TYPICAL BIT ERROR RATES

Typical bit error rate (BER) performance of the modem is shown in Figure 13-1. Performance is specified for a test configuration conforming to that specified in ITU-T Recommendation V.56. Bit error rates are measured for a flat line at a received line signal level of –20 dBm.

13.2 TYPICAL PHASE JITTER

At 2400 bps, the modem exhibits a bit error rate of 10^{-6} or less with a signal-to-noise ratio of 12.5 dB in the presence of 15° peak-to-peak phase jitter at 150 Hz or with a signal-to-noise ratio of 15 dB in the presence of 30° peak-to-noise phase jitter at 120 Hz.

At 4800 bps (V.27 ter), the modem exhibits a bit error rate of 10^{-6} or less with a signal-to-noise ratio of 19 dB in the presence of 15° peak-to-peak phase jitter at 60 Hz.

At 7200 bps (V.29), the modem exhibits a bit error rate of 10^{-6} or less with a signal-to-noise ratio of 25 dB in the presence of 12° peak-to-peak phase jitter at 300 Hz.

At 9600 bps (V.29), the modem exhibits a bit error rate of 10^{-6} or less with a signal-to-noise ratio of 23 dB in the presence of 10° peak-to-peak phase jitter at 60 Hz. The modem exhibits a bit error rate of 10^{-5} or less with a signal-to-noise ratio of 23 dB in the presence of 20° peak-to-peak phase jitter at 30 Hz.

13.3 DTMF PERFORMANCE

DTMF performance is described in Table 13-1.

Table 13-1. DTMF Receiver Performance Characteristics

Characteristic	Minimum[10]	Maximum[10]	Units	Programmable?	Notes
Acceptable Twist	–8.2 ±0.2	+4.3 ±0.2	dB	Yes	1, 2, 4, 5, 6, 7, 9
Acceptable Positive Frequency Deviation		+1.5 to +3.2	%	Yes	1, 3, 4, 5, 6, 7, 9
Acceptable Negative Frequency Deviation	–2.1 to –2.8		%	Yes	1, 3, 4, 5, 6, 7, 9
Required On-Time	40.0 ±1.0		ms	Yes	2, 3, 4, 5, 6, 7, 9
Required Off-Time	40.0 ±1.0		ms	Yes	2, 3, 4, 5, 6, 7, 9
Required Cycle-Time	93.0 ±1.0		ms	Yes	2, 3, 4, 5, 6, 7, 9
Dynamic Range	-43.0	0.0	dBm	Yes	1, 2, 3, 5, 6, 7, 9
Signal-to-Noise Ratio	12.0		dB	-	1, 2, 3, 4, 5, 6, 7, 9
Talk Off	2	3	Hits	-	8, 9

Notes:

1. On-time = 50 ms, off-time = 50 ms, and cycle-time = 100 ms.
2. Nominal DTMF frequencies.
3. Both tones of DTMF symbol have equal amplitude—0 dB twist.
4. Received signal level = –35.0 dBm.
5. All 16 DTMF symbols transmitted.
6. Error rate of 1/10,000 or less.
7. TAS Telephone Network Simulator Model #112, flat line transmission path.
8. Mitel CM7291 DTMF Receiver Test Cassette.
9. All DTMF receiver parameters are equal to their default values.
10. Values shown are for DTMF Receiver (configuration code 21h).

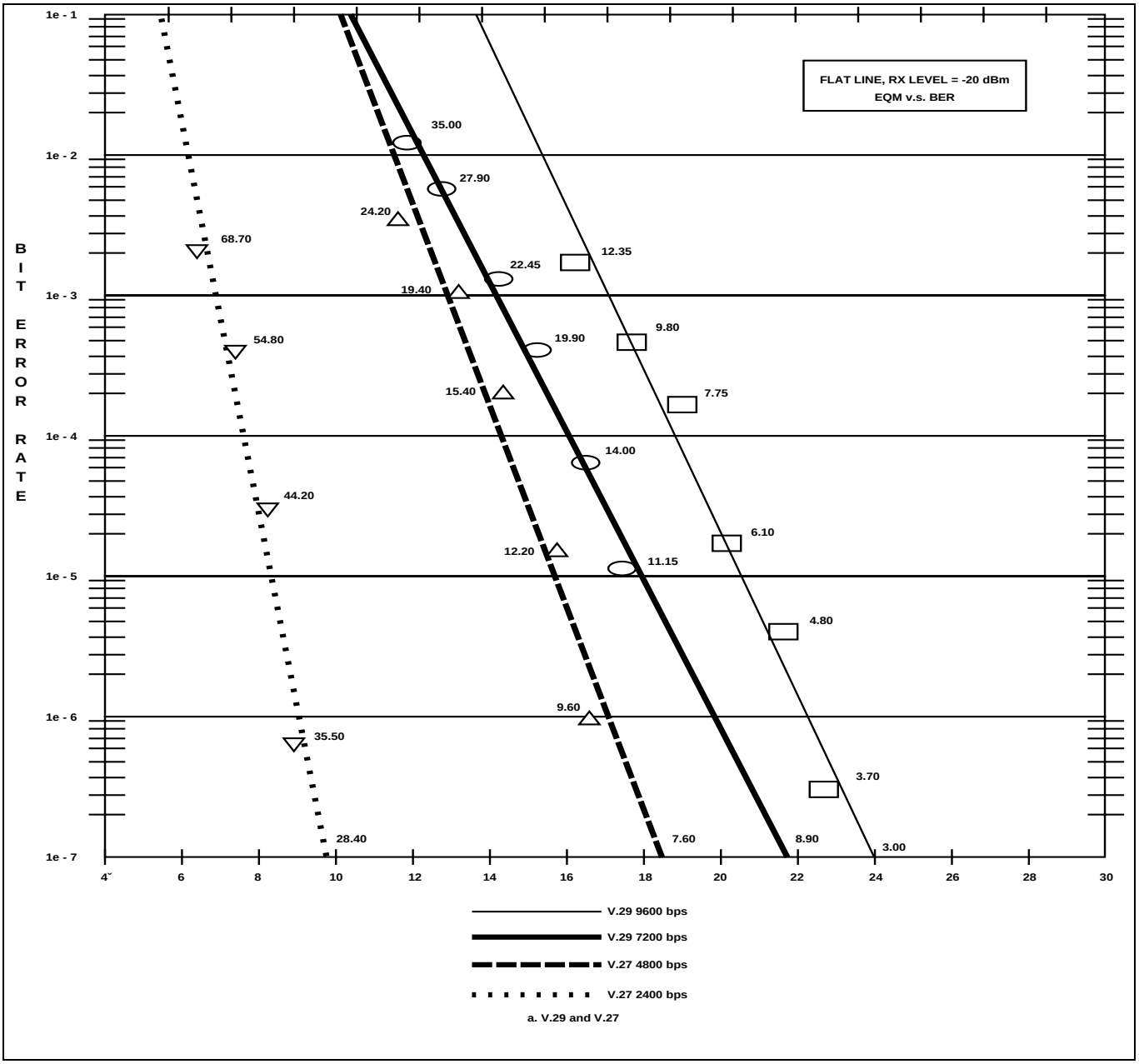

Figure 13-1. Typical Bit Error Rate (BER) Curves (V.29 and V.27)

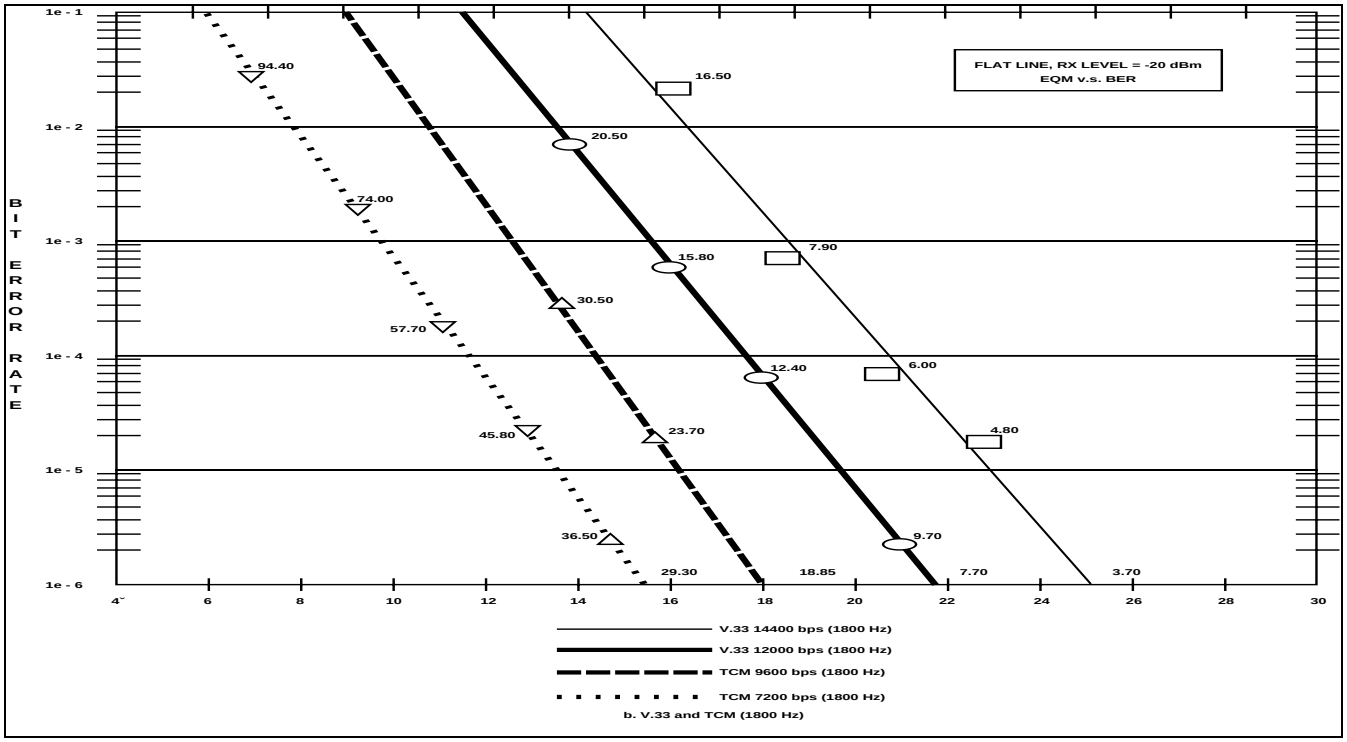

Figure 13-1. Typical Bit Error Rate (BER) Curves (V.33 and TCM (1800 Hz)) (Cont'd)

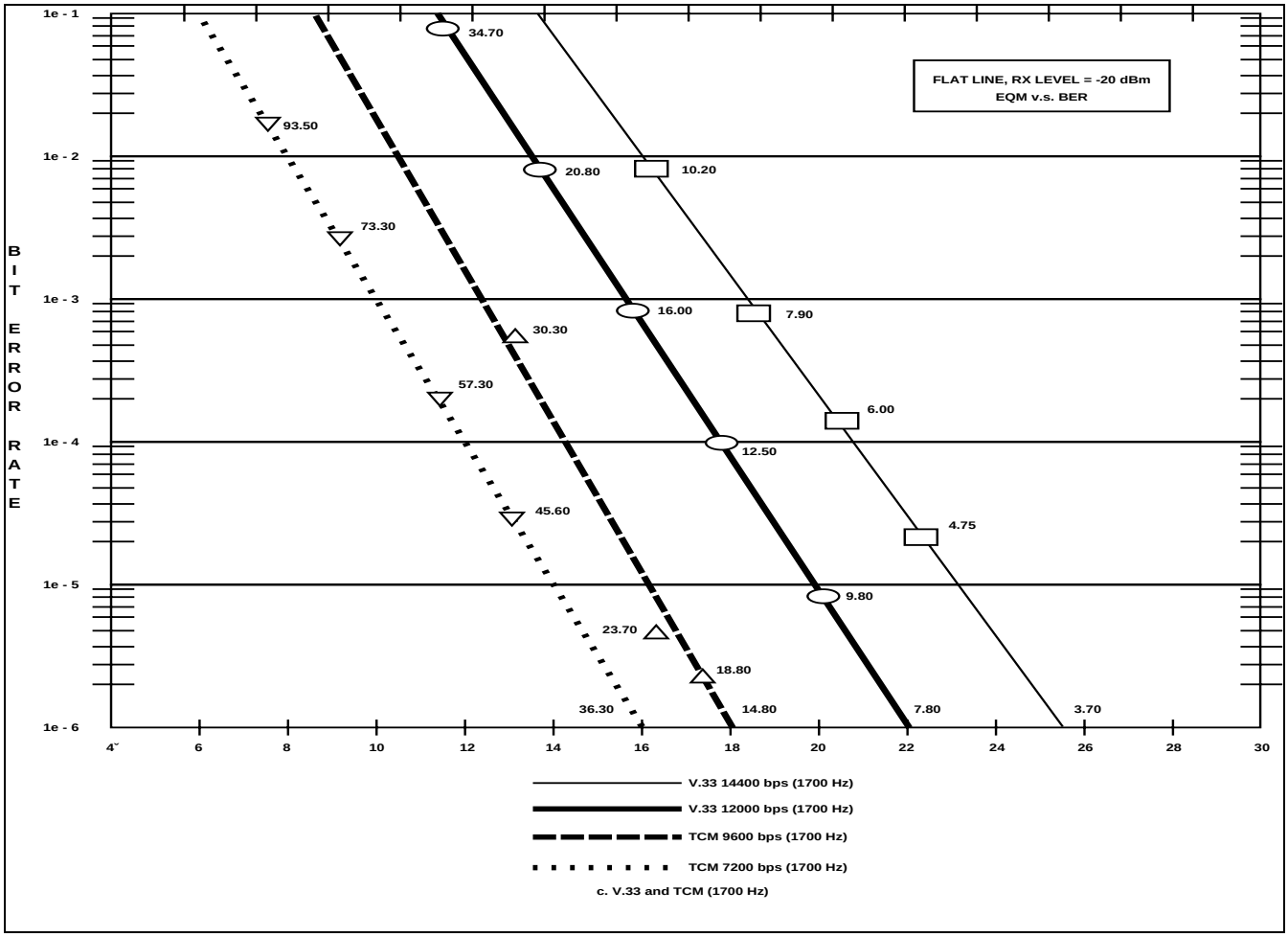

Figure 13-1. Typical Bit Error Rate (BER) Curves (V.33 and TCM (1700 Hz)) (Cont'd)

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14. MODEM INTERFACE CIRCUIT

14.1 CIRCUIT AND COMPONENTS

The modem is supplied in a 128-pin TQFP for design into OEM circuit boards. The Fax/TAM and Fax Speakerphone interface schematics in Figure 14-1 and Figure 14-2 illustrate the connections and components required to connect the modem to OEM electronics.

A typical line interface using an external hybrid is shown in Figure 14-3.

Figure 14-4 shows a typical microphone circuit.

Figure 14-5 shows a typical speaker circuit.

14.1.1 Crystal/Oscillator Specifications

Table 14-1 specifies parameters for crystals or oscillators identified in these schematics.

14.1.2 Transmit Level and Receive Threshold Trimmers

Resistors R5 and R7 (Figure 14-2)can be used to trim the transmit level and receive threshold to the accuracy required by the OEM equipment. For a tolerance of ±1 dBm, the 1% resistor values shown are correct for more than 99.8% of the units.

14.1.3 Echo Canceller Working Condition

Maximum echo return gain from LINEOUT to LINEIN must satisfy condition (1) in Section 12.3 at all passband frequencies.

14.1.4 Room Acoustic Echo Canceller Working Condition

Maximum echo return gain from SPPKRP or SPKRM to MICP and MICM must satisfy condition (2) in Section 12.3 at all passband frequencies.

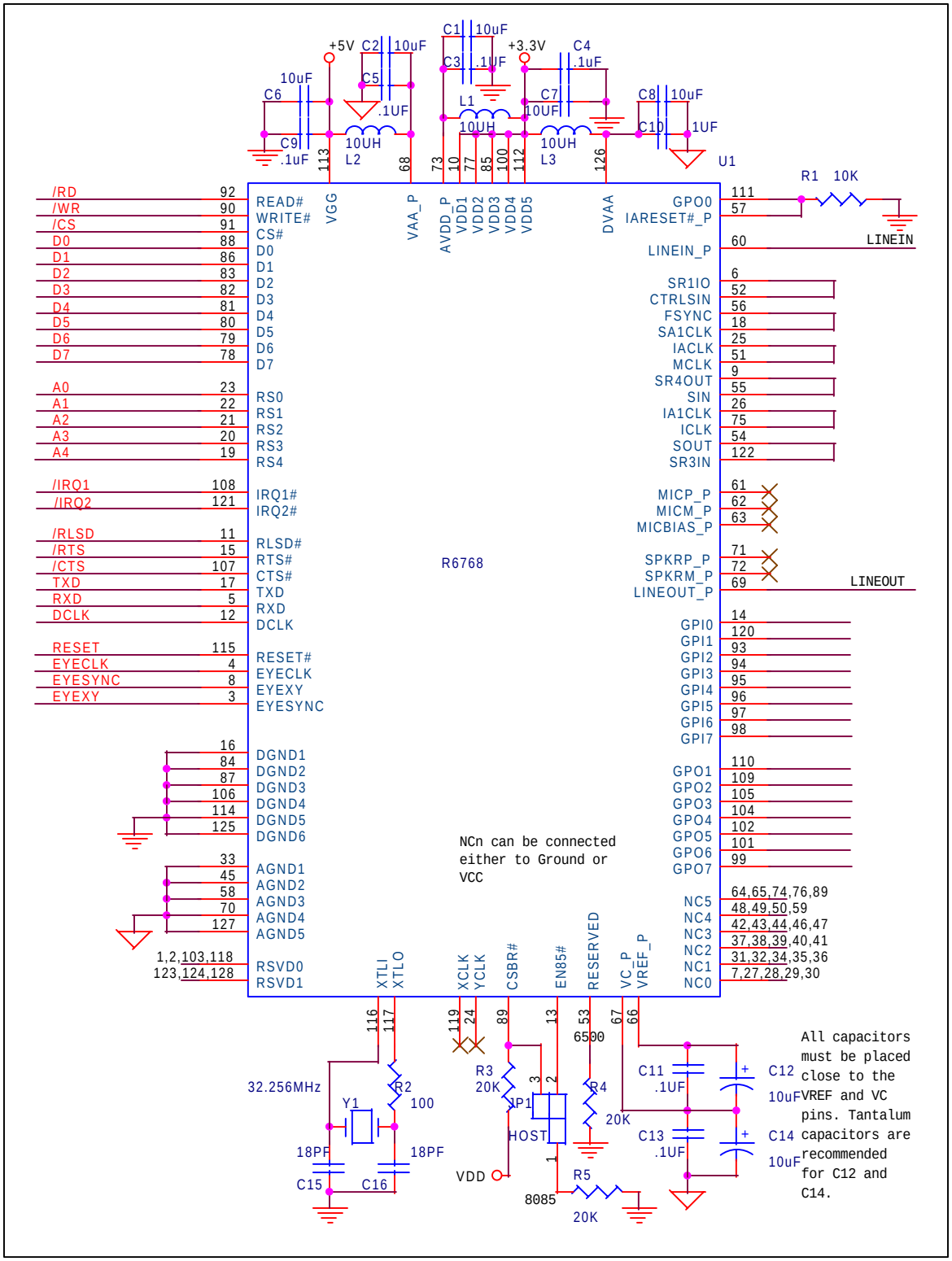


Figure 14-1. Fax/DTAM Interface Circuit

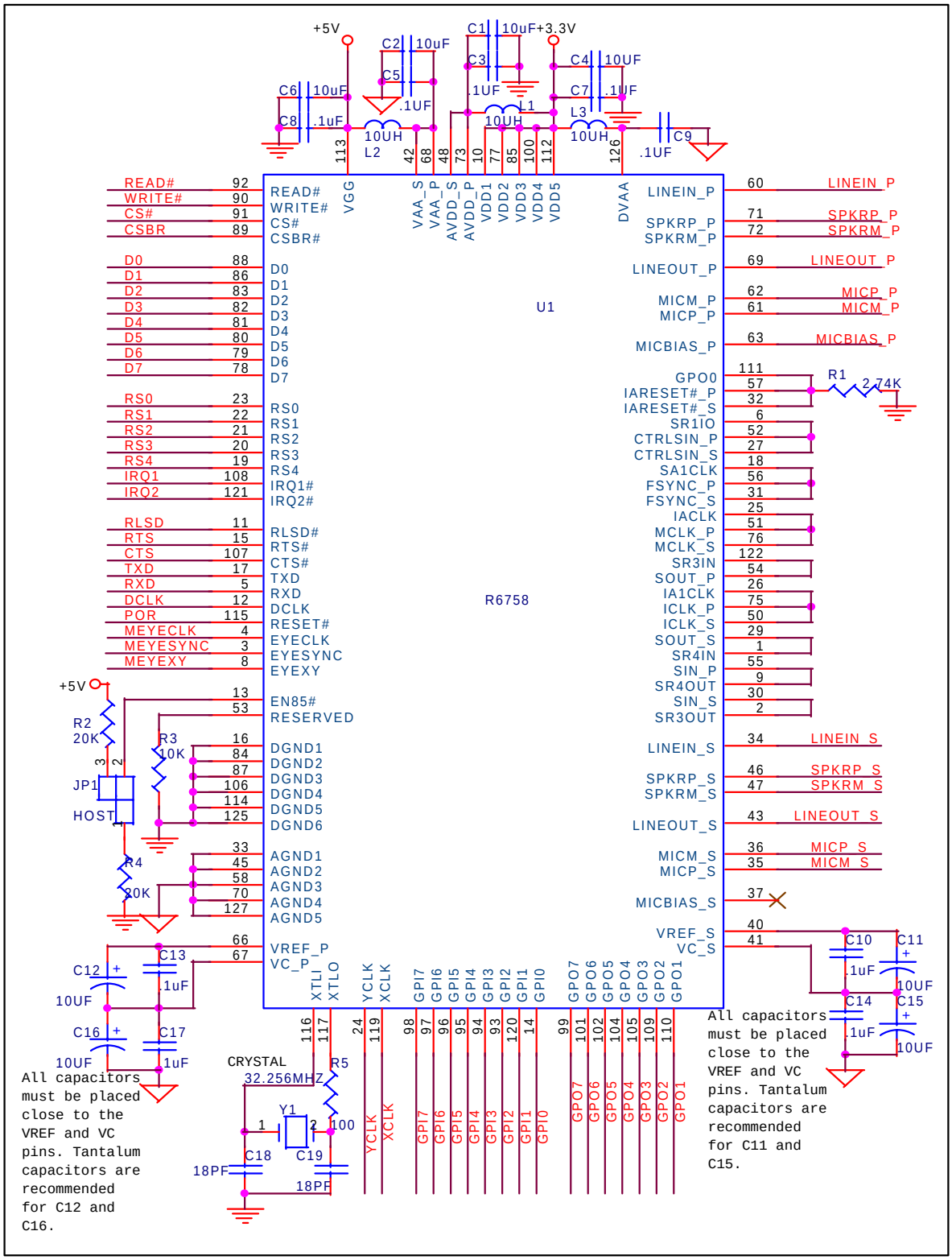


Figure 14-2. Fax Speakerphone Interface Circuit

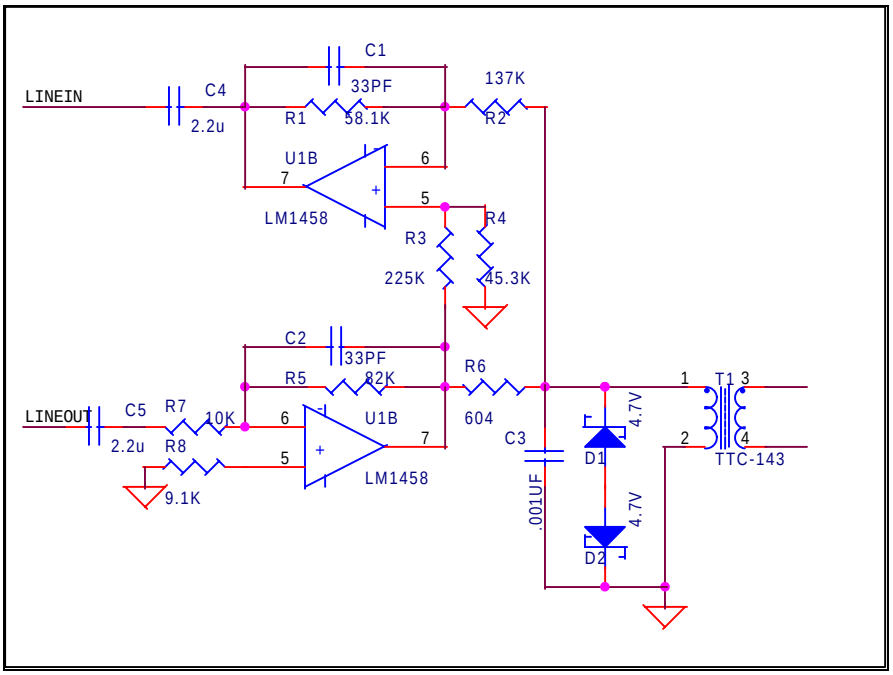


Figure 14-3. Typical Interface to External Hybrid

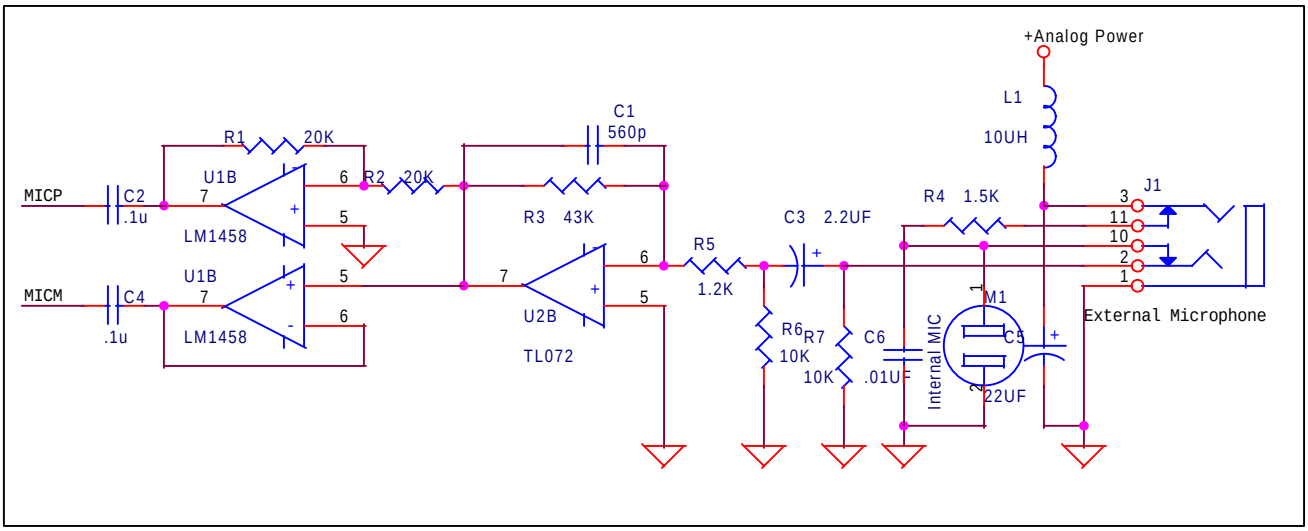


Figure 14-4. Typical Microphone Circuit

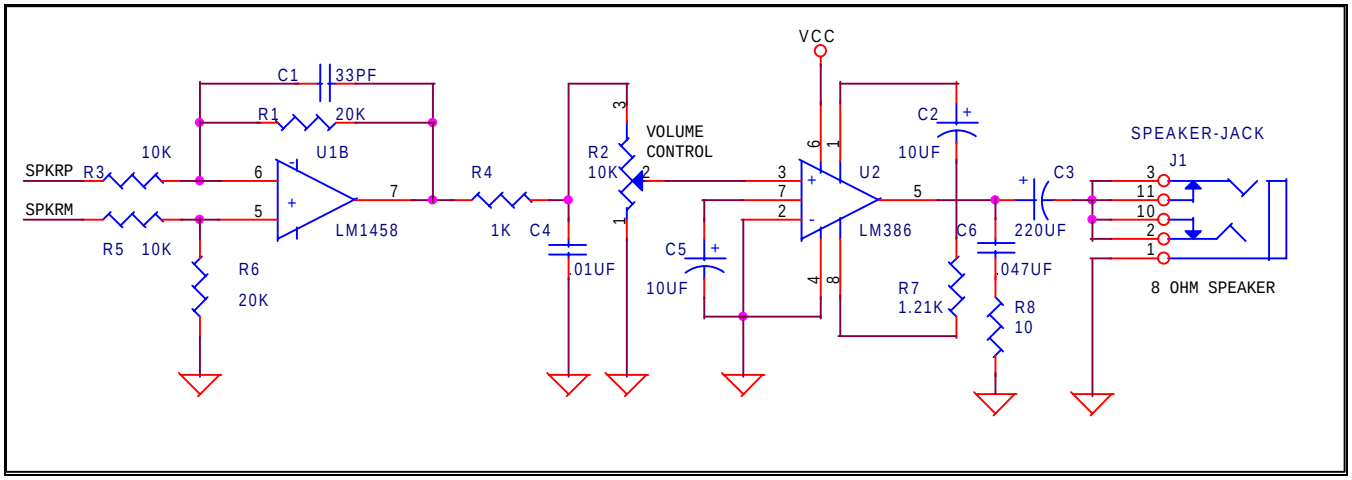


Figure 14-5. Typical Speaker Circuit

Table 14-1. Crystal Specifications - 32.256 Functional Mode

Characteristic	HC49U-32.256-FL	HC49U-32.256-L
Rockwell Part No.		
Electrical		
Frequency	32.256 MHz nominal	32.256 MHz nominal
Frequency Tolerance	±50 ppm (C_L = 18 pF)	±50 ppm (C_L = 18 pF)
Frequency Stability		
vs. Temperature	±35 ppm (-20°C to 70°C)	±35 ppm (-20°C to 70°C)
vs. Aging	±15 ppm/5 years	±15 ppm/5 years
Oscillation Mode	Fundamental	Third Overtone
Calibration Mode	Parallel resonant	Parallel resonant
Load Capacitance, C_L	18 pF nom.	18 pF nom.
Shunt Capacitance, C_O	7 pF max.	7 pF max.
Series Resistance, R_1	35 Ω max. @100 nW drive level	40 Ω max. @100 nW drive level
Drive Level	100 µW correlation; 500 µW max.	100 µW correlation; 1.0 mW max.
Operating Temperature	0°C to 70°C	-20°C to 70°C
Storage Temperature	–40°C to 85°C	–40°C to 85°C
Mechanical		
Holder Type	SMT	Through Hole
Third Lead	Required	Required

Notes:

1. Characteristics @ 25°C unless otherwise noted.
2. Suggested supplier:
   ILSI America
   8804-122ND Ave. NE
   Kirkland, WA 98033
   USA
   (425) 828-4886

14.2 PC BOARD LAYOUT CONSIDERATIONS

Good engineering practices must be adhered to when designing a printed circuit board (PCB) containing a MONOFAX modem. Suppression of noise is essential to the proper operation and performance of the modem and for surrounding equipment.

Several aspects of noise in an OEM board design containing a MONOFAX modem must be considered:

- On-board/off-board generated noise that affects analog signal levels and analog-to-digital (A/D) conversion/digital-to-analog (D/A) conversion (DAC)
- On-board generated noise that can radiate off-board

Both on-board and off-board generated noise coupled on-board can affect interfacing signal levels and quality—especially in low level analog signals. Of particular concern is noise in frequency ranges affecting modem performance.

On-board generated electromagnetic interference (EMI) noise that can be radiated or conducted off-board is a separate, but equally important, concern. This noise can affect the operation of surrounding equipment. Most local governing agencies have stringent certification requirements that must be met to allow use in specific environments.

Proper PC board layout (component placement, signal routing, trace thickness and geometry, etc.), component selection (composition, value, and tolerance), interface connections, and shielding is required for the board design to achieve desired modem performance and to attain EMI certification.

All the aspects of proper engineering practices are beyond the scope of this designer's guide. The designer should consult noise suppression techniques described in technical publications and journals, electronics and electrical engineering text books, and component supplier application notes. Seminars addressing noise suppression techniques are often offered by technical and professional associations as well as component suppliers.

14.2.1 General Board Layout Guidelines

The board design should adhere to the following general guidelines. Most of these guidelines are also applicable to minimizing on-board noise EMI generation (see Section 15). Also refer to Figure 14-1 and Figure 14-2.

1. All power traces should be at least a 0.1 inch width.
2. Place the decoupling capacitors from the VDD pins to DGND near the VDD pins. Place the decoupling capacitors from DVAA, AVDD_P, AVDD_S, VAA_P, and VAA_S pins to AGND near the DVAA, AVDD_P, AVDD_S, VAA_P, and VAA_S pins.
3. All circuitry connected to the XTLI and XTLO pins should be kept short to prevent stray capacitance from affecting the oscillator and to reduce EMI.
4. Keep the XTLO lead extremely short with no bends greater than 45° and containing no vias since the XTLO pin is connected to a fast rise time, high current driver. All components associated with the oscillator function must be close to the modem device.
5. Tie together the AGND1, AGND2, AGND3, AGDN4, and AGND5 pins at the modem package. Tie one pin directly, by a dedicated path, to the common ground point for analog and digital ground.
6. Supply an analog ground plane beneath all analog components. Connect the analog ground plane to the DGNDA and AGND pins.
7. Supply a digital ground plane to cover the remaining allocated area. Connect the digital ground plane to the DGND1, DGND2, DGND3, DGDN4, DGND5, and DGDN6 pins. Connect the crystal-can to digital ground.
8. Orient the128-pin TQFP package relative to the two ground planes so that the corner containing pin 1 is toward the digital ground plane and the corner containing pin 38 is toward the analog ground plane.
9. As a general rule, route digital signals on the component side of the PCB and route all analog signals on the solder side. The sides may be reversed to match a particular OEM requirement.
10. Routing of the modem signals should provide maximum isolation between noise sources and sensitive inputs. When layout requirements necessitate routing these signals together, they should be separated by neutral signals.

14.2.2 Electromagnetic Interference (EMI) Considerations

The following guidelines are offered to minimize EMI generation. In order to minimize contribution of MONOFAX modem-based design to EMI, the designer must understand the major sources of EMI and how to reduce them.

1. Keep the crystal/oscillator and other related external components as close to the device XTLI and XTLO pins as possible.
2. Keep any traces carrying high frequency signals as short as possible.
3. Have a good ground plane. In some cases a multilayer board may be required with full layers for ground and power distribution.
4. Decouple power to ground with decoupling capacitors as close to the device pins as possible.
5. Eliminate ground loops, which are unexpected current return paths to the power source.
6. Decouple the phone line cables at the telephone line jacks using series inductors or ferrite beads.
7. Decouple the power cord at the power cord interface with decoupling capacitors.
8. Locate high frequency circuits in a separate area to minimize capacitive coupling to other circuits.
9. Locate cables and connectors to avoid coupling from high frequency circuits.
10. Layout the highest frequency signal traces next to the ground grid.
11. If a multilayer board design is used, the following design rules are recommended:
    a) Make no cuts in the ground or power planes.
    b) The ground plane must cover all traces.

14.2.3 Crystal Oscillator EMI Considerations

A source of EMI radiation in a MONOFAX modem design can be the crystal oscillator circuit which produces fundamental energy at 32.256 MHz and third harmonic energy at 96.77 MHz.

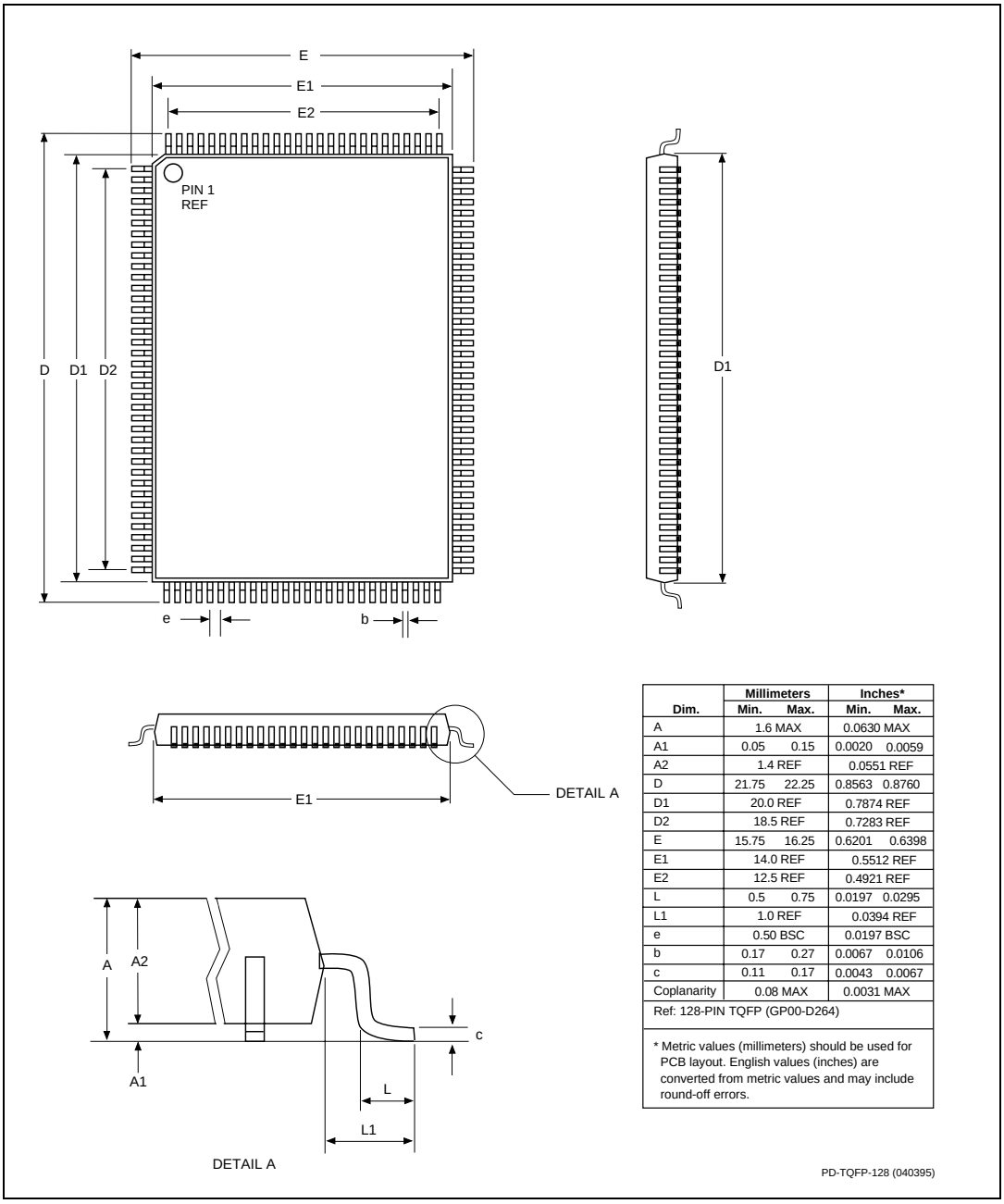
The third harmonic energy can be reduced by adding series resistance between the XTLO pin and the load capacitor as illustrated in Figure 14-1 and Figure 14-2. The resistor and the XTLO capacitor create a low pass filter which can attenuate the third harmonic component energy. Although a larger resistor value will further reduce the third harmonic component, it will attenuate the fundamental frequency and may cause an oscillator circuit start-up problem. A careful selection of this resistor is important.

Table 14-2. FM209/214 Modem Pin Noise Characteristics

Interface Signal Definition	Noise Source	Neutral	Noise Sensitive
Overhead	115, 116, 117	10, 16, 33, 42, 45, 48, 58, 68, 70, 73, 77, 84, 85, 87, 100, 106, 112, 113, 114, 125, 126, 127	
Microprocessor Bus	19-23, 78-83, 86, 88-92, 108, 121		
V.24 Serial	5, 11, 12, 15, 17, 107		
Auxiliary	13, 24, 119		
Telephone and Audio			34-37, 43, 46, 47, 60-63, 69, 71, 72
General Purpose Input and Output		14, 93-99, 101, 102, 104, 105, 109-111, 120	
Eye Diagnostic	3, 4, 8		
Modem Interconnect	1, 2, 6, 9, 18, 25-27, 29-32, 50-52, 54-57, 75, 76, 111, 122		40, 41, 66, 67
NC and Reserved		7, 28, 38, 39, 44, 49, 59, 64, 65, 74, 103, 118, 123, 124, 128	

15. PACKAGE DIMENSIONS

Package dimensions are shown in Figure 15-1 (128-pin TQFP).



Dim.	Millimeters Min.	Millimeters Max.	Inches* Min.	Inches* Max.
A		1.6 MAX		0.0630 MAX
A1	0.05	0.15	0.0020	0.0059
A2		1.4 REF		0.0551 REF
D	21.75	22.25	0.8563	0.8760
D1		20.0 REF		0.7874 REF
D2		18.5 REF		0.7283 REF
E	15.75	16.25	0.6201	0.6398
E1		14.0 REF		0.5512 REF
E2		12.5 REF		0.4921 REF
L	0.5	0.75	0.0197	0.0295
L1		1.0 REF		0.0394 REF
e		0.50 BSC		0.0197 BSC
b	0.17	0.27	0.0067	0.0106
c	0.11	0.17	0.0043	0.0067
Coplanarity		0.08 MAX		0.0031 MAX

Ref: 128-PIN TQFP (GP00-D264)

* Metric values (millimeters) should be used for PCB layout. English values (inches) are converted from metric values and may include round-off errors.

Figure 15-1. 128-Pin TQFP Dimensions

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