
HM62W16255HI Series

4M High Speed SRAM (256-kword × 16-bit)

HITACHI

ADE-203-1038A (Z)

Rev. 1.0

Apr. 15, 1999

Description

The HM62W16255HI is a 4-Mbit high speed static RAM organized 256-kword × 16-bit. It has realized high speed access time by employing CMOS process (4-transistor + 2-poly resistor memory cell) and high speed circuit designing technology. It is most appropriate for the application which requires high speed, high density memory and wide bit width configuration, such as cache and buffer memory in system. It is packaged in 400-mil 44-pin SOJ and 400-mil 44-pin plastic TSOPII.

Features

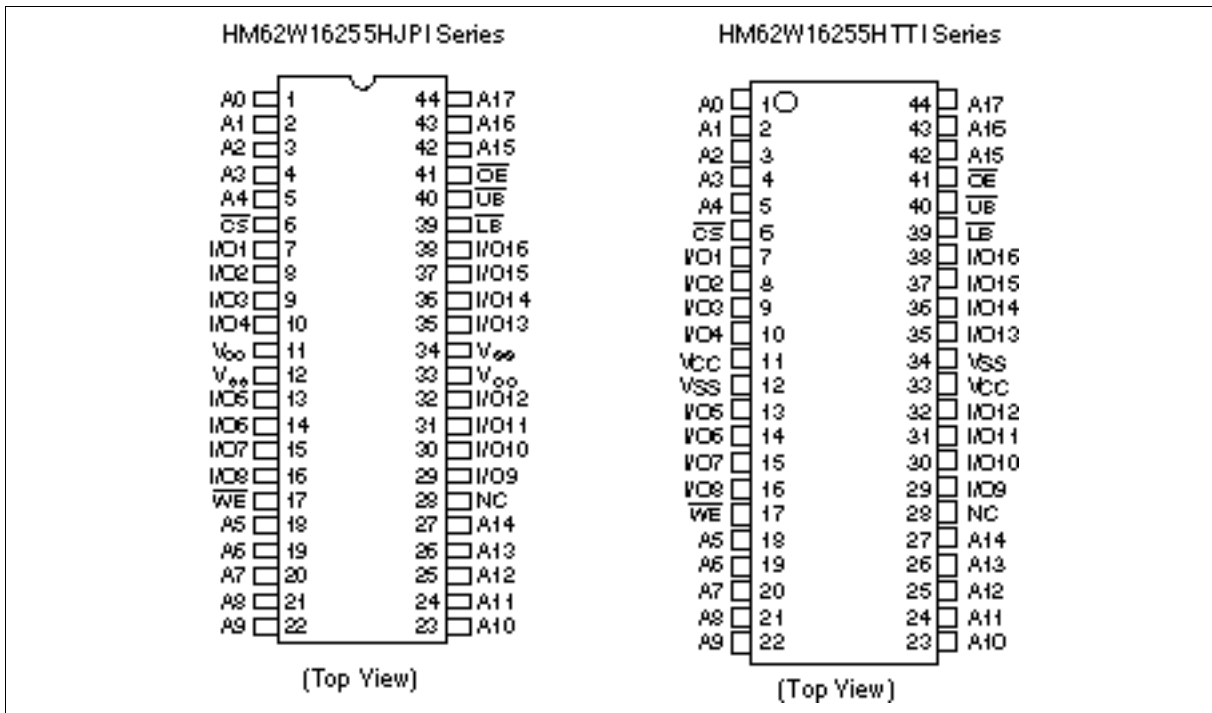
- Single 3.3 V supply: 3.3 V ± 0.3V
- Access time: 15 ns (max)
- Completely static memory
 - No clock or timing strobe required
- Equal access and cycle times
- Directly TTL compatible
 - All inputs and outputs
- Operating current: 160 mA (max)
- TTL standby current: 50 mA (max)
- CMOS standby current: 5 mA (max)
- Center V_{CC} and V_{SS} type pinout
- Temperature range: -40 to 85°C

HM62W16255HI Series

Ordering Information

Type No.	Access time	Package
HM62W16255HJPI-15	15 ns	400-mil 44-pin plastic SOJ (CP-44D)
HM62W16255HTTI-15	15 ns	400-mil 44-pin plastic SOJ (TTP-44DE)

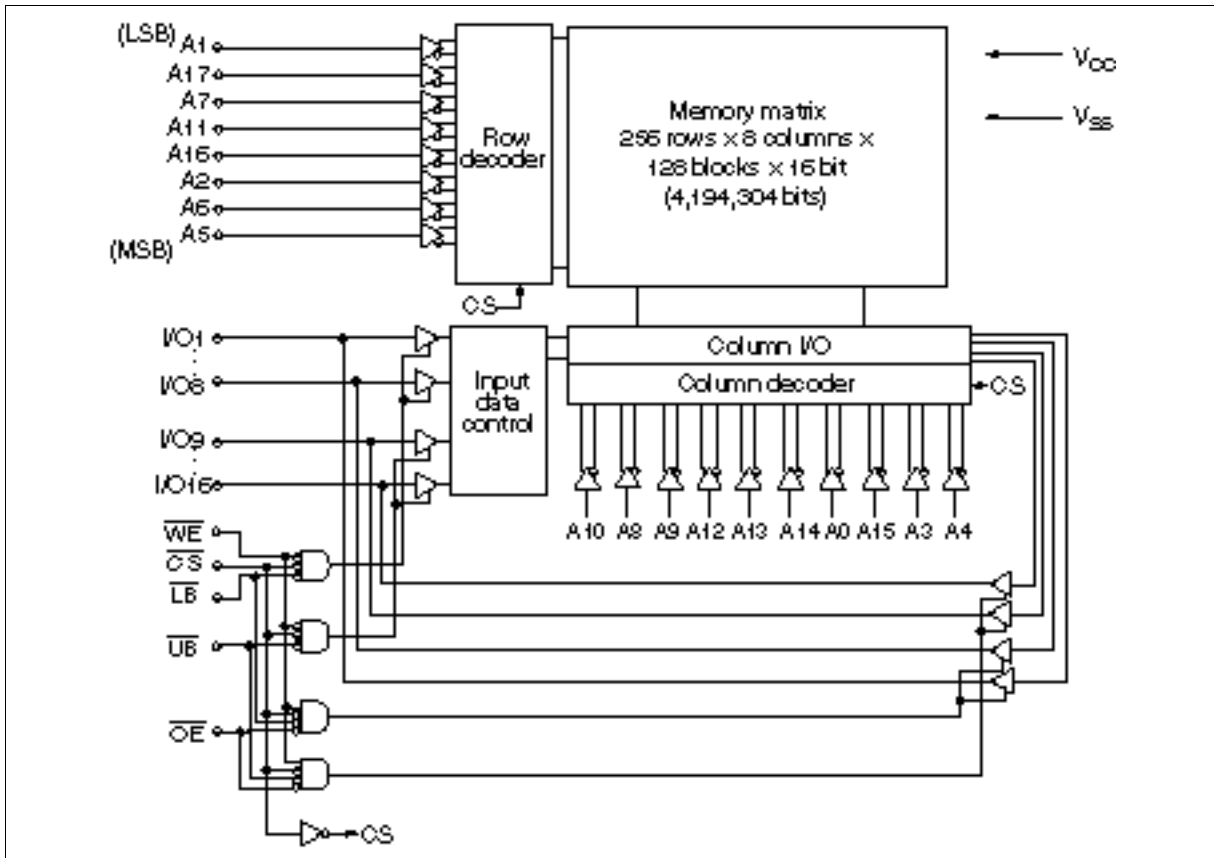
Pin Arrangement



Pin Description

Pin name	Function
A0 to A17	Address input
I/O1 to I/O16	Data input/output
CS	Chip select
OE	Output enable
WE	Write enable
UB	Upper byte select
LB	Lower byte select
V _{CC}	Power supply
V _{SS}	Ground
NC	No connection

Block Diagram



HM62W16255HI Series

Operation Table

CS	OE	WE	LB	UB	Mode	V _{CC} current	I/O1–I/O8	I/O9–I/O16	Ref. cycle
H	×	×	×	×	Standby	I _{SB} , I _{SB1}	High-Z	High-Z	—
L	H	H	×	×	Output disable	I _{CC}	High-Z	High-Z	—
L	L	H	L	L	Read	I _{CC}	Output	Output	Read cycle
L	L	H	L	H	Lower byte read	I _{CC}	Output	High-Z	Read cycle
L	L	H	H	L	Upper byte read	I _{CC}	High-Z	Output	Read cycle
L	L	H	H	H	—	I _{CC}	High-Z	High-Z	—
L	×	L	L	L	Write	I _{CC}	Input	Input	Write cycle
L	×	L	L	H	Lower byte write	I _{CC}	Input	High-Z	Write cycle
L	×	L	H	L	Upper byte write	I _{CC}	High-Z	Input	Write cycle
L	×	L	H	H	—	I _{CC}	High-Z	High-Z	—

Note: ×: H or L

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply voltage relative to V _{SS}	V _{CC}	–0.5 to +4.6	V
Voltage on any pin relative to V _{SS}	V _T	–0.5* ¹ to V _{CC} + 0.5* ²	V
Power dissipation	P _T	1.0	W
Operating temperature	T _{opr}	–40 to +85	°C
Storage temperature	T _{stg}	–55 to +125	°C
Storage temperature under bias	T _{bias}	–40 to +85	°C

Notes: 1. V_T (min) = –2.0 V for pulse width (under shoot) 8 ns

2. V_T (max) = V_{CC} + 2.0 V for pulse width (over shoot) 8 ns

HM62W16255HI Series

Recommended DC Operating Conditions (Ta = -40 to +85°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}^{*3}	3.0	3.3	3.6	V
	V_{SS}^{*4}	0	0	0	V
Input voltage	V_{IH}	2.2	—	$V_{CC} + 0.5^{*2}$	V
	V_{IL}	-0.5^{*1}	—	0.8	V

- Notes: 1. V_{IL} (min) = -2.0 V for pulse width (under shoot) 8 ns
 2. V_{IH} (max) = $V_{CC} + 2.0$ V for pulse width (over shoot) 8 ns
 3. The supply voltage with all V_{CC} pins must be on the same level.
 4. The supply voltage with all V_{SS} pins must be on the same level.

DC Characteristics (Ta = -40 to +85°C, $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$, $V_{SS} = 0 \text{ V}$)

Parameter	Symbol	Min	Typ ^{*1}	Max	Unit	Test conditions
Input leakage current	$ I_{LI} $	—	—	2	μA	$V_{in} = V_{SS} \text{ to } V_{CC}$
Output leakage current ^{*1}	$ I_{LO} $	—	—	2	μA	$V_{in} = V_{SS} \text{ to } V_{CC}$
Operating power supply current	15 ns cycle I_{CC}	—	—	160	mA	Min cycle CS = V_{IL} , $I_{out} = 0 \text{ mA}$ Other inputs = V_{IH}/V_{IL}
Standby power supply current	15 ns cycle I_{SB}	—	—	50	mA	Min cycle, CS = V_{IH} , Other inputs = V_{IH}/V_{IL}
	I_{SB1}	—	0.05	5	mA	f = 0 MHz V_{CC} CS $V_{CC} - 0.2 \text{ V}$, (1) 0 V V_{in} 0.2 V or (2) V_{CC} V_{in} $V_{CC} - 0.2 \text{ V}$ V
Output voltage	V_{OL}	—	—	0.4	V	$I_{OL} = 8 \text{ mA}$
	V_{OH}	2.4	—	—	V	$I_{OH} = -4 \text{ mA}$

Note: 1. Typical values are at $V_{CC} = 3.3 \text{ V}$, $T_a = +25^\circ\text{C}$ and not guaranteed.

Capacitance (Ta = +25°C, f = 1.0 MHz)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input capacitance ^{*1}	C_{in}	—	—	6	pF	$V_{in} = 0 \text{ V}$
Input/output capacitance ^{*1}	$C_{I/O}$	—	—	8	pF	$V_{I/O} = 0 \text{ V}$

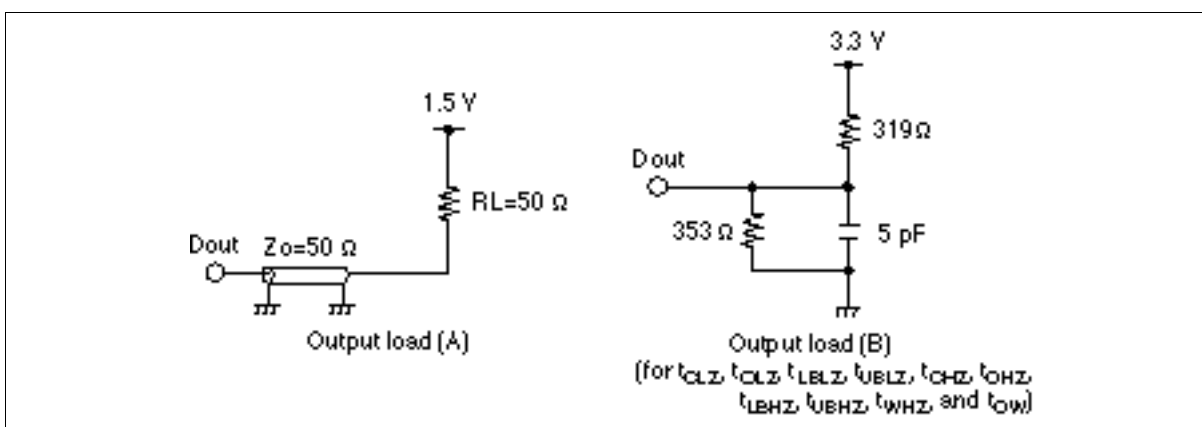
Note: 1. This parameter is sampled and not 100% tested.

HM62W16255HI Series

AC Characteristics ($T_a = -40$ to $+85^\circ\text{C}$, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$, unless otherwise noted.)

Test Conditions

- Input pulse levels: 3.0 V/0.0 V
- Input rise and fall time: 3 ns
- Input and output timing reference levels: 1.5 V
- Output load: See figures (Including scope and jig)



Read Cycle

Parameter	Symbol	HM62W16255HI		Unit	Notes
		Min	Max		
Read cycle time	t_{RC}	15	—	ns	
Address access time	t_{AA}	—	15	ns	
Chip select access time	t_{ACS}	—	15	ns	
Output enable to output valid	t_{OE}	—	7	ns	
Byte select to output valid	t_{LB}, t_{UB}	—	7	ns	
Output hold from address change	t_{OH}	3	—	ns	
Chip select to output in low-Z	t_{CLZ}	3	—	ns	1
Output enable to output in low-Z	t_{OLZ}	0	—	ns	1
Byte select to output in low-Z	t_{LBLEZ}, t_{UBLZ}	0	—	ns	1
Chip deselect to output in high-Z	t_{CHZ}	—	7	ns	1
Output disable to output in high-Z	t_{OHZ}	—	7	ns	1
Byte deselect to output in high-Z	t_{LBHZ}, t_{UBHZ}	—	7	ns	1

HM62W16255HI Series

Write Cycle

Parameter	Symbol	HM62W16255HI		Unit	Notes
		Min	Max		
Write cycle time	t_{WC}	15	—	ns	
Address valid to end of write	t_{AW}	10	—	ns	
Chip select to end of write	t_{CW}	10	—	ns	8
Write pulse width	t_{WP}	10	—	ns	7
Byte select to end of write	t_{LBW}, t_{UBW}	10	—	ns	9, 10
Address setup time	t_{AS}	0	—	ns	5
Write recovery time	t_{WR}	0	—	ns	6
Data to write time overlap	t_{DW}	7	—	ns	
Data hold from write time	t_{DH}	0	—	ns	
Write disable to output in low-Z	t_{OW}	3	—	ns	1
Output disable to output in high-Z	t_{OHZ}	—	7	ns	1
Write enable to output in high-Z	t_{WHZ}	—	7	ns	1

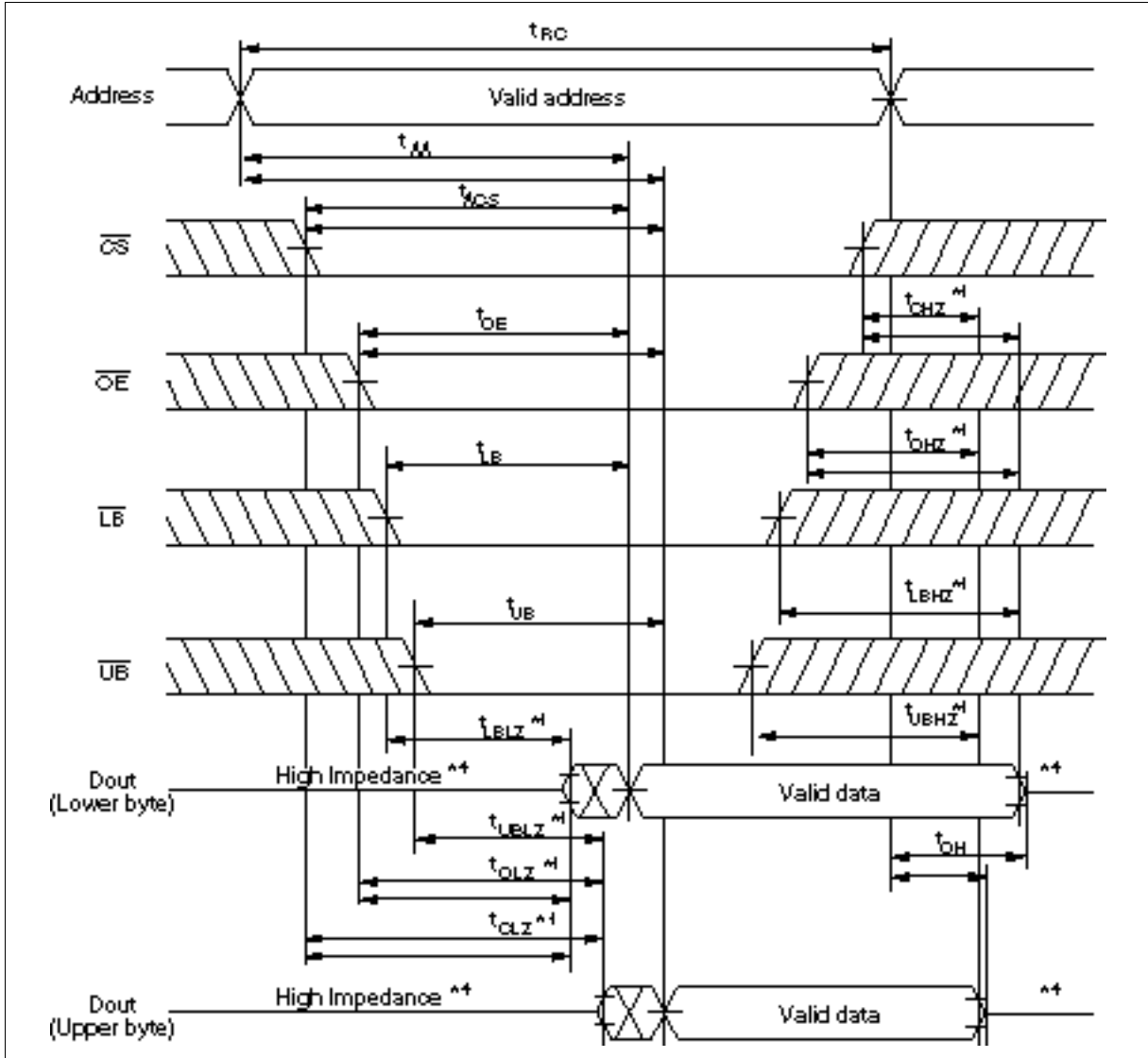
Notes: 1. Transition is measured ± 200 mV from steady voltage with Load (B). This parameter is sampled and not 100% tested.

2. If the CS or LB or UB low transition occurs simultaneously with the WE low transition or after the WE transition, output remains a high impedance state.
3. WE and/or CS must be high during address transition time.
4. If CS, OE, LB and UB are low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
5. t_{AS} is measured from the latest address transition to the latest of CS, WE, LB or UB going low.
6. t_{WR} is measured from the earliest of CS, WE, LB or UB going high to the first address transition.
7. A write occurs during the overlap of low CS, low WE and low LB or low UB.
8. t_{CW} is measured from the later of CS going low to the end of write.
9. t_{LBW} is measured from the later of LB going low to the end of write.
10. t_{UBW} is measured from the later of UB going low to the end of write.

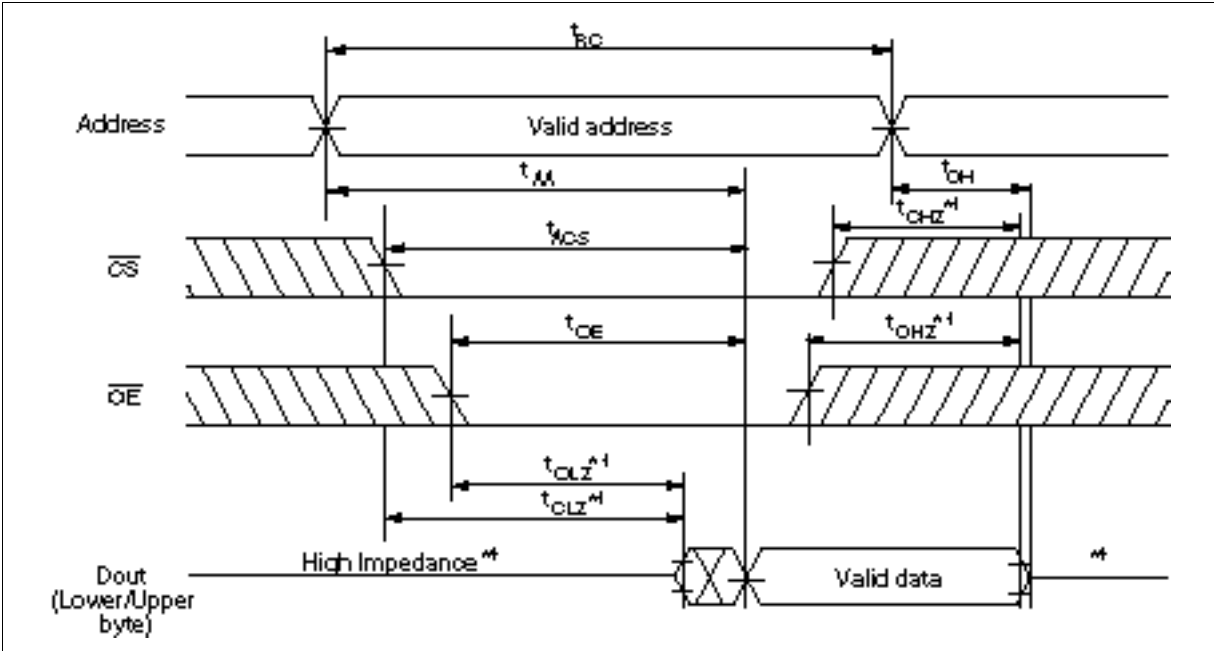
HM62W16255HI Series

Timing Waveforms

Read Timing Waveform (1) ($WE = V_{IH}$)

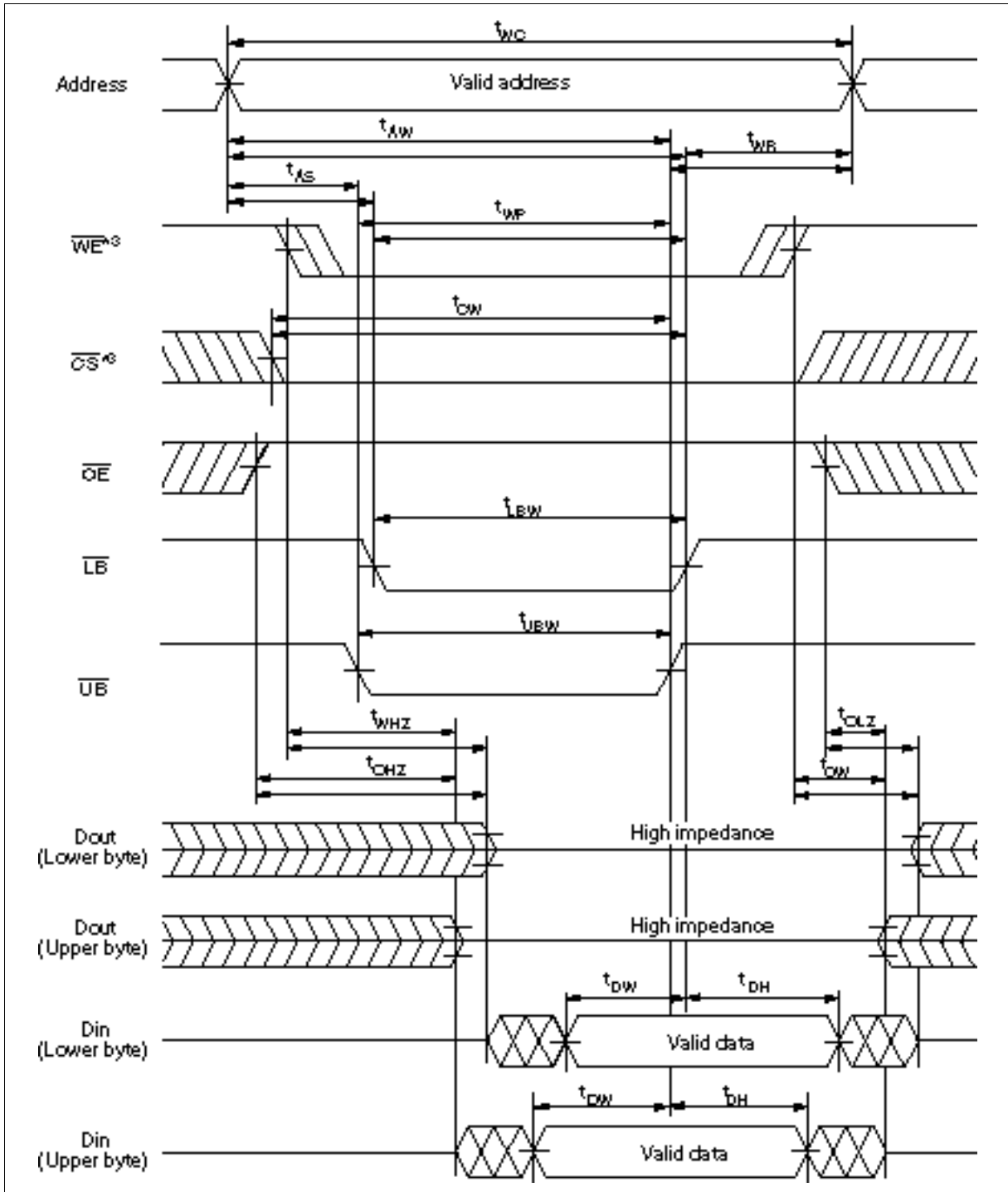


Read Timing Waveform (2) (WE = V_{IH}, LB = V_{IL}, UB, = V_{IL})

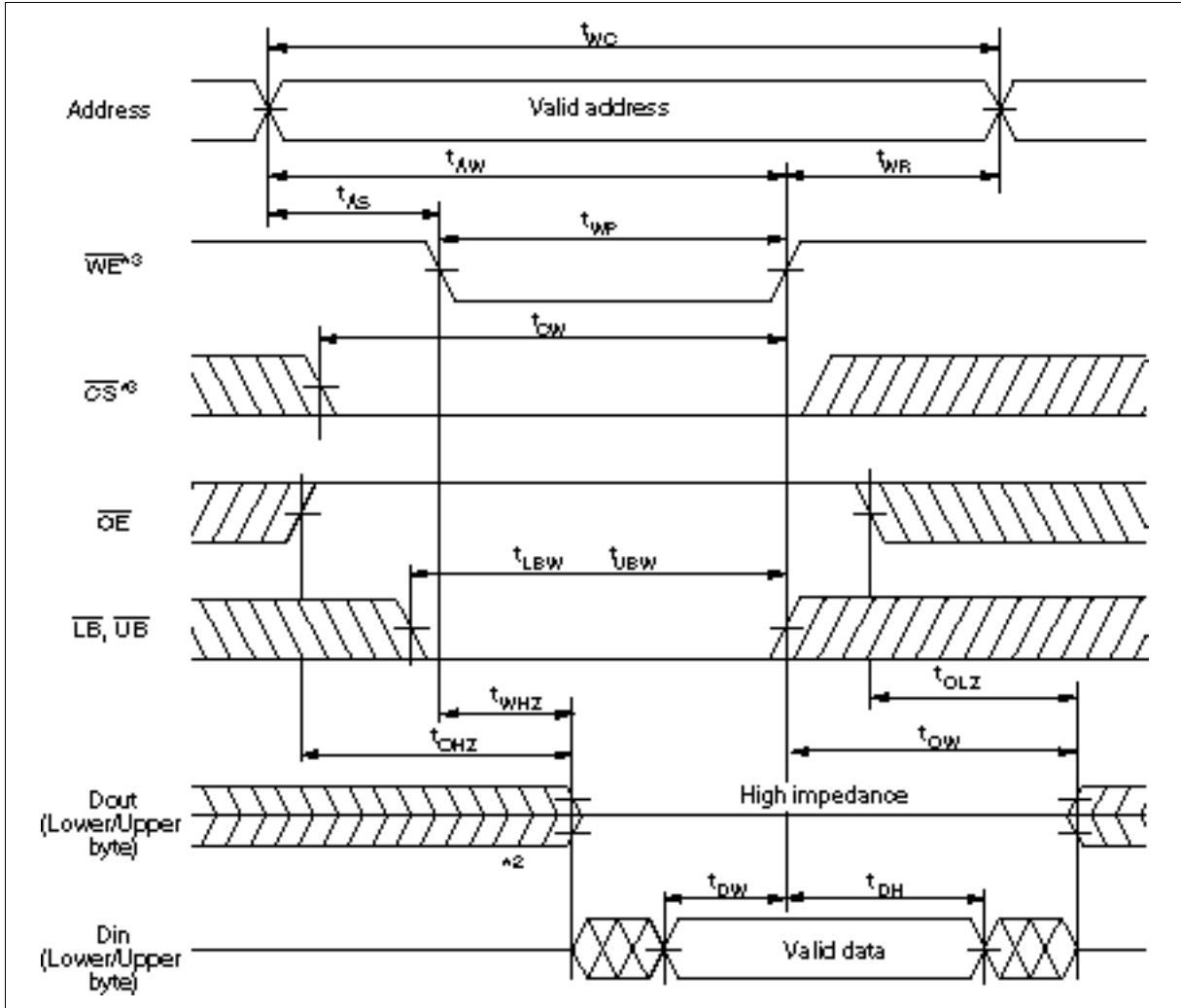


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Write Timing Waveform (1) (LB, UB Controlled)

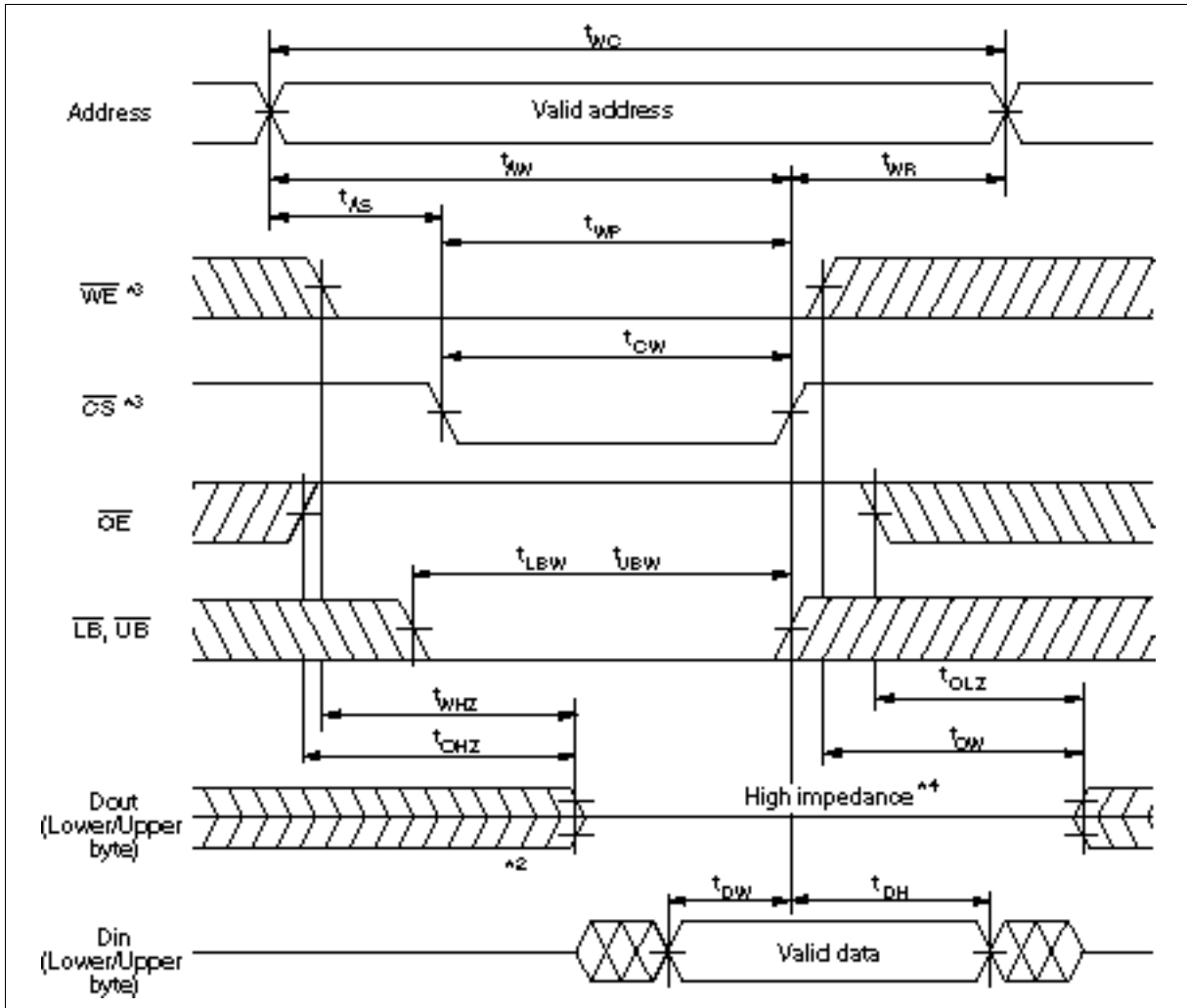


Write Timing Waveform (2) (WE Controlled)



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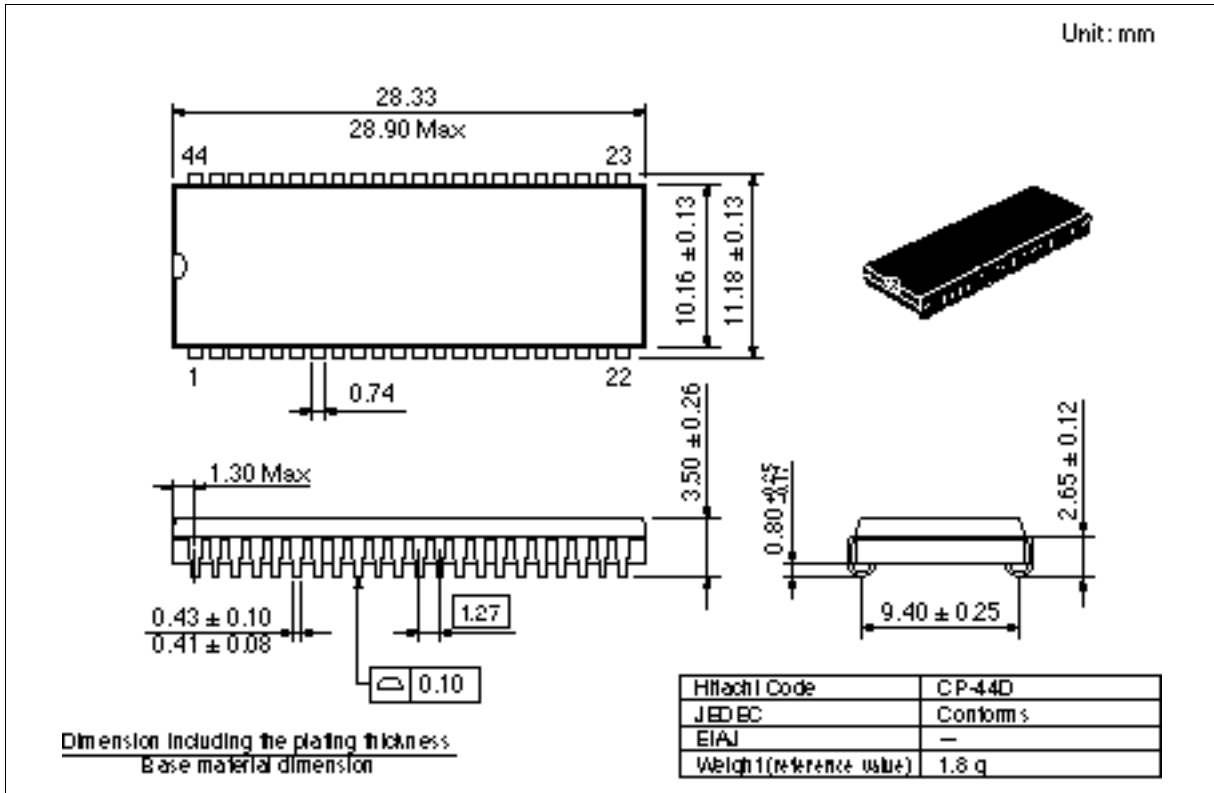
Write Timing Waveform (3) (CS Controlled)



HM62W16255HI Series

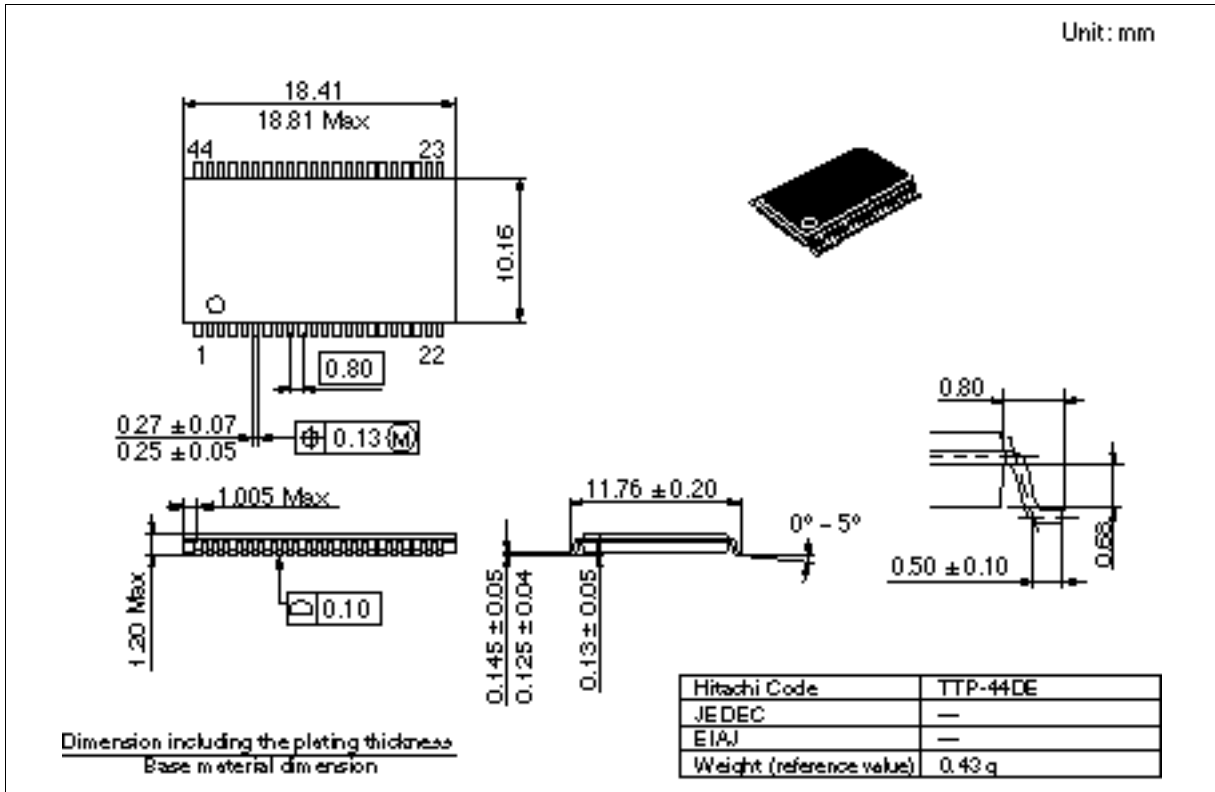
Package Dimensions

HM62W16255HJPI Series (CP-44D)



HM62W16255HI Series

HM62W16255HTTI Series (TTP-44DE)



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HM62W16255HI Series

Revision Record

Rev.	Date	Contents of Modification	Drawn by	Approved by
1.0	Apr. 15, 1999	Initial issue		
