Application of the CA1524 Series Pulse-Width Modulator ICs

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CA2524 IS AN OBSOLETE PRODUCT

This application note reviews pulse-width modulated (PWM) circuits, and the CA1524 series of pulse-width modulator ICs particularly intended for this type of application. It also includes descriptions of basic switching-regulator circuits, the generic CA1524 Series IC, its use in a variable switched power supply application, together with a variety of its unique circuit applications.

The CA1524, ~~CA2524~~, and CA3524 Series, a family of integrated circuits containing a pulse-width modulator and related control circuits, are particularly applicable to switching regulators, flyback converters, dc-to-dc converters and the like. These ICs operate with a power supply in the 8V to 40V range for use in both low and high power regulators. The CA1524 series ICs contain the following circuit functions: 5V temperature compensated zener reference, precision RC oscillator, transconductance error amplifier, current-limiting amplifier, control comparator, shutdown circuit, and dual output transistor switches. The circuit's functions make these devices attractive for a wide variety of other applications; e.g., low frequency pulse generators, automotive temperature voltage regulators, battery chargers, electronic bathroom scales, etc.

The CA1524 family of ICs is supplied in 16 lead plastic and ceramic (frit) packages, and is also available in chip form. Data on these types are found in the datasheet file number 1239.

CA1524 Series IC Features

The CA1524 PWM on-chip functions shown in the functional block diagram of Figure 1 include an error amplifier, a comparator, an oscillator, a flip-flop, and a voltage regulator. The error amplifier senses the difference between the actual and the desired regulator output and applies this signal to the comparator's positive input. The output of this stage is in turn a function of the error signal and the oscillator's ramp voltage.

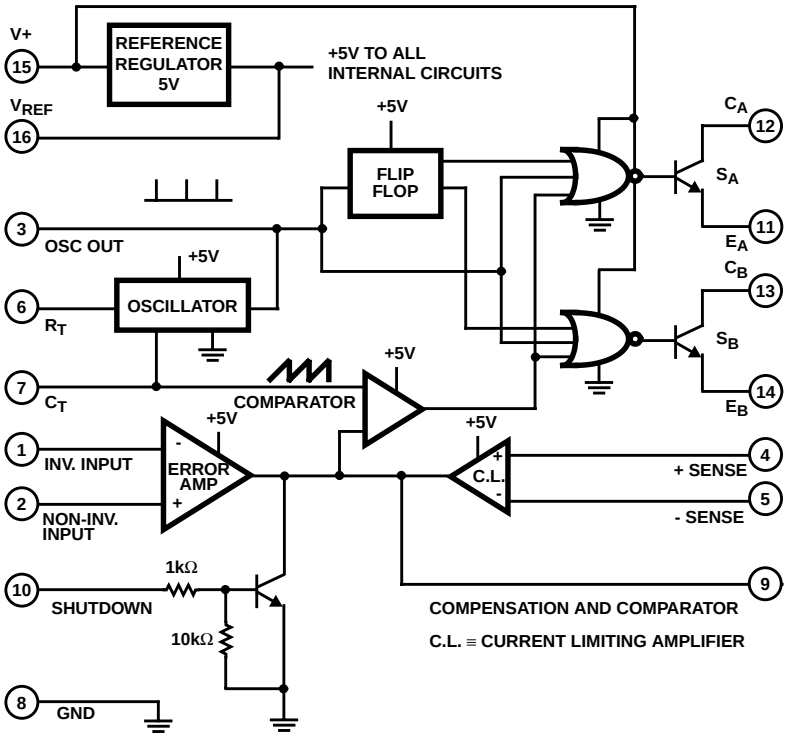


FIGURE 1A. FUNCTIONAL BLOCK DIAGRAM

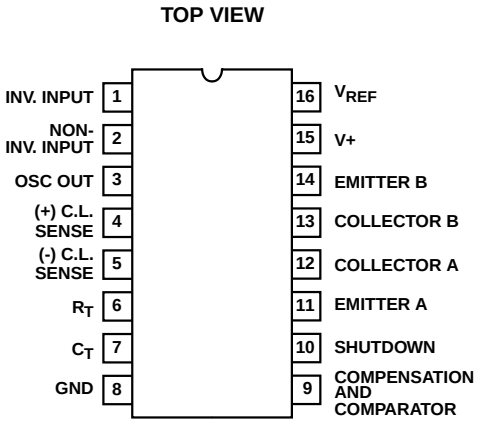


FIGURE 1B. TERMINAL CONNECTION DIAGRAM

FIGURE 1. CA1524 SERIES ICs

The oscillator's output pulses alternately trigger the flip-flop, whose output ultimately provides the circuits push-pull drive signal via the NOR-gates and the output transistors. The other NOR-gate inputs control the duration of the output pulses. Depending upon the oscillator's output level (high or low) and the comparator's high or low status, the "on" duty-cycle of the NOR gate can vary from 0 to 45 percent. It should be noted, that the NOR gates are on alternately. Thus, by connecting the output transistors in parallel, an effective on time of 0% to 90% and a wide voltage regulation range can be attained.

Comparative Operating Efficiencies in Series-Pass and PWM Types of Voltage Regulators

The series-pass circuit is a classical means of implementing the voltage regulator function; its simple and easy to design, but comparatively inefficient when required to operate over a range of supply voltages and output currents. The need to improve operational efficiency, in recent years, has been one of the major factors motivating engineers to use the PWM type of voltage regulator despite its greater circuit complexity.

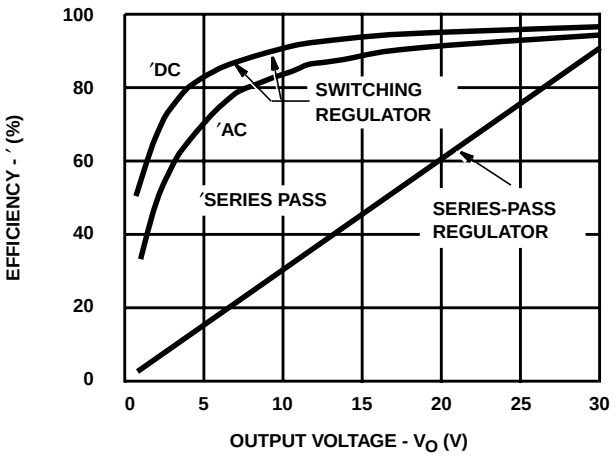
Figure 2 shows the high operating efficiency of the PWM type of voltage regulator design e.g., using CA1524 and compares it with that of a conventional linear series-pass circuit. In a series-pass type of regulated power supply, the pass transistor is biased in the linear region, to permit good line and load regulation and dynamic response, but at a sacrifice in efficiency. This loss in efficiency occurs as a result of the power dissipated in the pass transistor, i.e., the product of the voltage drop and the current flowing through it. In a series-pass regulator, the output current is about equal to the input current, therefore, the overall efficiency ≅ the ratio V_O/V_{IN}.

It is, therefore, apparent that the input/output voltage differential must be kept at a minimum if high efficiency is to be achieved. Dissipation in the pass device is $(V_{IN} - V_{DD})$ I_{PASS}, $(V_{IN} - V_O)$ is typically 2V to 3V. There are additional small operating losses in the IC itself. By way of contrast, the pass transistor for a switching-regulator control circuit is driven between two states, "on" and "off", and since the linear region is not used, loss is essentially limited to the product of the saturation voltage and the current flowing through the pass transistor during its on state. There is a small additional loss that occurs during the on/off transitions.

Additional losses in the switching regulator include diode-voltage losses, inductor-transformer core losses, and copper losses. The overall efficiency is essentially independent of input voltage or input current. A worst case theoretical value of the AC switching and DC transistor losses approaches a value equal to $V_O/(V_O + 2V)$ (assuming a diode V_{BE} and transistor V_{CE}(s) of 1V each). Therefore, a minimum input voltage of V_O + 2V is needed to operate a switching regulator.

Circuit Description

The CA1524, CA2524, and CA3524 monolithic integrated circuits are designed to provide all of the control circuitry necessary for a broad range of switching regulator applications. On-chip functional blocks, shown in Figure 1, include a zener voltage reference, transconductance error amplifier, precision RC oscillator, pulse width modulator, pulse steering flip-flop, dual alternating output switches, and current limiting and shutdown circuitry. A complete schematic is shown in Figure 4



Pulse Width Modulator (PWM) Switching Regulator

Linear Series-Pass Regulator

$$\eta_{DC} = \frac{P_O}{P_{IN}} = \frac{V_O I_O}{V_O I_O + I_O 1} = \frac{V_O}{V_O + 1} \qquad \eta = \frac{P_O}{P_{IN}}$$

$$\eta_{AC} = \frac{P_O}{P_{IN}} = \frac{V_O I_O}{V_O I_O + I_O 2} = \frac{V_O}{V_O + 2} \qquad \eta = \frac{V_O I_O}{V_{IN} I_{IN}} \cong \frac{V_O}{V_I N}$$

FIGURE 2. EFFICIENCY CURVES FOR LINEAR (SERIES-PASS) REGULATOR AND PULSE-WIDTH MODULATED SWITCHING REGULATOR (PWM)

Voltage Reference Section

The CA1524 Series devices contain an internal series voltage regulator employing a zener reference to provide a nominal 5 volts output, which is used to bias all internal timing and control circuitry. The output of this regulator is available at terminal 16 and is capable of supplying up to 50mA output current. For higher currents, the circuit of Figure 3 may be used with an external p-n-p transistor and bias resistor. The internal regulator may be bypassed for operation from a fixed 5V supply by connecting both terminal 15 and 16 to the input voltage, which must not exceed 6V.

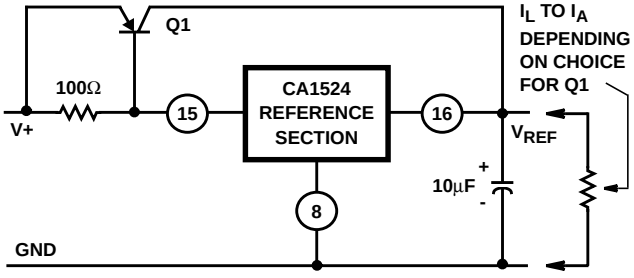


FIGURE 3. CIRCUIT FOR EXPANDING THE REFERENCE

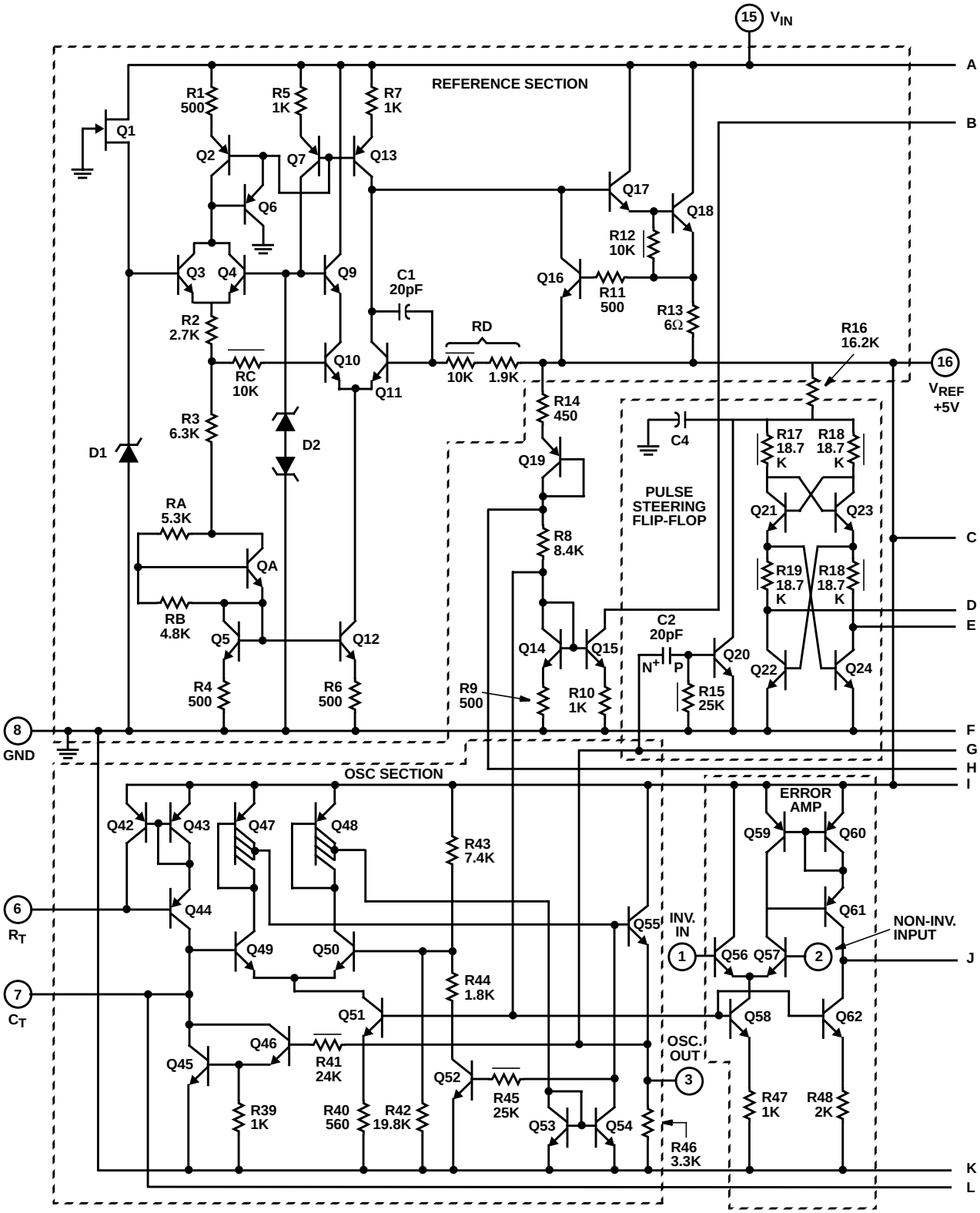


FIGURE 4. SCHEMATIC DIAGRAM OF CA1524 SERIES IC

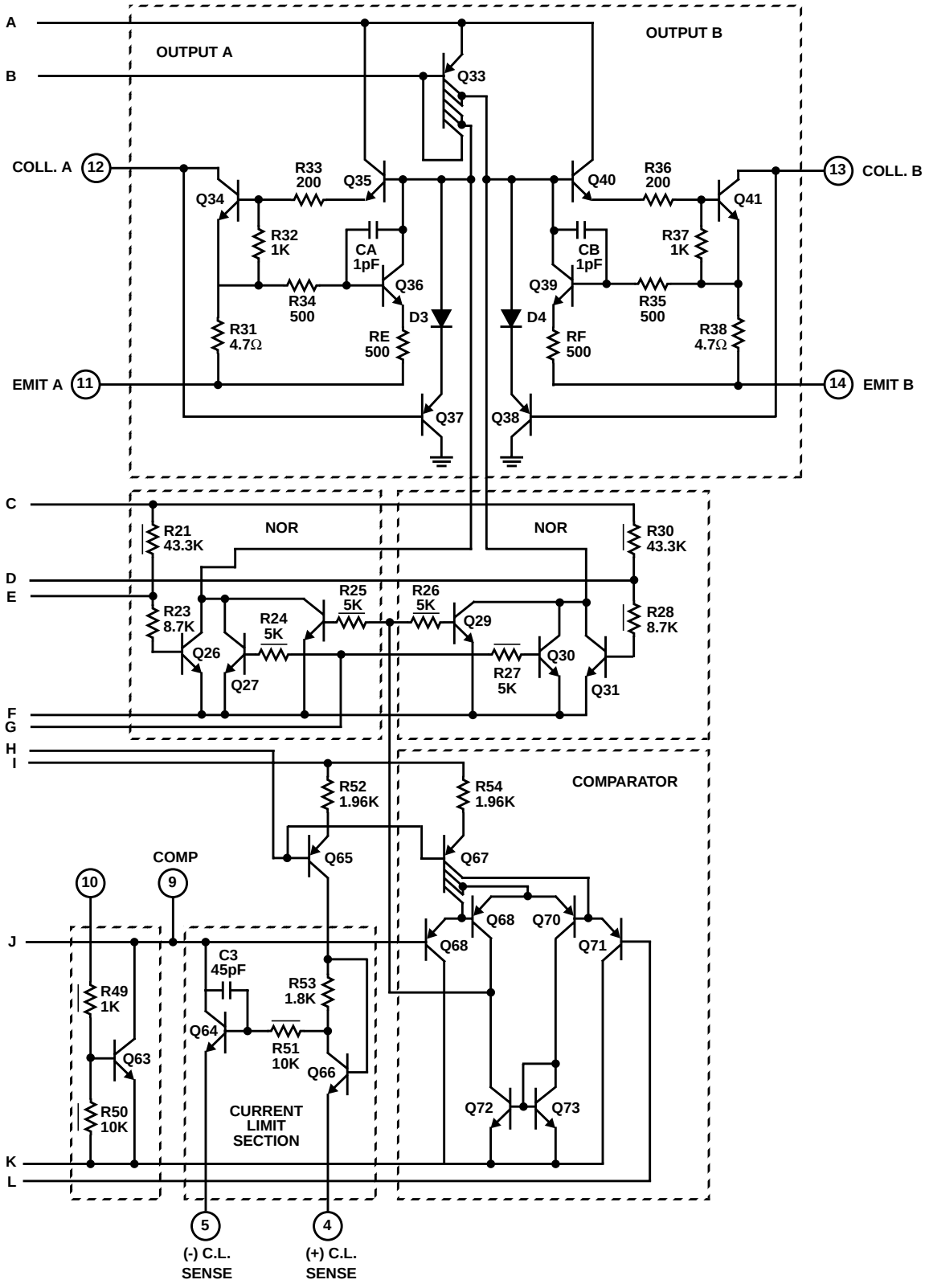


FIGURE 4. SCHEMATIC DIAGRAM OF CA1524 SERIES IC (Continued)

Figure 5 shows the temperature variation of the reference voltage with supply voltages of 8V to 40V and load currents up to 20mA. Load regulation and line regulation curves are shown in Figures 6 and 7, respectively.

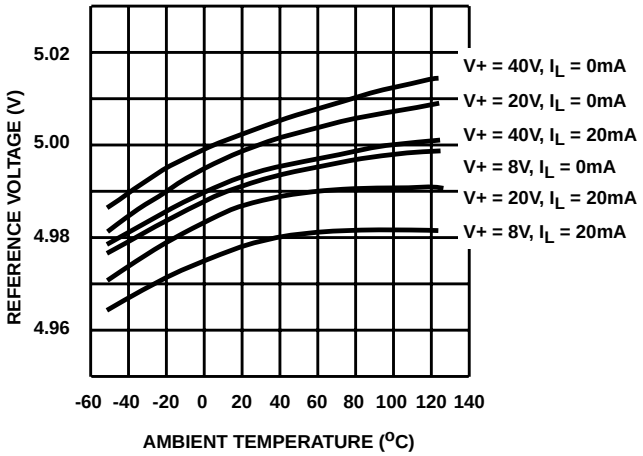


FIGURE 5. TYPICAL REFERENCE VOLTAGE AS A FUNCTION OF AMBIENT TEMPERATURE

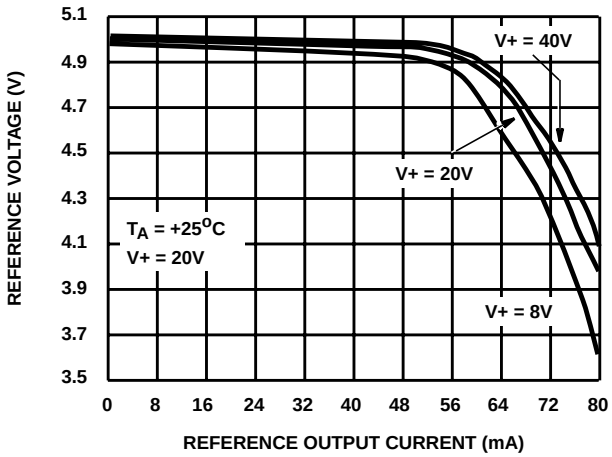


FIGURE 6. TYPICAL REFERENCE VOLTAGE AS A FUNCTION OF REFERENCE OUTPUT CURRENT

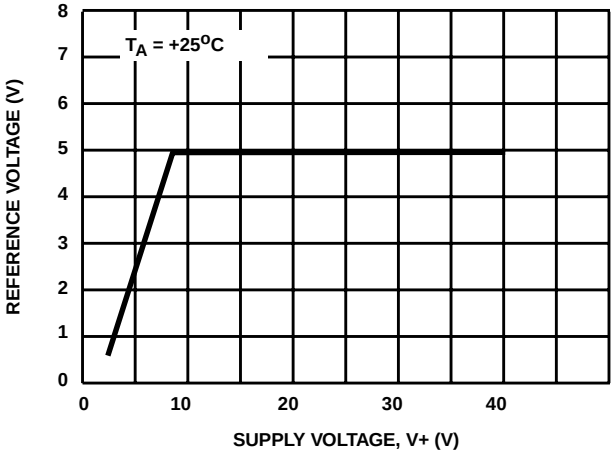


FIGURE 7. TYPICAL REFERENCE VOLTAGE AS A FUNCTION OF SUPPLY VOLTAGE

Oscillator Section

Transistors Q42, Q43 and Q44, in conjunction with an external resistor R_T, establishes a constant charging current into an external capacitor C_T to provide a linear ramp voltage at terminal 7. The ramp voltage has value that ranges from 0.6 to 3.5V and is used as the reference for the comparator in the device. The charging current is equal to $(5\text{-}2V_{BE})/R_T$ or approximately $3.6/R_T$ and should be kept within the range of 30µA to 2mA by varying R_T. The discharge time of C_T determines the pulse width of the oscillator output pulse at terminal 3. This pulse has a practical range of 0.5µs to 5µs for a capacitor range of 0.001 to 0.1µF. The pulse has two internal uses: as a dead-time control or blanking pulse to the output stages to assure that both outputs cannot be on simultaneously and as a trigger pulse to the internal flip-flop which alternately enables the output transistors. The output dead-time relationship is shown in Figure 8, a curve which is useful when a value of dead time for a particular switching transistor has to be established. A larger value of dead time will assure that both output transistors in push-pull, bridge, or forward converter configurations will not conduct simultaneously.

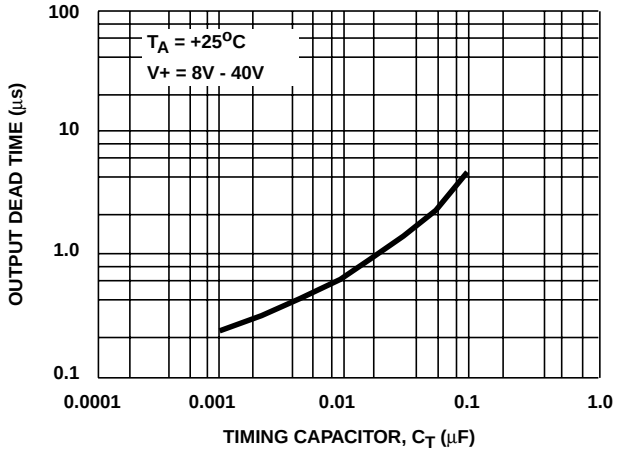


FIGURE 8. TYPICAL OUTPUT STAGE DEAD TIME AS A FUNCTION OF TIMING CAPACITOR VALUE

If a small value of C_T must be used, the pulse width can be further expanded by the addition of a shunt capacitor in the order of 100pF (but no greater then 1000pF), from terminal 3 to ground.

This shunt capacitor will expand the dead time from 0.5µs to 5.0µs when required. When the oscillator output pulse is used as a sync input to an oscilloscope, the cable and input capacitances may increase the pulse width slightly. A 2kΩ resistor at terminal 3 will usually provide sufficient decoupling of the cable. The upper limit of the pulse width is determined by the maximum duty cycle acceptable. To provide an expansion of the dead time without loading the oscillator, the circuit of Figure 9 may be used.

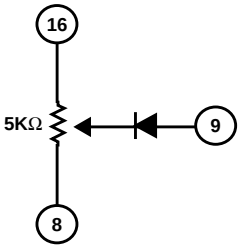


FIGURE 9. CIRCUIT FOR EXPANSION OF DEAD TIME

This diode clamp will limit the output voltage of the error amplifier; it also limits the error amplifier's source output current to about 200µA. Curves for selecting the values of the oscillator resistor (R_T) and the oscillator capacitor (C_T), as a function of oscillator period (t), are shown in Figure 10.

The oscillator period is determined by R_T and C_T, with an approximate value of $t = R_TC_T$, where R_T is in ohms, C_T is in µF, and t is in µs. Excess lead lengths, which product stray capacitances, should be avoided in connecting R_T and C_T to their respective terminals.

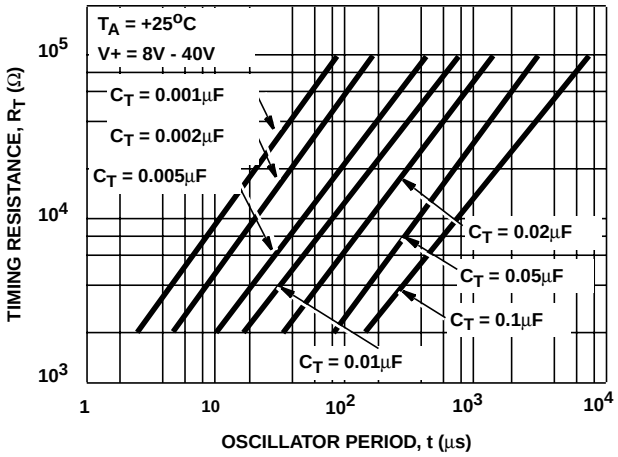


FIGURE 10. TYPICAL OSCILLATOR PERIOD AS A FUNCTION OF R_T AND C_T

For example, to obtain an oscillator period (t), select C_1 = 0.1µF and R_T = 10kΩ. Based on these values the output dead time is 0.7µs. For series regulator applications, the two outputs can be connected in parallel to provide an effective 0% - 90% duty cycle with the output stage frequency being equal to that of the oscillator. Since separate output terminals are provided, push-pull and flyback applications are possible. The flip-flop divides the frequency such that the duty cycle of each output is 0% - 45% and the overall frequency is half that of the oscillator. Curves of the output duty cycle as a function of the voltage at terminal 9 are shown in Figure 11.

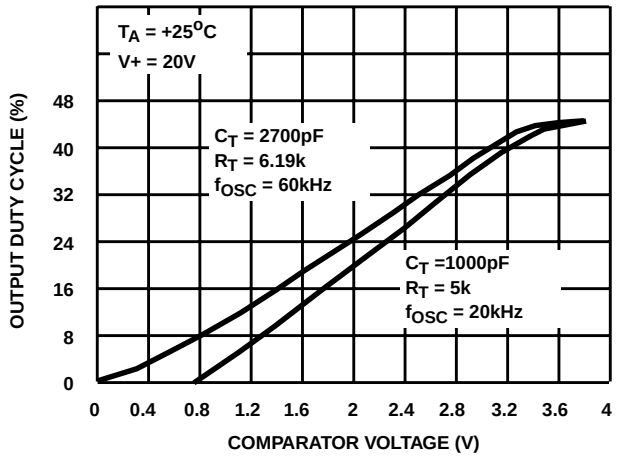


FIGURE 11. TYPICAL DUTY CYCLE AS A FUNCTION OF COMPARATOR VOLTAGE (AT TERMINAL 9)

Error Amplifier Section

The error amplifier consists of a differential pair (Q56, Q57) with an active load (Q61 and Q62) forming a differential transconductance amplifier. Since Q61 is driven by a constant current source, Q62, the output impedance R_{OUT}, terminal 9, is very high (≅ 5MΩ). The gain is:

$$Av = gmR = 8\ Ic\ R/2KT = 10^4,$$

$$\text{where } R = \frac{R_{OUT}R_L}{R_{OUT} = R_L}\quad R_L = \infty,\ Av \cong 10^4$$

Since R_{OUT} is extremely high, the gain can be easily reduced from a nominal 10^4 (80dB) by the addition of an external shunt resistor from terminal 9 to ground as shown in Figure 12. The output amplifier terminal is also used to compensate the system for AC stability. The frequency response and phase shift curves are shown in Figure 12. The uncompensated amplifier has a single pole at approximately 250Hz and a unity gain crossover at 3MHz.

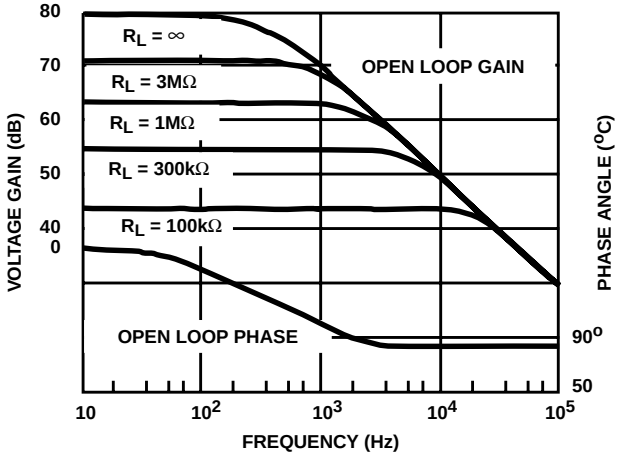


FIGURE 12. OPEN-LOOP ERROR AMPLIFIER RESPONSE CHARACTERISTICS

Since most output filter designs introduce one or more additional poles at a lower frequency, the best network to stabilize the system is a series RC combination at terminal 9 to ground. This network should be designed to introduce a zero to cancel out one of the output filter poles. A good starting point to determine the external poles is a 1000pF capacitor and a variable series 50kΩ potentiometer from terminal 9 to ground. The compensation point is also a convenient place to insert any programming signal to override the error amplifier. Internal shutdown and current limiting are also connected at terminal 9. Any external circuit that can sink 200μA can pull this point to ground and shut off both output drivers.

While feedback is normally applied around the entire regulator, the error amplifier can be used with conventional operational amplifier feedback and will be stable in either the inverting or non-inverting mode. Input common-mode limits must be observed; if not, output signal inversion may result. The internal 5V reference can be used for conventional regulator applications if divided as shown in Figure 13. If the error amplifier is connected as a unity gain amplifier, a fixed duty cycle application results.

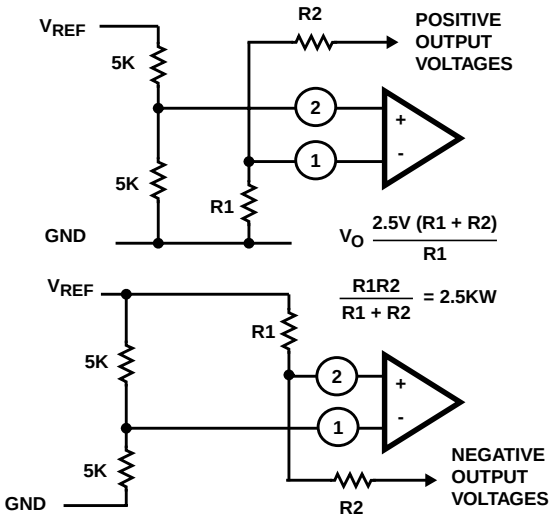


FIGURE 13. ERROR AMPLIFIER BIASING CIRCUITS

Current Limiting Section

The current limiting section consists of two transistors (Q64, Q66) connected to the error amplifier output terminal. By matching the base-to-emitter voltages of Q64 and Q66 and assuming negligible voltage drop across R51:

$$V_{THRESHOLD} = V_{BE}(Q64) + I(Q65)R53 - V_{BE}(Q66)$$
$$= I(Q65)R53 \cong 200mV$$

Although this circuit provides a small threshold with a negligible temperature coefficient, some limitations to its use must be considered. The circuit has a 11 volt common mode range which requires sensing in the ground line. The other factor to consider is that the frequency compensation provided by R51, C3 and Q64 produces a roll-off pole at approximately 300Hz.

Due to the low gain of this circuit, there is a transition region as the current limit amplifier takes over pulse width control from the error amplifier. For testing purposes, the threshold is defined as the input voltage to the current limiting amplifier to get 25% duty cycle with the error amplifier signaling maximum duty cycle.

In addition to constant current limiting, terminal 4 and 5 may also be used in transformer coupled circuits to sense primary current and shorten an output pulse, should transformer saturation occur (See Figure 37). Another application is to ground terminal 5 and use terminal 4 as an additional shutdown terminal: i.e. the output will be off with terminal 4 open and on when it is grounded. Finally, foldback current limiting can be provided with the network of Figure 14. This circuit can reduce the short circuit current (I_{SC}) to approximately 1/3 the maximum available output current (I_{MAX}).

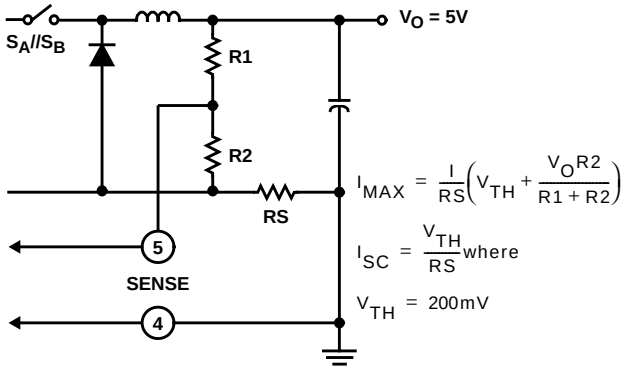


FIGURE 14. FOLDBACK CURRENT-LIMITING CIRCUIT USED TO REDUCE POWER DISSIPATION UNDER SHORTED OUTPUT CONDITIONS

Output Section

The CA1524 Series outputs are two identical n-p-n transistors with both collectors and emitters uncommitted. Each output transistor response for the wide range of oscillator frequencies. Current limiting of the output section is set at 100mA for each output and 100mA total if both outputs are paralleled. Having both emitters and collectors available provides the versatility to drive either n-p-n or p-n-p external transistors. Curves of the output saturation voltage as a function of temperature and output current are shown in Figures 15 and 16 respectively.

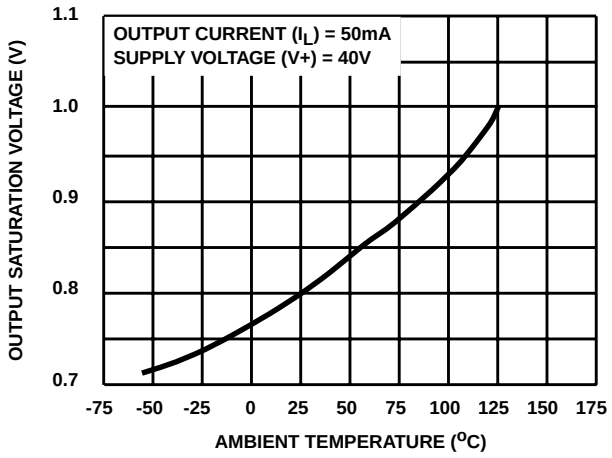


FIGURE 15. TYPICAL OUTPUT SATURATION VOLTAGE AS FUNCTION OF AMBIENT TEMPERATURE

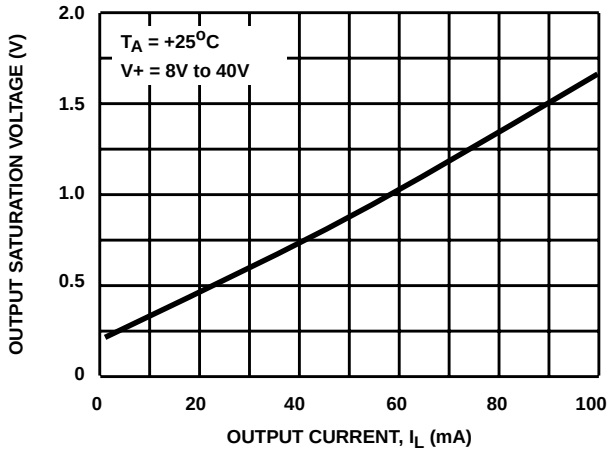


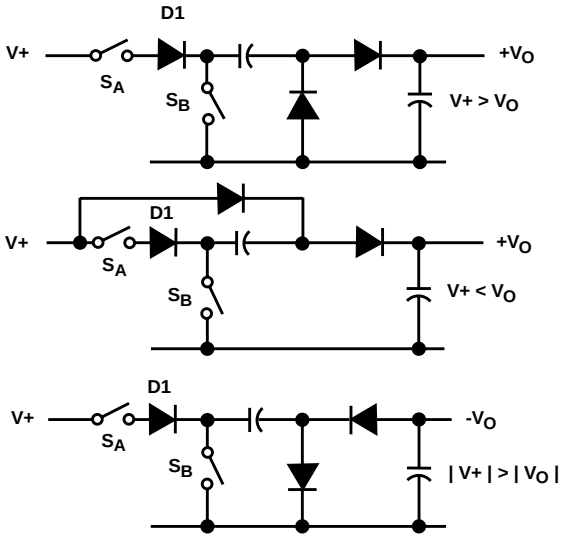
FIGURE 16. TYPICAL OUTPUT SATURATION VOLTAGE AS A FUNCTION OF OUTPUT CURRENT

There are a number of possible output configurations in the application of the CA1524 to voltage regulator circuits, they fall into three basic classifications:

1. Capacitor diode coupled voltage multipliers
2. Inductor capacitor single ended circuits
3. Transformer coupled circuits

Examples of these configurations are shown in Figures 17, 18 and 19. In each case, the switches can be either the output transistors in the CA1524 or added external transistors, depending on the load current requirements.

Capacitor diode coupled voltage multipliers are particularly useful in those low-power applications where inductive components are undesirable. Although the efficiencies of these voltage multipliers may not be as good as their inductive component counterparts, they are more efficient than the series-pass circuit.



NOTE: Diode D1 Is Necessary To Prevent Reverse Emitter-Base Breakdown of Transistor Switch S_A

FIGURE 17. CAPACITOR-DIODE COUPLED VOLTAGE MULTIPLIER OUTPUT STAGES

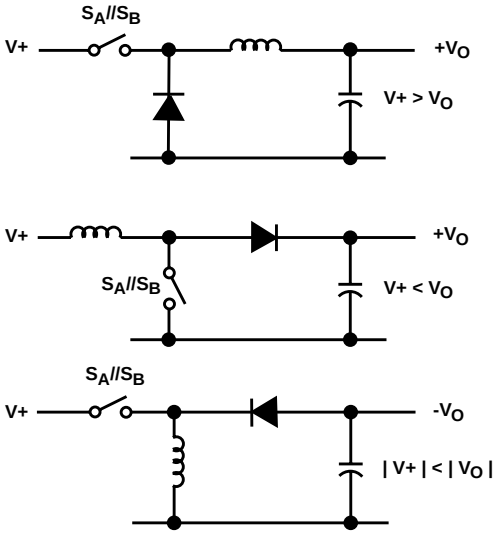


FIGURE 18. SINGLE-ENDED INDUCTOR CIRCUITS WHERE THE TWO OUTPUTS ARE CONNECTED IN PARALLEL (i.e.; SA//SB)

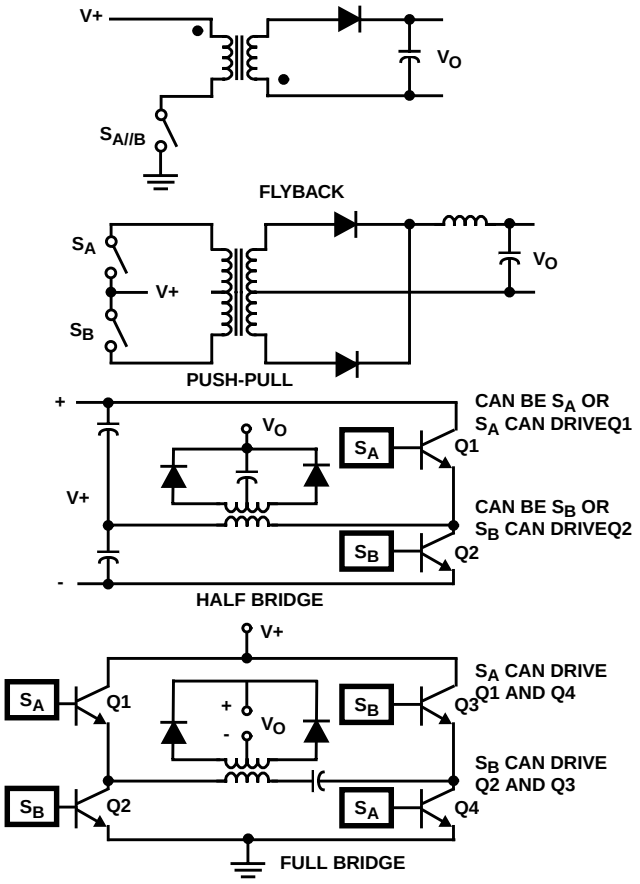


FIGURE 19. TRANSFORMER-COUPLED OUTPUTS

General Applications Considerations

The CA1524, in addition to having all the control circuits for switching regulator applications, employs two output NPN transistors. These transistors are internally current limited and can be used in a variety of switching regulator configurations.

Three such modes are:

1. Single-ended single stage configurations for forward and flyback converters.
2. Single-ended parallel output stages for switching regulators
3. Dual or individual stage configurations for push-pull, 1/2 bridge circuits, etc.

Single-Ended Applications

The single-ended configuration provides for simple regulator designs in which an LC and diode filter network provide the DC output voltage. The PWM controlled duty cycle can vary from 0% to 45%.

The duty cycle variation depends on the divided reference voltage applied to the error amplifier terminals. This voltage, in turn, adjusts the comparator's trip level to control the ON time. Figure 11 shows the duty cycle variation vs. the error amplifier output voltage (pin 9) for the CA1524.

If the outputs are connected in parallel, the duty cycle can range from 0% to 90% a normal mode for switching regulators. For flyback operation, care must be taken to prevent the on time from exceeding 45% to allow for retrace in the flyback transformer.

Dual-Ended Applications

The dual-ended configuration can be used for the following applications:

1. Push-Pull circuits
2. Voltage Multipliers; (capacitor diode filters)
3. Half or full bridge circuits

The oscillator has a dead band feature to ensure against both output transistors conducting simultaneously. This dead band applies not only to the internal transistors, but for any additional drivers used for push-pull applications.

When using push-pull and bridge circuits, the dead time becomes important. Since the frequency of the oscillator is $1/R_TC_T$, a good method for establishing dead band time is to select f first, C_T second, and then R_T. The value of C_T determines the dead time or discharging rate of C_T. The curves in Figures 8 and 10 are used for this purpose. The oscillator provides a ramp at the C_T terminal with an equivalent dead time pulse at Pin 3 for slaving multiple units. This terminal can also be used as an oscilloscope sync. With an output resistance of 2KΩ at Pin 3, capacitive loading of this terminal will be adequate for most applications, but for larger systems some type of external dead time adjustment must be employed. To provide an expansion of the dead time without loading the oscillator, the simple 5kΩ potentiometer and diode arrangement shown in Figure 9 can be used. The output frequency of each individual output stage is approximately half that of the oscillator frequency. When the stages are connected in parallel, $f_{OSC} = f_{OUT}$.

The selection of components - capacitors, diodes, inductors, transformer cores, etc., depends primarily on the operating frequency of the switching regulator. It is important, therefore, that care be exercised in the selection of these components. Capacitors should have low equivalent series resistance (ESR) and low equivalent series inductance (ESL), because high ESR is the principal cause of capacitor ripple, and high ESL causes high frequency ringing in the MHz region. Most capacitor manufacturers rate capacitance at 120Hz, a frequency quite different from the 20kHz - 100kHz operating frequency of PWM regulator circuits. Because the characteristics of capacitors may change with change in frequency, the careful selection of close tolerance capacitors will tend to offset any degradation in PWM regulator performance resulting from the difference in the frequency rating of capacitor vs PWM regulator circuit operating frequency.

Free-wheeling diode clamps must have fast turn on and low distributed capacitance. The DC resistance of inductors should be kept low to minimize the effects of added losses that may occur at high load currents. In addition, the selection of the size and type of transformer core will also depend on the input voltage range and on the output voltage and current requirements.

Basic Switching Regulators

Figure 20 shows the basic switching regulator, the Buck or Step-Down type. In this type of regulator V_O is always ≤ V_{IN}. The simplified waveforms for this regulator are shown in Figure 21.

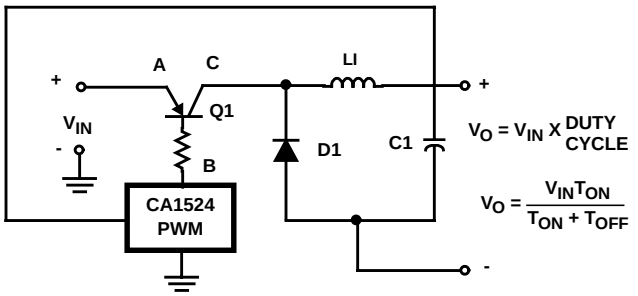
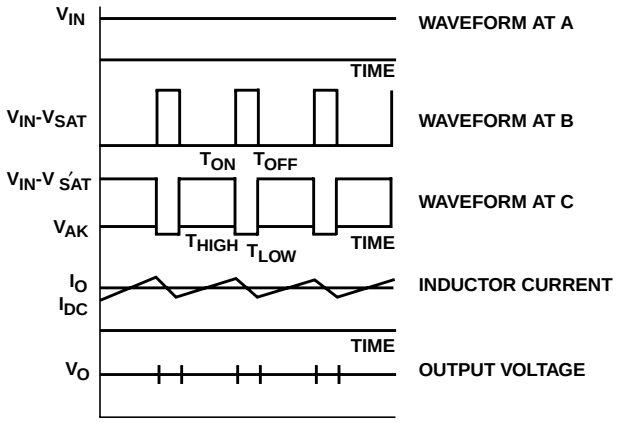


FIGURE 20. BUCK (STEP-DOWN) REGULATOR

The Buck Regulator shown in Figure 20 operates by chopping an unregulated DC voltage. The frequency of the circuit waveforms remains constant but the duty cycle is varied to effect regulation. The output LC filter, together with the free-wheeling diode D1, smooths the chopped waveform. With V_O set at some selected level by means of the reference voltage, the sample of the output voltage applied t the input of the CA1524 error amplifier adjusts the duty cycle in response to changes in load currents. When transistor Q1 is turned on diode D1 is non-conductive and current flows from V_{IN} through L1 to $+V_O$. When Q1 is off, the reserve energy in C1 provides the necessary current to the load. The overall output regulation depends primarily on the characteristics of the CA1524 and on the design of the output filter.

Switching regulator circuits are categorized for single-ended and dual-ended (bridge) applications. The basic circuits shown in Figures 22 through 30 include an inductive element. In these circuits SA represents transistor A, SB transistor B, and SA/SB indicated that both transistors can be connected in parallel. A description of the single-ended and dual-ended bridge configuration is given in subsequent pages.



V_{IN} = Unregulated DC Voltage
V_{SAT} = Saturation Voltage of CA1524 Output Transistor
$V'_{(SAT)PASS}$ = Saturation Voltage of Switching Pass Transistor
V_{AK} = Diode on Voltage
I_O = Output Inductor Current with it's DC Component
V_O = Regulated Output Voltage

FIGURE 21. SIMPLIFIED WAVEFORM FOR BUCK (STEP-DOWN) REGULATOR

Single-Ended Applications

For low-power applications up to 100 watts.

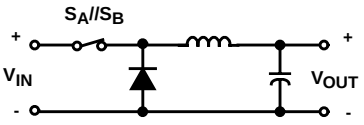


FIGURE 22. BUCK OR STEP-DOWN REGULATOR

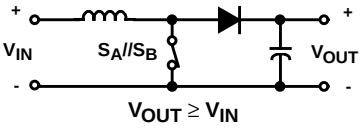


FIGURE 23. BOOST OR STEP-UP REGULATOR

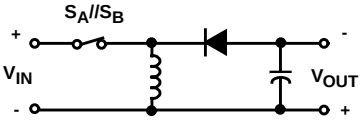
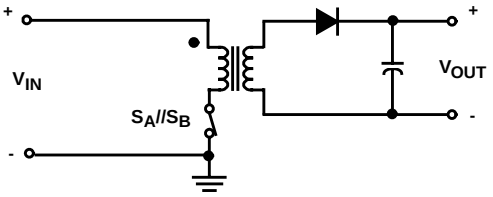
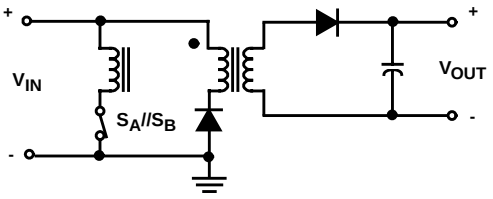


FIGURE 24. VARIATION OF THE BOOST OR STEP-UP REGULATOR RESEMBLES THE FLYBACK REGULATOR AND CAN BE EITHER STEP-UP OR STEP-DOWN

For low-power applications from 50 to 100 watts.



FLYBACK CONVERTER

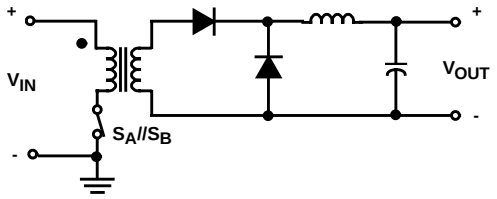


FLYBACK CONVERTER WITH CLAMP WINDING

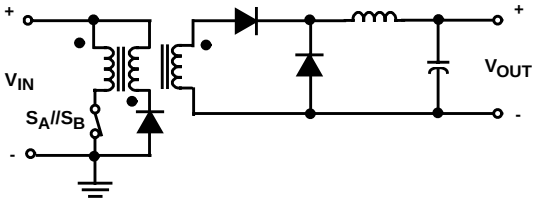
The clamp winding returns excess stored energy to the line, thereby preventing avalanche in the switching transistor.

FIGURE 25. FLYBACK CONVERTER (OPERATING MODEL FOR THIS CONVERTER IS THE BOOST REGULATOR)

For low-to-medium-power applications from 100 to 200 watts.



FORWARD CONVERTER



FORWARD CONVERTER WITH DIODE CLAMP

FIGURE 26. FORWARD CONVERTER (OPERATING MODEL FOR THIS CONVERTER IS THE BUCK REGULATOR)

Dual-Ended (Bridge) Applications

For low-to-medium-power applications from 100 to 200 watts.

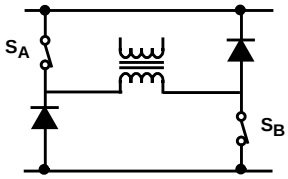


FIGURE 27. FLYBACK OR FORWARD CONVERTER WITH A CLAMP WINDING

For Medium-power applications from 200 to 500 watts.

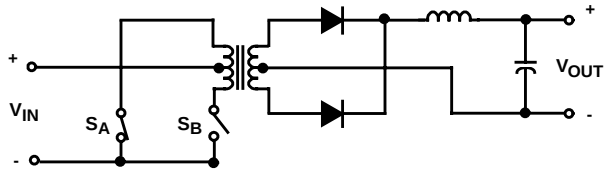


FIGURE 28. PUSH-PULL OR DC-TO-DC CONVERTER

For medium-to-high power applications from 200 to 1000 watts.

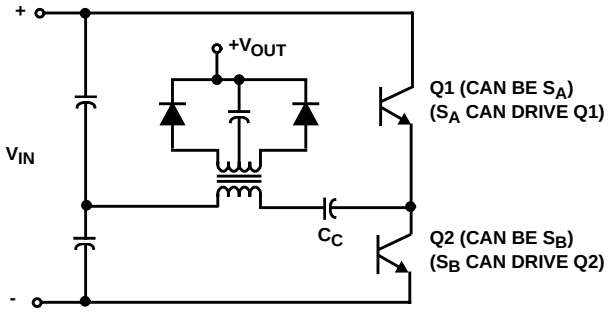


FIGURE 29. HALF-BRIDGE CIRCUIT

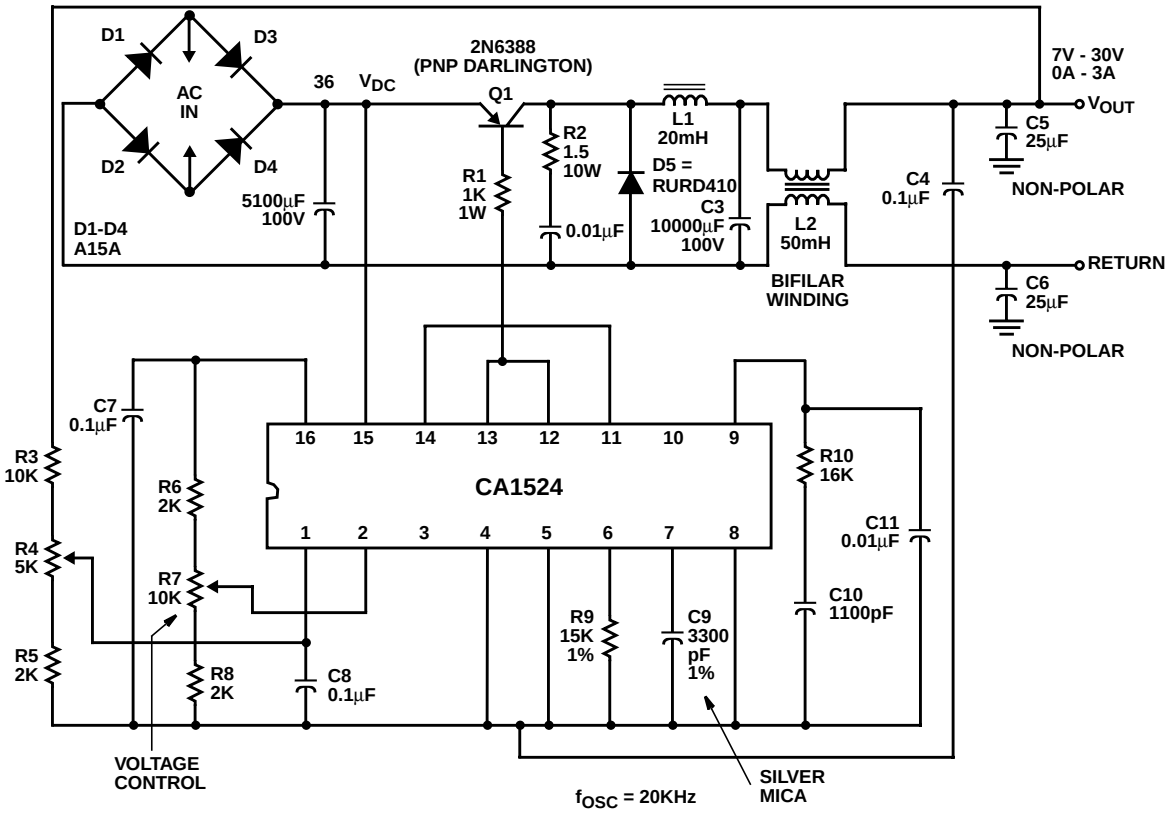


FIGURE 31. THE CA1524 USED AS A 0A TO 5A 7V TO 30V LABORATORY SUPPLY

For high-power applications from 500 to 2000 watts.

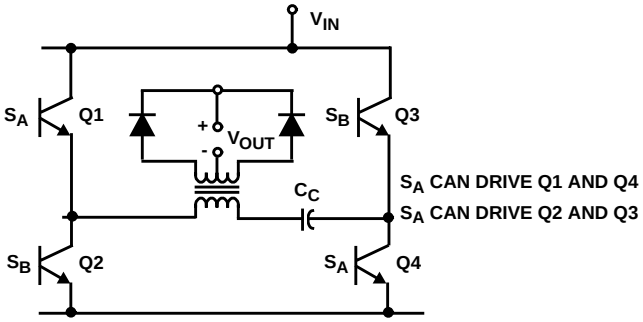


FIGURE 30. FULL-BRIDGE CIRCUIT

Capacitor C_C and diode clamps have same function as in the half-bridge circuit. In the full-bridge circuit full line voltage can be applied to the primary winding to approximately double the power output of the half-bridge circuit.

Regulator Applications

The Variable Switcher

The following review of some of the characteristics and unique design features of a variable switching pulse-width-modulated (PWM) circuit will provide the equipment designer with some of the basic principles of a PWM circuit and its associated circuitry, and a better understanding of the CA1524 Series ICs intended for this type of application.

Although most switching regulator designs and applications imply a fixed output voltage, the CA1524 Series can be applied to a variable-output-voltage power supply.

This type of circuit provides many advantages:

1. Excellent overall efficiency for the full output range; generates less heat, thereby reducing cooling requirements.
2. Input current level ≈ maximum output current level.
3. Limited dependence on V_{IA} (i.e., $V_{IN} \geq V_{OUT}$ max. +2) at the power supply's maximum output current level.
4. Light weight due to small, light cores.
5. Space saver.

and some disadvantages:

1. Low output voltage due to the limited lower end range of the error amplifier (i.e., V_{OUT} min ≠ 0, but = 7V in this particular application).
2. Losses in efficiency when output current levels are within the range of the no load dissipation for the IC and pass transistor.
3. Time lag in changing voltage levels at no load or light loads. This time lag is due to two conditions:
   A. V_C cannot change instantaneously; and
   B. C_T remains charged since it is not performing its function of supply current to the output load when the free wheeling diode conducts.

Basic Circuit Operation

The circuit diagram of the CA1524, used as a variable output voltage power supply is shown in Figure 31. By connecting the two output transistors in parallel, the duty cycle is doubled i.e.; 0^o to 90^o. Transistor Q1, 2N6388 PNP Darlington Transistor, is used as the switching pass element. Its base is driven by the CA1524's outputs. Variability is obtained by fist presetting the error amplifier inverting input (terminal 1) to 3.4V by appropriate selection of values for resistor network R_3, R_4 and R_5, in accordance with the maximum output voltage desired, e.g.; this particular supply was adjusted so that V_{OUT} (max.) = 30V. By varying the internal reference voltage at the comparator input (Pin 9) or 0.5V to 3.8V is achieved. This output voltage will cause the ON time of the output section to vary accordingly. As the reference voltage level is varied, the feedback voltage will track that level and cause the output voltage to change according to the change in reference voltage. The operating frequency of the regulator with R_T = 16KΩ and C_T = 3300pF is 23KHz (T = 43.5µs). The output voltage is directly related to the duty cycle and can be determined by the following equation:

$$V_O = \frac{V_{IN} - V_{(SAT)}}{\frac{t_{ON}}{T}}$$

where t_{ON} is the "on" time in µs, T is the oscillator period in µs; and Q1 is operating in a saturated mode.

The following table shows both the calculated and measured data for the regulator circuit of Figure 31.

V_O (I_{LOAD} = 3A) (V)	V_{IN}-V_{SAT} (V)	t (µs)	t_{ON} (CALC.) (µs)	t_{ON} (MEAS.) (µs)
30	32.5	43.5	40.15	40.50
20	32.5	43.5	26.77	26.45
10	32.5	43.5	13.88	13.70

As the load current increases, the level of the input voltage to the D5-L1-C3 filter network decreases slightly due to an increase in the saturation voltage of Q1. this change in load causes the ON time of Q1's base to increase in proportion to the decrease in voltage at Q1's collector. This decrease in voltage, in turn, adjusts the output voltage at C_3. Resistor R_7 controls the output voltage level.

The efficiency curve for the variable output voltage power supply is shown in Figure 32 at load currents in the range of 0.5A to 3A over the full output voltage range (7V - 30V). The efficiency of the variable switcher falls short of the ideal due to the losses incurred during the fall time of Q1's collector voltage. Use of a lower frequency would improve efficiency, but would require more expensive inductive and capacitive components. Even though the efficiency values shown in Figure 32 are appreciably lower at the lower output voltages, the overall efficiency of the PWM variable supply is superior to that of the linear variable supply.

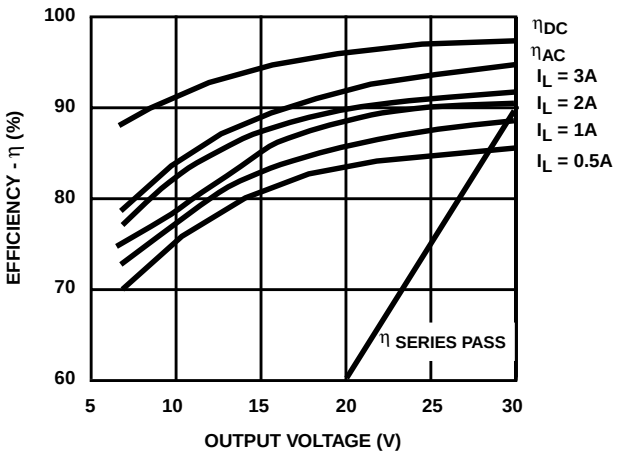


FIGURE 32A.

FIGURE 32. EFFICIENCY CURVE FOR THE VARIABLE OUTPUT VOLTAGE POWER SUPPLY SHOWN IN FIGURE 31

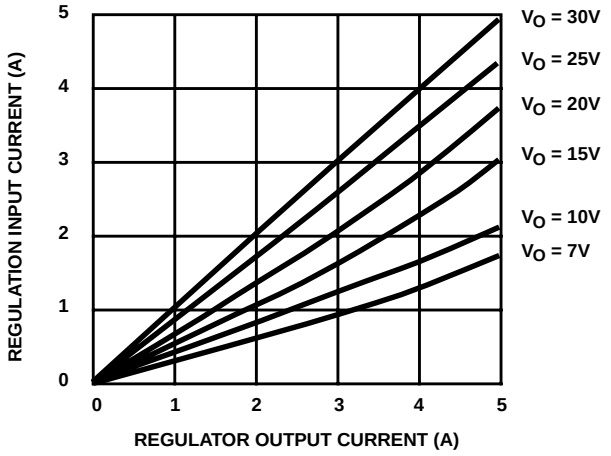


FIGURE 32B.

FIGURE 32. EFFICIENCY CURVE FOR THE VARIABLE OUTPUT VOLTAGE POWER SUPPLY SHOWN IN FIGURE 3

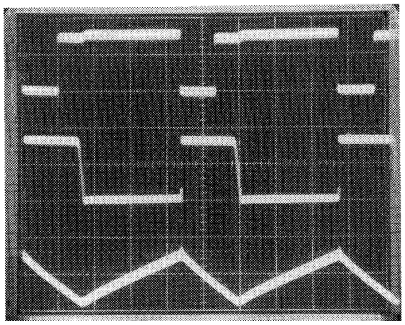


FIGURE 33A. I_{OUT} = 1A, V_{OUT} = 10V

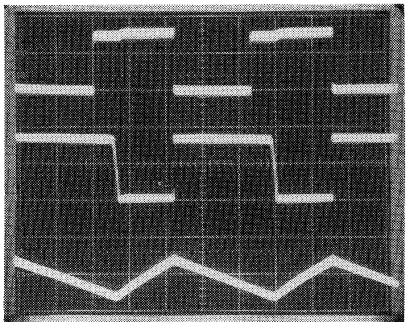


FIGURE 33B. V_{OUT} = 20V

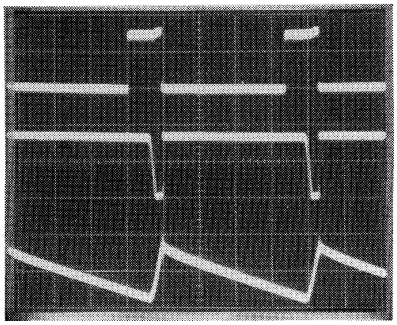


FIGURE 33C. V_{OUT} = 30V

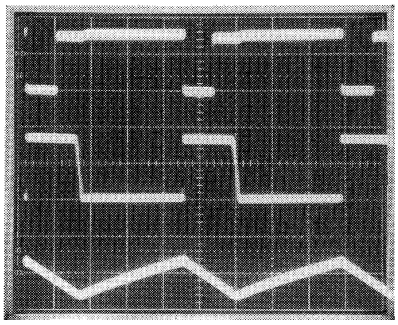


FIGURE 33D. I_{OUT} = 3A, V_{OUT} = 10V

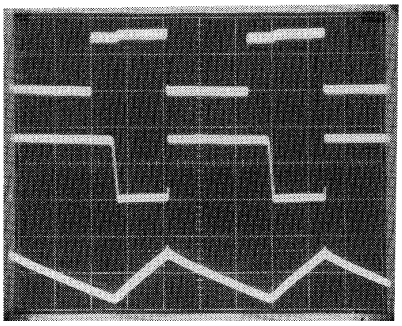


FIGURE 33E. V_{OUT} = 20V

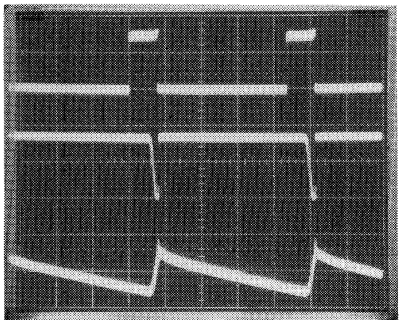


FIGURE 33F. V_{OUT} = 30V

NOTES:

All Photos: V_{IN} = 33Vdc, Horizontal - 10µs/Div
Vertical Scale Factors:
Upper Trace: CA1524 Output Voltage (Pins 12, 13) = 20V/Div
Middle Trace: Q1 Collector Voltage = 20V/Div
NOTES: Lower Trace:L_1 Current = 0.5A/Div, Figures 33A, B, D, E; 0.1A/Div, Figures 33C, F

Variable output switching power supply design employ pulse width modulation techniques to achieve high performance. Note that “on” times of Q1 and the CA1524 are more dependent on the circuit’s output voltage than by the output current to the load

FIGURE 33. TYPICAL VOLTAGE AND CURRENT WAVEFORMS FOR CA1524 PWM REGULATOR OPERATED WITH P-N-P PASS TRANSISTOR AND SERIES LC AND DIODE FILTER NETWORK

A major factor in the improved efficiency of the switching regulator is that output current does not have to be equal to input current as the output voltage swings between the end points of its range. The curves in Figure 32B show the ing regulator accomplishes its high level of efficiency. At some combinations of output voltages and currents, the large reservoir energy capacitor (C_3) supplies the difference between the required load current and available input current (see Figure 31). Note that the switching regulator has a higher efficiency for DC than AC - due primarily to the additional losses caused by the input bridge rectifiers D1 through D4 in Figure 31. However, the advantage of the linear regulator is also apparent, it can provide output voltage down to nearly zero volts.

Figure 33 shows the variation in ON time as a function of output loadings as measured at the base and collector of Q1 respectively. The regulated output voltages are 30, 20, and 10V, respectively with load currents of from 3A to 1A. The lower curve is the inductor current for the same voltages and loads. Note the change in the duty cycle and inductor current level waveforms in response to the short ON time required to supply the 30V output voltage level.

Radio frequency interference (RFI) is usually generated with any switching regulator and certain networks must be added to minimize this interference. R_2 and C_2 (Figure 31) provide a snubber network for the switching current transients of diode D5 to reduce the level of the RFI generated. The output filter network L2 and C4 through C6 provides a bifilar coil which additionally suppresses the switching noise. Varistors and input L-C filters can also be employed.

Pulse-Width Modulator (PWM) Supply Details

The CA1524 provides all sense and control functions in the variable output voltage power supply design of Figure 31. In this application, the ICs two alternately switched output stages (pins 12 and 13) are connected in parallel to drive the switching transistor (Q1). The PWM IC provides an “on” drive signal to Q1 that, in effect, spans a 0% to 90% duty cycle. (The ICs output transistors can each provide a 0% to 45% duty cycle during their alternate “on” periods, but when the outputs are connected in parallel their separate “on” times effectively add serially.) This 0% to 90% duty cycle span makes possible the design’s wide output voltage/current range without manual switching.

Other supply features include high operating efficiency (70% to 80%) over the full output voltage/current range. This high efficiency leads to fewer heat dissipation problems; therefore, the design is easier to cool and its reliability is higher than that of conventional linear designs. Additionally, because the circuit switches at a relatively high frequency (approximately 23KHz), circuit capacitors and inductors are small, and the combination of small size components with low power dissipation permits a compact overall design.

The PWM supply does present a few disadvantages. For example, output voltages of less than 7V cannot be attained because the on-chip error amplifier of the PWM device has a limited low-end range. And efficiency suffers when the output load current levels are low enough to nearly equal the active devices' no-load dissipation levels. In addition, a time lag occurs in voltage regulation with no load or light loads because C3 does not supply load current when the commutating diode D5 tries to conduct.

Component and Wiring Considerations

Besides being simple in concept, the regulator in Figure 31 is easy to construct and align. Layout isn't critical except in the ground returns where high circulating currents could cause problems. Note the indicated chassis and earth grounding points. The circuit diagram shows two separate return lines, one for all components in the power section and one for the control section. This arrangement is essential to assure good line and load regulation as well as minimal output noise. Keep the DC output well away from the switching circuits (switching occurs at 23kHz).

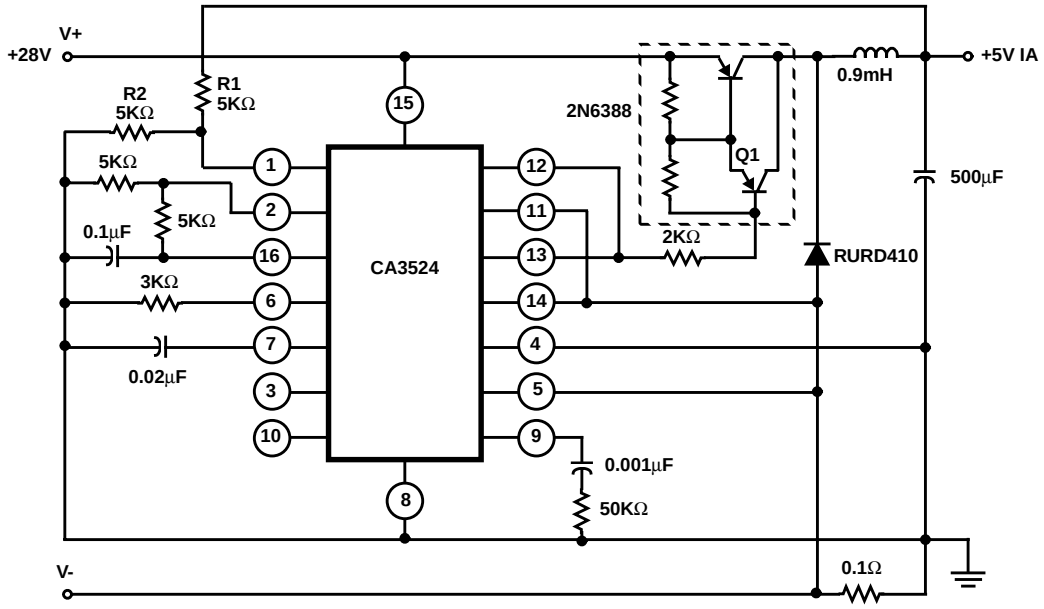


FIGURE 34. SINGLE-ENDED LC SWITCHING REGULATOR CIRCUIT

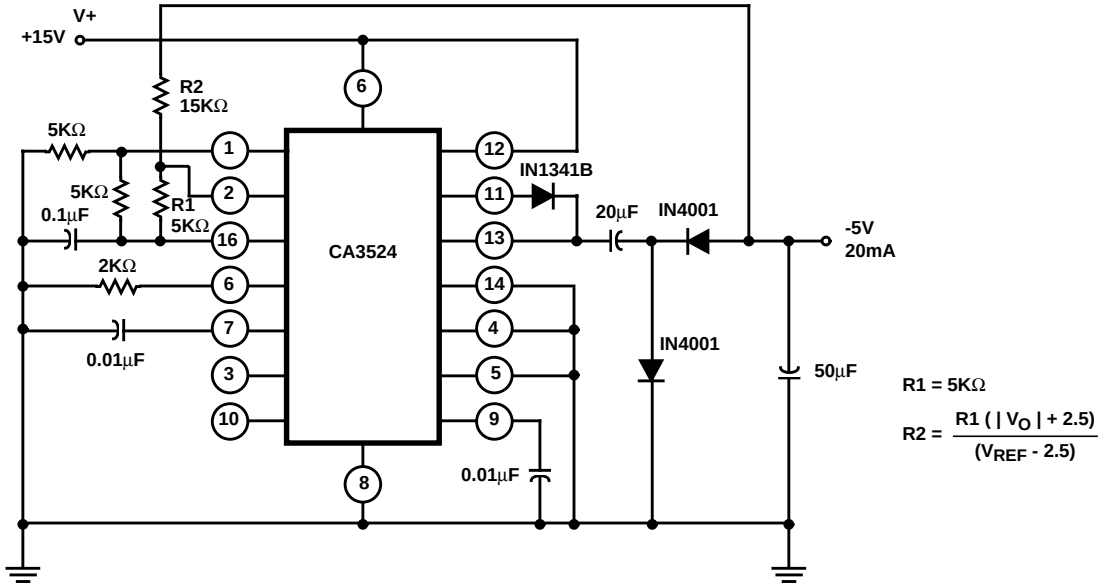


FIGURE 35. CAPACITOR DIODE OUTPUT CIRCUIT

TABLE 1. INPUT vs OUTPUT VOLTAGE AND FEEDBACK RESISTOR VALUES FOR I_L = 40mA

(For capacitor diode output circuit shown in Figure 35)

V_O (V)	R2 (kΩ)	V+ (Min) (V)	V_O (V)	R2 (kΩ)	V+ (Min) (V)
-0.5	6	8	-11	27	18
-2.5	10	9	-12	29	19
-3.0	11	10	-13	31	20
-4.0	13	11	-14	33	21
-5.0	15	12	-15	35	22
-6.0	17	13	-16	37	23
-7.0	19	14	-17	39	24
-8.0	21	15	-18	41	25
-9.0	23	16	-19	43	26
-10	25	17	-20	45	27

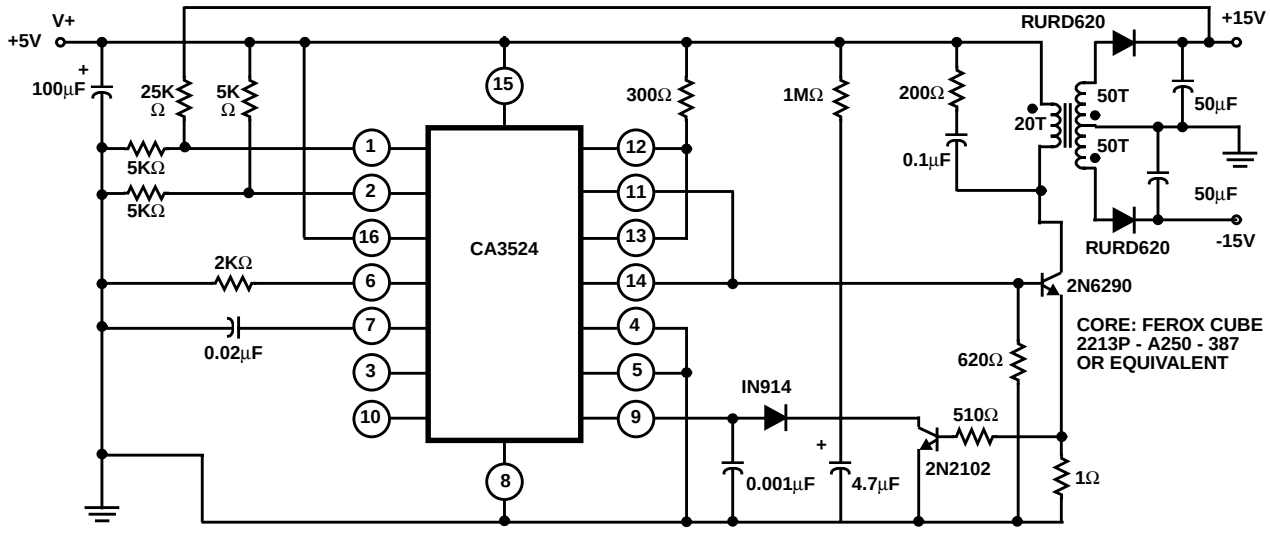


FIGURE 36. FLYBACK CONVERTER CIRCUIT

To align the supply of Figure 31, first set the PWM error amplifier's inverting input (pin 2) to approximately 33V by means of R7. (This voltage is the maximum value for the voltage control potentiometer). Then adjust the output of R4 to pin 1 to 3.4V. This value yields a maximum supply output of 30V. When the voltage control potentiometer is varied from minimum to maximum, the ICs comparator input voltage at pin 9 varies from 0.5V to 3.8V. This voltage controls the PWMs on-to-off ratio and, therefore, the conduction time of switching transistor Q1. During operation, the control voltage is set to the desired supply output voltage, and the output to the PWM feedback network consisting of R3 through R5 controls the timing.

Other Applications

Single-Ended Switching Regulator

The CA1524 in the circuit of Figure 34 has both output stages connected in parallel to produce an effective 0% - 90% duty cycle. Transistor Q1 is pulsed on and off by these output stages. Regulation is achieved from the feedback provided by R1 and R2 to the error amplifier which adjusts the on-time of the output transistors according to the load current being drawn. Various output voltages can be obtained by adjusting R1 ad R2. The use of an output inductor requires an R-C phase compensation network to stabilize the system. Current limiting is set at 1.9A by the sense resistor R3.

Capacitor Diode Output Circuit

A capacitor diode output filter is used in Figure 35 to convert +15Vdc to -5Vdc at output currents up to 50mA. Since the output transistors have built-in current limiting, no additional current limiting is needed. Table 1 gives the required minimum input voltage and feedback resistor values, R2, for an output voltage range of -0.5V to -20V with an output current of 40mA.

Flyback Converter

Figure 36 shows a flyback converter circuit for generating a dual 15V output at 20mA from a 5V regulated line. Reference voltage is provided by the input and the internal reference generator is unused. Current limiting in this circuit is accomplished by sensing current in the primary line and resetting the soft start circuit.

Push-Pull Converter

The output stages of the CA1524 provide the drive for transistors Q1 and Q2 in the push-pull application of Figure 37. Since the internal flip-flop divides the oscillator frequency by two, the oscillator must be set at twice the output frequency. Current limiting for this circuit is done in the primary of transformer T1 so that the pulse width will be reduced if transformer saturation should occur.

Low Frequency Pulse Generator

Figure 38 shows the CA1524 being used as a low frequency pulse generator. Since all components (error amplifier, oscillator, oscillator reference regulator, output transistor drivers) are on the IC, a regulated 5V (or 2.5V) pulse of 0% to 45% (or 0% to 90%) on time is possible over a frequency range of 150Hz to 500Hz. Switch S1 is used to go from a 5V output pulse (S1 closed) to a 2.5V output pulse (S1 open) with a duty cycle range of 0% to 45%. The output frequency will be roughly half of the oscillator frequency when the output transistors are not connected in parallel (75Hz to 250Hz respectively). Switch S2 will allow both output stages to be paralleled for an effective duty cycle of 0% to 90% with the output frequency range from 150Hz to 500Hz. The frequency is adjusted by R_1; R_2 controls duty cycle.

Digital Readout Scale

The CA1524 can be used as the driving source for an electronic scale application. The circuit shown in Figures 39 and 40 uses half (Q2) of the CA1524 output in a low voltage switching regulator (2.2V) application to drive the LED's displaying the weight. The remaining output stage (Q1) is used as a driver for the sampling plates PL1 and PL2. Since the CA1524 contains a 5V internal regulator and a wide operating range of 8V to 40V, a single 9V battery can power the total system. The two plates, PL1 and PL2, are driven with opposite phase signals (frequency held constant but duty cycle may change) from the pulse width modulator IC (CA1524). The sensor, S, is located between the two plates. Plates PL1, S and PL2 form an effective capacitance bridge type divider network. As plate S is moved according to the object's weight, a change in capacitance is noted between PL1, S and PL2. This change is reflected as a voltage to the amplifier (CA3160). At the null position the signals from PL1 and PL2 as detected by S are equal in amplitude, but opposite in phase. As S is driven by the scale mechanism down toward PL2, the signal as S becomes greater. The CA3160 AC amplifier provides a buffer for the small signal change noted at S. The output of the CA3160 is converted to a DC voltage by a peak-to-peak detector. A peak-to-peak detector is needed, since the duty cycle of the sampled waveform is subject to change. The detector output is filtered further and displayed via the CA3161E and CA3162E digital readout system, indicating the weight on the scale.

References

For additional information concerning regulator designs and pulse width modulator applications, and for a list of integrated circuits and power transistors suitable for series switching applications, refer to the following publications:

1. "CA1524 Series ICs Offer Efficiency in Power Supply Design".
2. Data Sheet for the CA1524, Regulating Pulse Width Modulator, File Number 1239.2
3. Application Note, ICAN-6605, "Power Devices in Off-the-Line High-Frequency Inverter/Converter Circuits". R Minton, I. Martin, and J. Vara.
4. Application Note, ICAN-6743, "900 Watt, Off-the-Line, Half-Bridge Converter Using Only Two 15A Switch Max High Voltage Power Transistors", R.B. Jarl and K.R. Kemp.
5. Application Note, ICAN-6843, "A 450 Watt, 40kHz, 240VAC to 5VDC Forward Converter Using a New Type of Transistor", R.B. Jarl and W.R. Witte
6. EDN Design Ideas, EDN Publication, December 16, 1981, "Pulse Width Modulators Measure Weights", C.P. Salerno and P.J. Stabile, RCA Solid State Division, Somerville, N.J.
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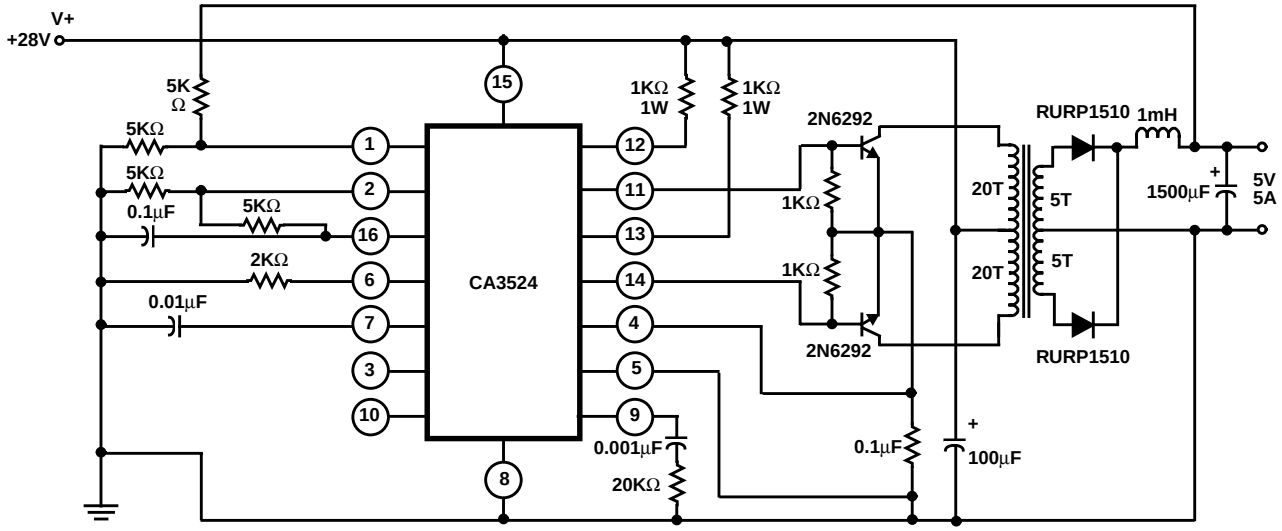
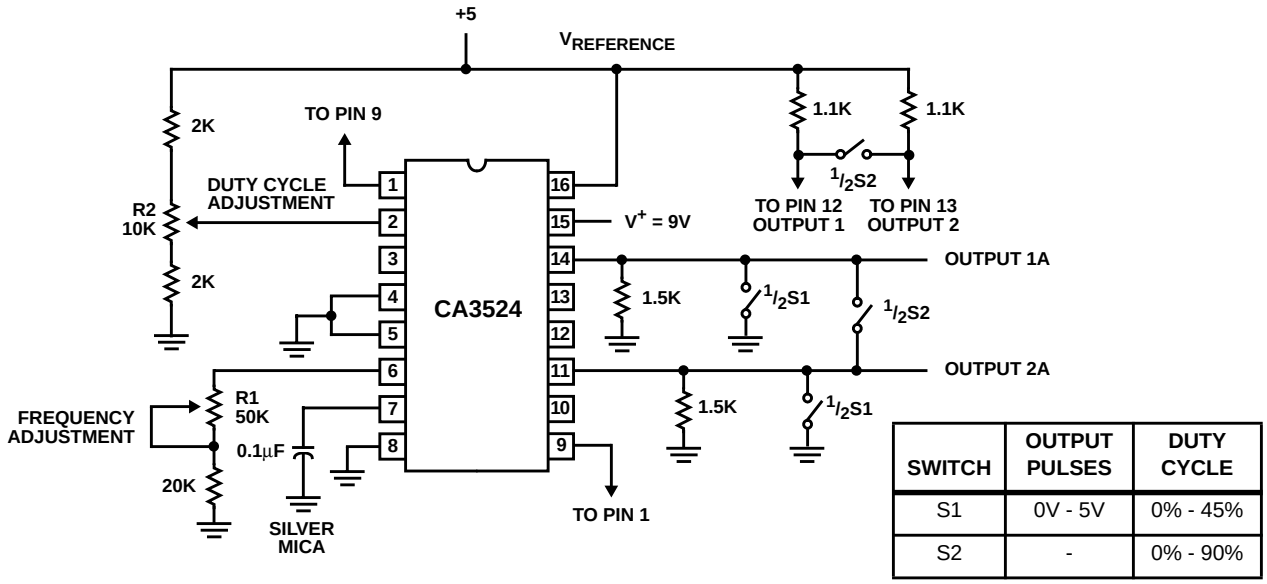


FIGURE 37. PUSH-PULL TRANSFORMER COUPLED CONVERTER



SWITCH	OUTPUT PULSES	DUTY CYCLE
S1	0V - 5V	0% - 45%
S2	-	0% - 90%

FIGURE 38. LOW FREQUENCY PULSE GENERATOR

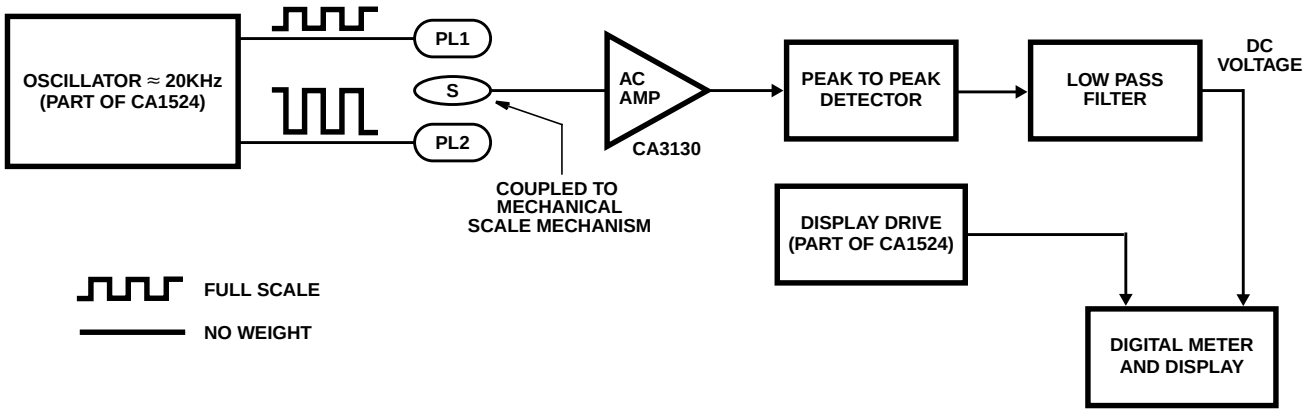


FIGURE 39. BLOCK DIAGRAM - DIGITAL READOUT SCALE CIRCUIT

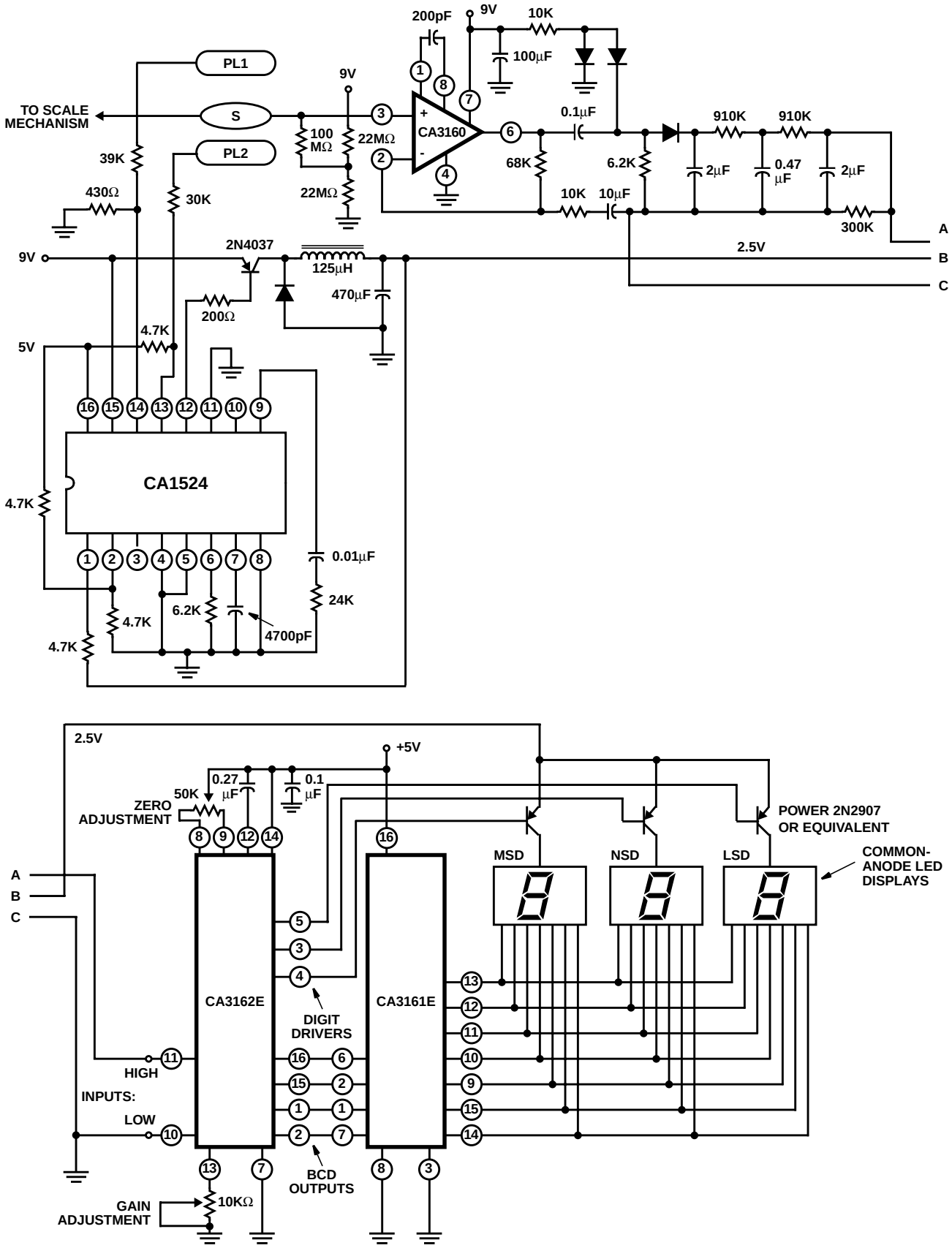


FIGURE 40. SCHEMATIC DIAGRAM OF DIGITAL READOUT SCALE

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