1/4-INCH CMOS ACTIVE-PIXEL DIGITAL IMAGE SENSOR

MT9V043

Micron Part Number: MT9V043P11ST

Description

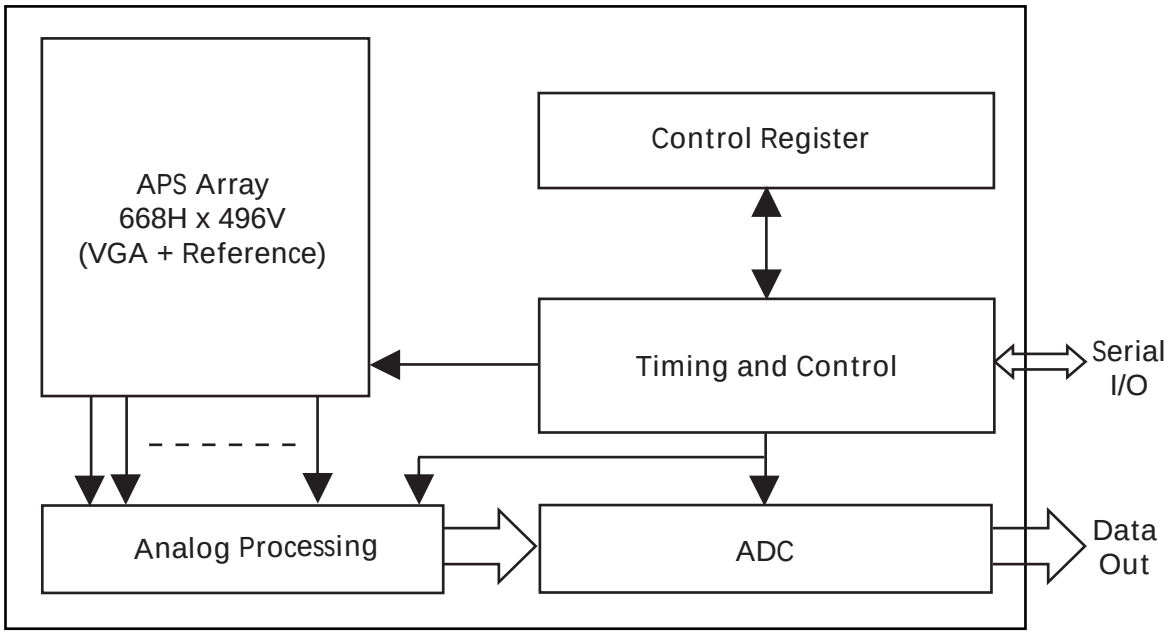
The MT9V043 is a 1/4-inch CMOS active-pixel digital image sensor. The active imaging pixel array is 640H x 480V. It incorporates sophisticated camera functions on-chip such as windowing, column mirroring and row mirroring. It is programmable through a simple two-wire serial interface and has very low power consumption.

The sensor can be operated in its default mode or programmed by the user for frame size, exposure, gain setting, and other parameters. The default mode outputs a VGA-size image at 30 frames per second (fps). An on-chip analog-to-digital converter (ADC) provides 10 bits per pixel. Frame- and line-valid signals are output on dedicated pins, along with a pixel clock which is synchronous with valid data.

Features

- Array Format: Active 640H x 480V (307,200 pixels)
  Oversize: 648H x 488V (316, 224 pixels)
  Total including dark pixels: 668H x 496V (331,328 pixels)
- Pixel Size and Type: 5.6µm x 5.6µm active-pixel photodiode
- Color Filter Array: R, G, and B primary color filters
- Optical Format: 1/4-inch
- Supply Voltage 2.55V to 3.05V, 2.8V nominal
- Frame Rate: 30 fps progressive scan; programmable
- Pixel Rate: 13.5 MHz at 27 MHz master clock
- Responsivity (green pixels): 1.8 V/lux-sec with source illumination @ 550nm
- SNR_{max}: >45dB
- Dynamic Range: 60dB
- Shutter: Electronic rolling shutter (ERS)
- Programmable Controls: Gain, frame rate, left-right and up-down image reversal
- Window Size: VGA; programmable to any smaller format (QVGA, CIF, QCIF, etc.)
- ADC: On-chip, 10-bit serial
- Power Consumption: 42mW @ 30 fps and 37mW @ 15 fps
- Package: 28-pin PLCC, Die (in Wafer form)

Figure 1: Block Diagram



Pin Description

Figure 2: Functional Diagram

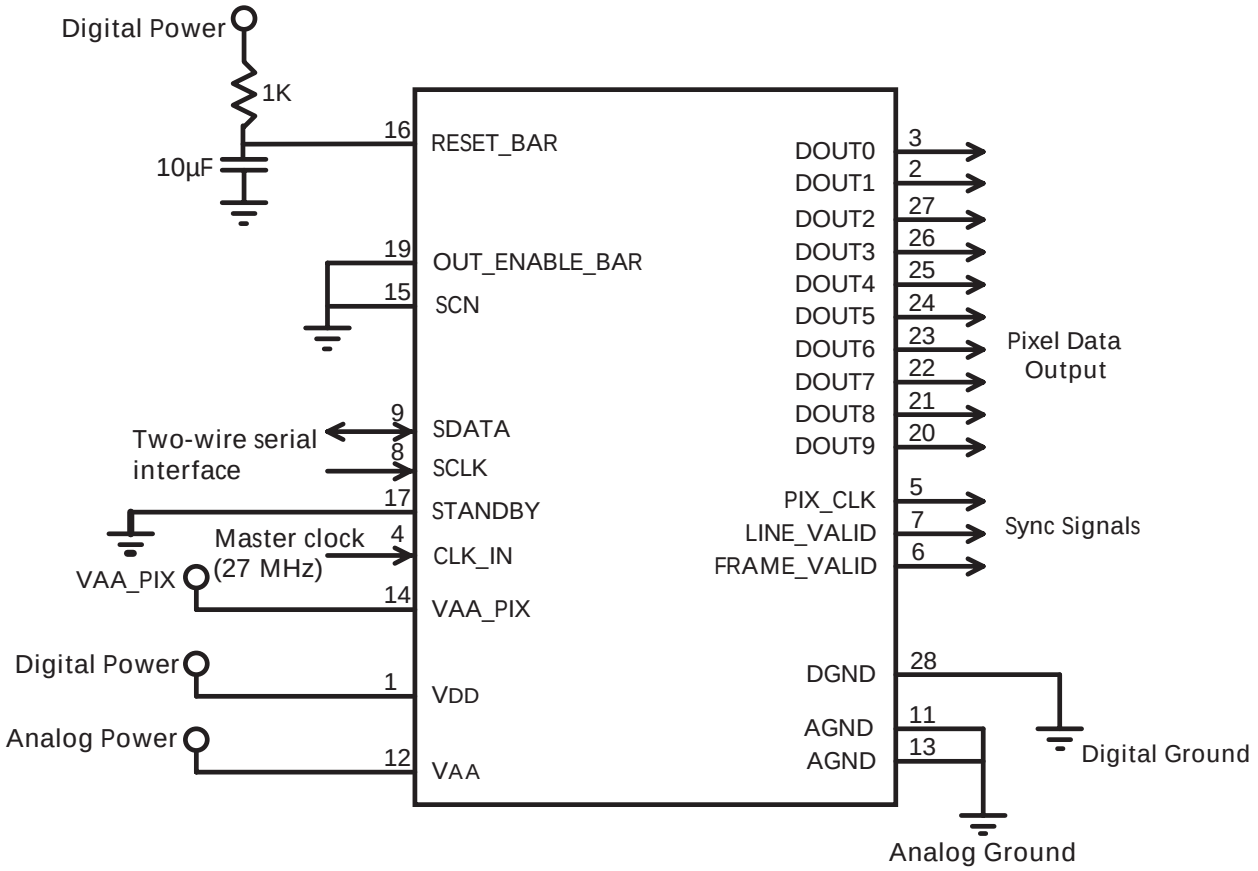


Table 1: Pin Descriptions

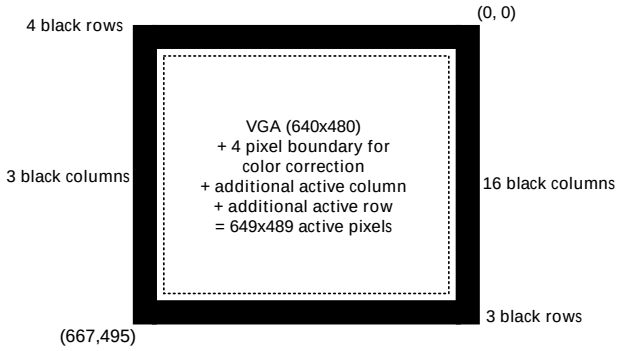
PIN NUMBER	NAME	TYPE	DESCRIPTION
1	VDD	Power	Digital power supply (2.8V)
2	DOUT1	Output	Pixel data output bit 1, D1
3	DOUT0	Output	Pixel data output bit 0, D0 (LSB)
4	Master Clock	Input	Master clock into sensor (27 MHz maximum)
5	Pixel Clock	Output	Pixel clock out. Pixel data outputs are valid during rising edge of this clock. Frequency = 1/2 (Master Clock)
6	Frame Valid	Output	Active high during frame of valid pixel data
7	Line Valid	Output	Active high during line of selectable valid pixel data (see Reg #0x20 for options)
8	SCLK	Input	Serial Clock
9	SDATA	Bi-directional	Serial data I/O
10	NC	–	No Connect
11	AGND	Ground	Analog ground
12	VAA	Power	Analog power (2.8V)
13	AGND	Ground	Analog ground
14	VAAPIX	Power	Pixel power (2.8V)
15	Scan	Input	Scanchain Enable - must be grounded for sensor operation
16	Reset Bar	Input	Asynchronous reset of sensor when low. All registers assume factory defaults.
17	Standby	Input	When high: disables the imager
18	NC	–	No Connect
19	Output Enable Bar	Input	When high: disables the pixel data output drivers
20	DOUT9	Output	Pixel data output bit 9, D9 (MSB)
21	DOUT8	Output	Pixel data output bit 8, D8
22	DOUT7	Output	Pixel data output bit 7, D7
23	DOUT6	Output	Pixel data output bit 6, D6
24	DOUT5	Output	Pixel data output bit 5, D5
25	DOUT4	Output	Pixel data output bit 4, D4
26	DOUT3	Output	Pixel data output bit 3, D3
27	DOUT2	Output	Pixel data output bit 2, D2
28	DGND	Ground	Digital ground

Pixel Data Format

Pixel Array Structure

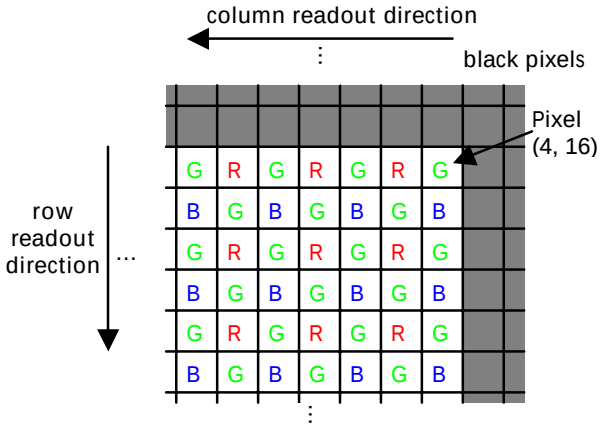
The MT9V043 pixel array is 668 columns by 496 rows. The first 16 columns and the first 4 rows of pixels are optically black, and can be used to monitor the black level. The last 3 columns and the last 3 rows of pixels are also optically black. The black row data is used internally for the automatic black level adjustment. However, the black rows can also be read out by setting the sensor to raw data output mode (Reg0x20, bit 11 = 1). There are 649 columns by 489 rows of optically active pixels, which provides a four-pixel boundary around the VGA (640 x 480) image to avoid boundary affects during color interpolation and correction. The additional active column and additional active row are used to allow horizontally and vertically mirrored readout to also start on the same color pixel.

Figure 3: Pixel Array Description



The MT9V043 uses a Bayer color pattern. Even numbered rows have green and red color pixels, and odd numbered rows have blue and green color pixels. Likewise, even numbered columns have green and blue color pixels, and odd numbered columns have red and green color pixels. Since there are an odd number of rows and columns, the color order can be preserved during mirrored readout.

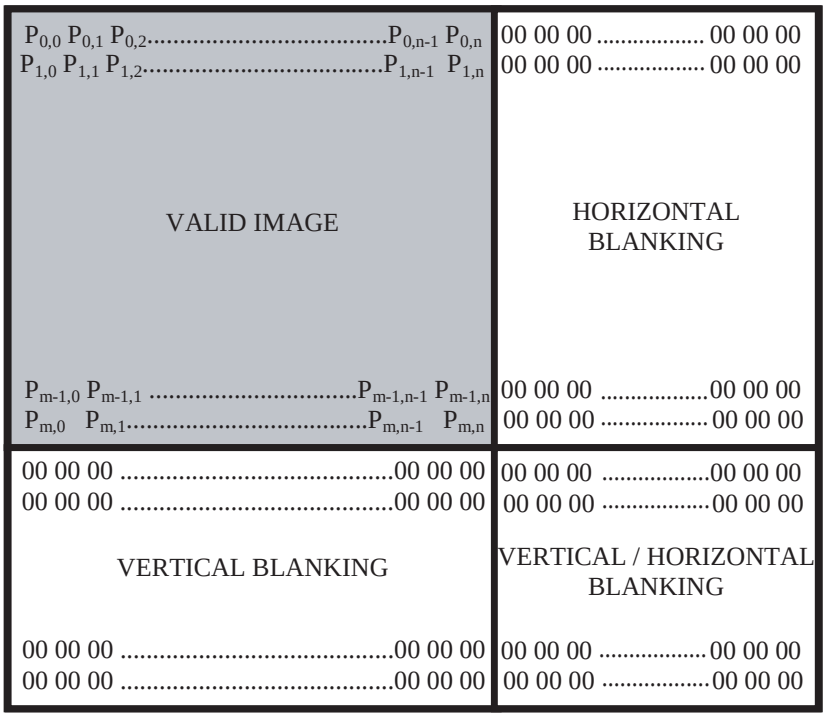
Figure 4: Pixel Color Pattern Detail (Top Right Corner)



Output Data Format

The MT9V043 image data is read-out in a progressive scan. Valid image data is surrounded by horizontal and vertical blanking, as shown in Figure 5. The amount of horizontal and vertical blanking is programmable through Reg0x05 and Reg0x06, respectively. LINE_VALID is high during the shaded region of the figure. FRAME_VALID timing is described in the next section.

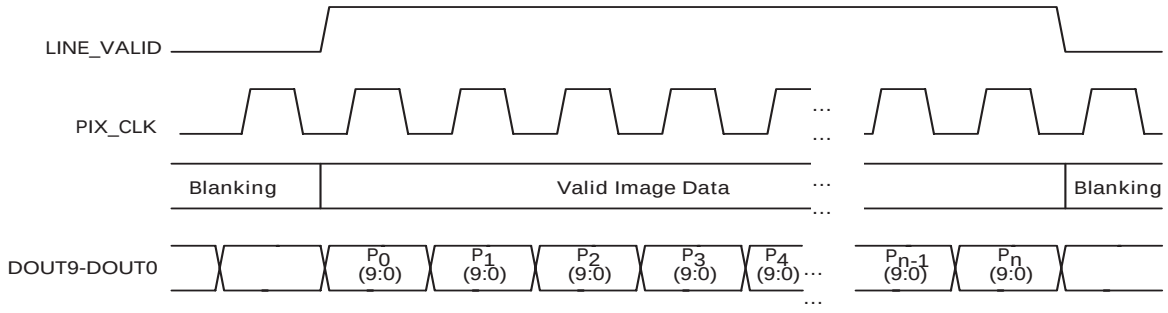
Figure 5: Spatial Illustration of Image Readout



Output Data Timing

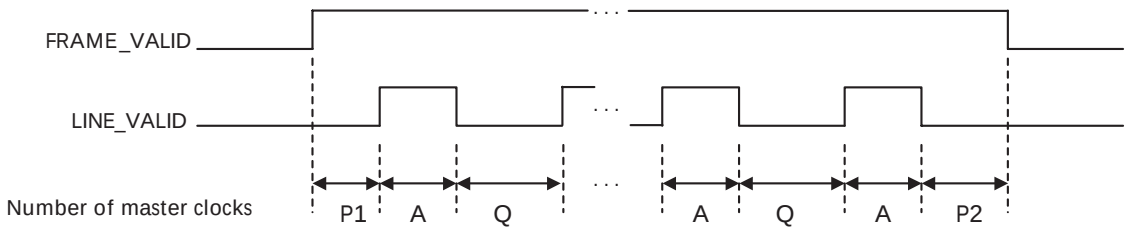
The data output of the MT9V043 is synchronized with the PIX_CLK output. When LINE_VALID is high, one 10-bit pixel datum is output every PIX_CLK period.

Figure 6: Timing Example of Pixel Data



The rising edges of the PIX_CLK signal are nominally timed to occur one-half of a master clock period after the DOUT edges. This allows PIX_CLK to be used as a clock to latch the data. The PIX_CLK is high for one complete master clock period and then low for one complete master clock period. It is continuously enabled, even during the blanking period. The MT9V043 can be programmed to move the PIX_CLK edge relative to the DOUT transitions from +1 to -1 master clock, in steps of one-half of a master clock. This can be achieved by programming the corresponding bits in Reg0x07.

Figure 7: Row Timing and FRAME_VALID/LINE_VALID Signals



Frame Timing Formulas

Table 2: Frame Time

PARAMETER	NAME	EQUATION	DEFAULT TIMING
A	Active Data Time	(Reg0x04 + 1) * (Reg0x0A + 2)	640 pixel clocks = 1280 master = 47.4µs
P1	Frame Start Blanking	(114 * (Reg0x0A + 2))	114 pixel clocks = 228 master = 8.44µs
P2	Frame End Blanking	(Reg0x05 – 7) * (Reg0x0A + 2)	10 pixel clocks = 20 master = 0.74µs
Q (P1+P2)	Horizontal Blanking	(107 + Reg0x05) * (Reg0x0A + 2)	124 pixel clocks = 248 master = 9.19µs
A+Q	Row Time	(Reg0x04 + 1) + 107 + Reg0x05) * (Reg0x0A + 2)	764 pixel clocks = 1528 master = 56.59µs
V	Vertical Blanking	(Reg0x06 + 1) * (A + Q) (minimum Reg0x06 value = 7)	83276 pixel clocks = 166552 master = 6.17ms
N_{rows} * (A+Q)	Frame Valid Time	(Reg0x03 + 1) * (A + Q)	366720 pixel clocks = 733440 master = 27.16ms
F	Total Frame Time	(Reg0x03 + 1 + Reg0x06 + 1) * (A + Q)	449996 pixel clocks = 899992 master = 33.33ms

Sensor timing is shown above in terms of pixel clock and master clock cycles. The recommended master clock frequency is 27 MHz. The vertical blank and total frame time equations assume that the number of integration rows (bits 11 through 0 of Reg0x09) is less than the number of active plus blanking rows (Reg0x03 + 1 + Reg0x06 + 1). If this is not the case, the number of integration rows must be used instead to determine the frame time, as shown in Table 3.

Table 3: Frame Time - Master Clock

PARAMETER	NAME	EQUATION (MASTER CLOCK)	DEFAULT TIMING
V’	Vertical Blanking (long integration time)	(Reg0x09 - Reg0x03)* (A + Q)	83276 pixel clocks = 166552 master = 6.17ms
F’	Total Frame Time (long integration time)	(Reg0x09 + 1) * (A + Q)	449996 pixel clocks = 899992 master = 33.33ms

Serial Bus Description

Registers are written to and read from the MT9V043 through the two-wire serial bus. The MT9V043 is a serial slave controlled by the clock (SCLK), which is driven by the two-wire serial master. Data is transferred into and out through the data (SDATA) line. The SDATA line is pulled up to 3.3V off-chip by a 1.5KΩ resistor. Either the slave or master device can pull the SDATA line down -- the serial protocol determines which device is allowed to pull the SDATA line down at any given time.

Protocol

The two-wire serial bus defines several different transmission codes, as follows:

- A Start bit.
- The slave device 8-bit address.
- An (no) Acknowledge bit.
- An 8-bit message.
- A Stop bit.

Sequence

A typical read or write sequence begins by the master sending a start bit. After the start bit, the master sends the slave device's 8-bit address. The last bit of the address determines if the request will be a read or a write, where a 0 indicates a write and a 1 indicates a read. The slave device acknowledges its address by sending an acknowledge bit back to the master.

If the request was a write, the master then transfers the 8-bit register address to which a write should take place. The slave sends an acknowledge bit to indicate that the register address has been received. The master then transfers the data 8 bits at a time, with the slave sending an acknowledge bit after each 8 bits. The MT9V043 uses 16 bit data for its internal registers, thus requiring two 8-bit transfers to write to one register. After 16 bits are transferred, the register address is automatically incremented, so that the next 16 bits are written to the next register address. The master stops writing by sending a start or stop bit.

A typical read sequence is executed as follows. First the master sends the write-mode slave address and 8-bit register address just as in the write request. The master then sends a start bit and the read-mode slave address. The master then clocks out the register data 8 bits at a time. The master sends an acknowledge bit after each 8-bit transfer. The register address is auto-incremented after every 16 bits is transferred. The data transfer is stopped when the master sends a no-acknowledge bit.

Bus Idle State

The bus is idle when both the data and clock lines are HIGH. Control of the bus is initiated with a Start bit, and the bus is released with a Stop bit. Only the master can generate the start and stop bits.

Start Bit

The start bit is defined as a HIGH to LOW transition of the data line while the clock line is HIGH.

Stop Bit

The stop bit is defined as a LOW to HIGH transition of the data line while the clock line is HIGH.

Slave Address

The 8-bit address of a serial device consists of 7 bits of address and 1 bit of direction. A 0 in the LSB of the address indicates write-mode, and a 1 indicates read-mode. The write address of MT9V043 is 0xBA, while the read address is 0xBB.

Data Bit Transfer

One data bit is transferred during each clock pulse. The serial clock pulse is provided by the master. The data must be stable during the HIGH period of the serial clock – it can only change when the serial clock is LOW. Data is transferred 8 bits at a time, followed by an acknowledge bit.

Acknowledge Bit

The master generates the acknowledge clock pulse. The transmitter (which is the master when writing, or the slave when reading) releases the data line, and the receiver indicates an acknowledge bit by pulling the data line low during the acknowledge clock pulse.

No-acknowledge Bit

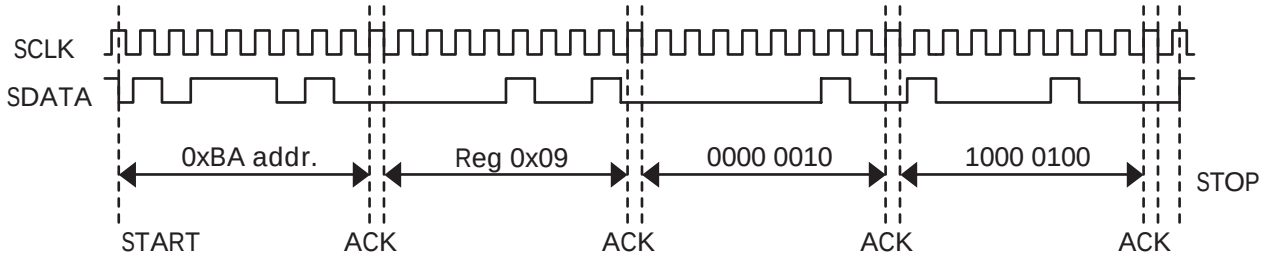
The no-acknowledge bit is generated when the data line is not pulled down by the receiver during the acknowledge clock pulse. A no-acknowledge bit is used to terminate a read sequence.

Two-Wire Serial Interface Sample Read and Write Sequences

16-bit Write Sequence

A typical write sequence for writing 16 bits to a register is shown in Figure 8. A start bit given by the master, followed by the write address starts the sequence. The image sensor will then give an acknowledge bit and expects the register address to come first, followed by the 16 bit data. After each 8 bit the image sensor will give an acknowledge bit. All 16 bits must be written before the register will be updated. After 16 bits are transferred, the register address is automatically incremented, so that the next 16 bits are written to the next register. The master stops writing by sending a start or stop bit.

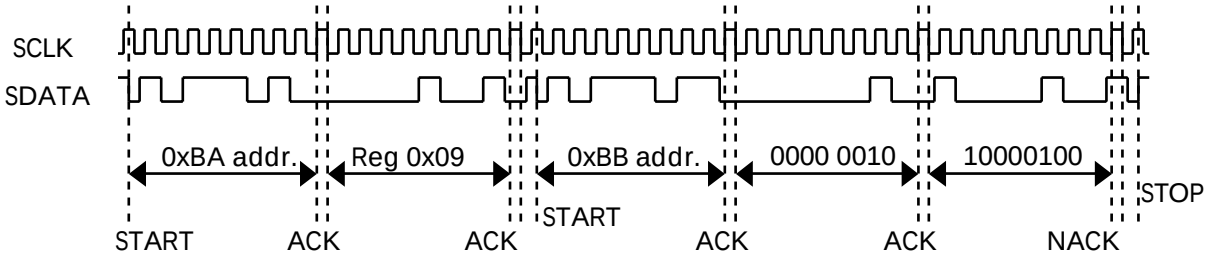
Figure 8: Timing Diagram Showing a Write to Register 0x09 with the Value 0x0284



16-bit Read Sequence

A typical read sequence is shown in Figure 9. First the master has to write the register address as in a write sequence. Then a start bit and the read address specifies that a read is about to happen from the register. The master then clocks out the register data 8 bits at a time. The master send an acknowledge bit after each 8-bit transfer. The register address is auto-incremented after every 16 bits is transferred. The data transfer is stopped when the master sends a no-acknowledge bit.

Figure 9: Timing Diagram Showing a Read From Register 0x09 with the Returned Value 0x0284



Registers

Register Map

Table 4: Register Map

REGISTER # (HEX)	DESCRIPTION	DATA FORMAT (BINARY)	DEFAULT VALUE (HEX)
0x00	Chip Version	1110 0011 0011 0010	0xE342
0x01	Row Start	0000 000d dddd dddd	0x0008
0x02	Column Start	0000 00dd dddd dddd	0x0014
0x03	Window Height	0000 000d dddd dddd	0x01DF
0x04	Window Width	0000 00dd dddd dddd	0x027F
0x05	Horizontal Blank	0000 00dd dddd dddd	0x0011
0x06	Vertical Blank	0000 000d dddd dddd	0x006C
0x07	Output Control	d000 dddd 0d0d dddd	0x000A
0x09	Shutter Width	0000 00dd dddd dddd	0x024C
0x0A	Pixel Clock Speed	0000 0000 000d dddd	0x0000
0x0B	Restart	0000 0000 0000 000d	0x0000
0x0C	Shutter Delay	0000 00dd dddd dddd	0x0000
0x0D	Reset	0000 0000 0000 000d	0x0000
0x1E	Digital Zoom	0000 0000 0000 00dd	0x0000
0x20	Read Mode	dddd ddd0 d0dd d0dd	0x1000
0x27	DAC Control	0000 000d d0dd 0dd0	0x0024
0x28	Iref Adjust	0000 0000 dddd dddd	0x0000
0x2B	Green1 Gain	0000 0ddd dddd dddd	0x0010
0x2C	Blue Gain	0000 0ddd dddd dddd	0x0010
0x2D	Red Gain	0000 0ddd dddd dddd	0x0010
0x2E	Green2 Gain	0000 0ddd dddd dddd	0x0010
0x32	Test Data	0000 00dd dddd dddd	0x0000
0x35	Global Gain	0000 0ddd dddd dddd	0x0010
0x3B	Vref	0000 00dd dddd dddd	0x0260
0x3C	Iref	0000 0000 dddd dddd	0x0022
0x5F	Cal Threshold	dddd dddd d0dd dddd	0x0904
0x60	Cal G1	0000 000d dddd dddd	0x0000
0x61	Cal G2	0000 000d dddd dddd	0x0000
0x62	Cal Ctrl	d0dd dddd dddd dddd	0x0498
0x63	Cal R	0000 000d dddd dddd	0x0000
0x64	Cal B	0000 000d dddd dddd	0x0000
0x65	Clock Control	0000 0000 0000 00dd	0x0000
0xF1	Chip Enable	0000 0000 0000 00dd	0x0001

NOTE:

1= always 1
0 = always 0
d = programmable

Table 5: Register Descriptions

REGISTER	BIT	DESCRIPTION
Chip ID		
0x00		This register is read-only and gives the chip id #: 0xE342
Window Control These registers control the size of the window.		
01		First row to be read out, default = 0x0008 (8)
02		First column to be read out, default = 0x0014 (20)
03		Window height (number of rows - 1), default = 0x01DF (479)
04		Window width (number of columns - 1), default = 0x027F (639)
Blanking Control These registers control the blanking time in a row (called column fill-in or horizontal blanking) and between frames (vertical blanking). Horizontal blanking is specified in terms of pixel clocks. Vertical blanking is specified in terms of row readout times. The actual imager timing can be calculated using Table 2 which describes “Row Timing and FRAME_VALID/LINE_VALID Signals.”		
0x05		Horizontal Blank, default = 0x0011 (17 pixels) Minimum = 9
0x06		Vertical Blank (number of rows - 1), default = 0x006C (108 rows) Minimum = 7
Output Control This register controls various features of the output format for the sensor.		
07	0	Synchronize changes (copied to Reg0xF1, bit1): 0 = update changes to registers that affect image brightness (integration time, integration delay, gain, horizontal and vertical blank, window size, pixel clock speed, row/column skip, row/column mirror, or zoom) at the next frame boundary. 1 = do not update any changes to these settings until this bit is returned to 0
	1	Chip Enable (copied to Reg0xF1, bit0): 1 = normal operation 0 = stop sensor readout. The digital power consumption can then be reduced to less than 5µA by turning off the master clock. When this is returned to 1, sensor readout restarts at the starting row in a new frame.
	2	Analog chain test mode: 0= adjusted reset timing (DO NOT USE), common-mode feedback disconnected one-half master clock before reset off. 1=normal operation, common-mode feedback disconnected 1 ns after reset off
	3	Adjust amplifier reset timing: 0 = normal operation, common-mode feedback disconnected one-half master clock before reset off 1= adjusted reset timing (DO NOT USE), common-mode feedback disconnected 1 ns after reset off
	6	Override pixel data: 0 = normal operation 1 = output programmed test data. First valid columns will output contents of test data register; second columns will output inverted data. Third columns will output uninverted data, fourth inverted, etc.
	8-11	Shift pixel clock: (11,10,9,8) = (1, x, x, x): shift pixel clock 1 clock earlier (0, 1, x, x): shift pixel clock one-half clock earlier (0, 0, 1, x): delay pixel clock by one-half clock (0, 0, 0, 1): delay pixel clock by 1 clock
	15	Invert pixel clock: 0 = normal operation 1 = invert pixel clock

Table 5: Register Descriptions (Continued)

REGISTER	BIT	DESCRIPTION
Pixel Integration Control These registers (along with the Window Sizing and Blanking registers) control the integration time for the pixels. The actual total integration time, T_{int}, is: T_{int} = Reg0x09 * row time - overhead time - reset delay, where: Row time = ((Reg0x04 + 1) + 107 + Reg0x05)* (Reg0x0A + 2) master clock periods Overhead time = 124 master clock periods Reset delay = 4 * Reg0x0C master clock periods If the value in Reg0x0C exceeds (row time - 284)/4 master clock cycles, the row time will be extended by (4 * Reg0x0C - (row time - 284)) clock cycles. In this expression the row time term, Reg0x09 *((number of columns) + 107 + horizontal blanking register)* (pixel clock setting + 2), corresponds to the number of rows integrated. The overhead time (124 master clocks) is the overhead time between the read cycle and the reset cycle, and the final term is the effect of the reset delay. Typically, the value of Reg0x09 is limited to the number of rows per frame (which includes vertical blanking rows), such that the frame rate is not affected by the integration time. If Reg0x09 is increased beyond the total number of rows per frame, the MT9V043 will add additional blanking rows as needed. A second constraint is that T_{int} must be adjusted to avoid banding in the image from light flicker. Under 60 Hz flicker, this means T_{int} must be a multiple of 1/120 of a second. Under 50 Hz flicker, T_{int} must be a multiple of 1/100 of a second.		
09		Number of rows of integration, default = 0x024C (588)
0C		Reset delay, default = 0x0000 (0) This is the number of master clock * 4 that the timing and control logic waits before asserting the reset for a given row.
Pixel Clock Speed		
0A		Bits 4:0 of this register determine the pixel data rate, default = 0x0000 (0). Maximum = 0x0015. Pixel clock period = 2 master clocks + [Reg0x0A, bits (4:0)]
Frame Restart		
0B		Setting bit 0 to '1' of Reg0x0B will cause the sensor to abandon the readout of the current frame and restart from the first row. This register automatically resets itself to 0x0000 after the frame restart. The first frame after this event is considered to be a “bad frame” (see description for Reg0x20, bit 0).
Reset		
0D		This register is used to reset the sensor to its default, power-up state. To reset the MT9V043, first write a 1 into bit 0 of this register to put the MT9V043 in reset mode, then write a 0 into bit 0 to resume operation.
Zoom Mode In zoom mode, the pixel data rate is slowed down by a factor of either 2 or 4, and either 1 or 3 additional blank rows are added between each output row. This is designed to give the controller logic time to repeat data to fill in a window that is either 2 or 4 times larger with repeated data. The pixel clock speed is not affected by this operation, and the output data for each pixel is valid for either 2 or 4 pixel clocks. In zoom by 2 mode, every row is followed by a blank row (with its own line valid, but all data bits = 0) of equal time. In zoom by 4 mode, every row is followed by three blank rows. The combination of this register and an appropriate change to the window sizing registers allows the user to zoom to a region of interest without affecting the frame rate. **Note: Zoom mode should not be used with left-right image mirroring.**		
1E	0	Zoom by 2
	1	Zoom by 4 (if bit 0 is 0)

Table 5: Register Descriptions (Continued)

REGISTER	BIT	DESCRIPTION
Read Mode This register is used to control many aspects of the readout of the sensor. **To preserve a right-reading image and the correct color order, bits 15, 14, 7 and 5 should be set to 1 to invert the image. It is critical that bit 7 be set whenever bit 15 is set, and that bit 5 is set whenever bit 14 is set.**		
20	15	1 = read out from bottom to top (upside down) 0 = normal readout
	14	1 = read out from right to left (mirrored) 0 = normal readout
	7	1 = readout starting 1 row later 0 = normal readout
	5	1 = readout starting 1 column later 0 = normal readout
	13	Bit line charge: keeps pixel output lines charged. This is not recommended and will increase power consumption; keep to 0 at all times.
	12	Enable boosted reset: Resets pixels to a higher voltage. This is required to ensure adequate pixel well depth; keep to 1 at all times.
	11	1 = all 7 dark rows are read out in addition to the valid data 0 = normal readout
	10	1 = Line valid = “Continuous” Line Valid XOR Frame Valid 0 = Line Valid determined by bit 9
	9	1 = “Continuous” Line Valid (continue producing line valid during vertical blank) 0 = Normal Line Valid (default, no line valid during vertical blank).
	4	Row skip: 1 = read out two rows, and then skip two rows (i.e. row 0, row 1, row 4, row 5...) 0 = normal readout.
	3	Column skip: 1= read out two columns, and then skip two columns (as with rows) 0 = normal readout
	1	Non-destructive readout: 1= do not reset pixels after read 0 = normal operation. Not recommended, keep to 0 at all times
	0	No bad frames: 1 = output all frames (including bad frames) 0 = only output good frames.A bad frame is defined as the first frame following a change to: window size or position, horizontal blanking, pixel clock speed, zoom, row or column skip, or mirroring.
DAC Control This register controls certain aspects of the on-chip current and voltage references. The customer should not adjust them under any circumstance.		
27	8-7	Clamp voltage control: 0,0 = Normal operation, Vcl driven to columns only during pixel sampling (default) 0,1 = Disable clamp voltage driver, Vcl driven to ground 1,X = Constant clamp voltage, Vcl always driven into columns
	5	High boost: 1 = high pixel reset voltage 0 = normal pixel reset voltage (default)
	4	Load defaults: Reloads the Vref and Iref DACs with their default values, as set in the analog circuitry. A change to the Vref or Iref DAC registers will override these settings.
	2	Invert standby operation: 1 = disable analog circuitry on Standby pad = VDD (default) 0 = disable analog circuitry on Standby pad = GND
	1	No function

Table 5: Register Descriptions (Continued)

REGISTER	BIT	DESCRIPTION
Current Setting Adjustment Bits 6:0 of Reg0x28 is used to increase the current for an individual circuit by 20%. The customer should not alter these settings.		
28	7	Reverse sign of ADC test voltage input
	6	Offset voltage DAC
	5	Voltage DAC drivers
	4	Pixel output bias (Vln)
	3	Voltage DAC ladder
	2	Boost (reset high) voltage driver
	1	Reset low voltage driver
	0	Gain amplifiers
Gain Settings The gain is individually controllable for each color in the Bayer pattern as shown in the register chart. Initial Gain = bits (5:0) x 0.0625 Analog gain = (Bit 6 + 1) * (Bit 7 + 1) * Initial Gain -- (each bits give 2x gain) Total gain = (Bit 9 + 1) * (Bit 10 + 1) * Analog Gain -- (each bits give 2x gain) Bit 8 has no effect		
2B		Green1 gain, default = 0x0010 (16) = 1x gain
2C		Blue gain, default = 0x0010 (16) = 1x gain
2D		Red gain, default = 0x0010 (16) = 1x gain
2E		Green2 gain, default = 0x0010 (16) = 1x gain
35		Global gain, default = 0x0010 (16) = 1x gain. This register can be used to set all four gains at once. When read, it will return the value stored in Reg0x2B.
Test Data		
32		This is the data fed output during pixel data override (Reg0x07, bit 6 = 1). Only bits 9:0 are used. Even columns will output the test data. Odd columns will output the test data with each bit inverted.
Voltage References This register sets the on-chip voltage references. The ADC references can be determined from the following formula: ADC Vref = Vref_hi - Vref_lo = 1.045 + 0.11 * (Reg0x3B, bits 7:6) - 0.11 * (Reg0x3B, bits 5:4) The default programmed value for ADC Vref is 0001 (binary) = 0.935V. This is the recommended operational setting. ***The clamp voltage is an internal bias voltage that should NOT be changed by the customer. If the clamp voltage is incorrectly set, some sensors may fail at some operating conditions. The default programmed value for Vcl is 10 (binary) = 1.265V. This is the recommended operational setting.***		
3B	9-8	Vcl (on-chip clamp/common-mode voltage) Vcl = 1.485 - 0.11 * (Reg0x3B, bits 9:8)
	7-6	Vref_hi (ADC “top” voltage reference) Vref_hi = 1.21 + 0.11 * (Reg0x3B, bits 7:6)
	5-4	Vref_lo (ADC “bottom” voltage reference) Vref_lo = 0.165 + 0.11* (Reg0x3B, bits 5:4)
	3-0	Not Functional
Current Reference The customer should not adjust this register under any circumstances. An incorrect setting will cause some sensors to fail at some operating conditions.		

Table 5: Register Descriptions (Continued)

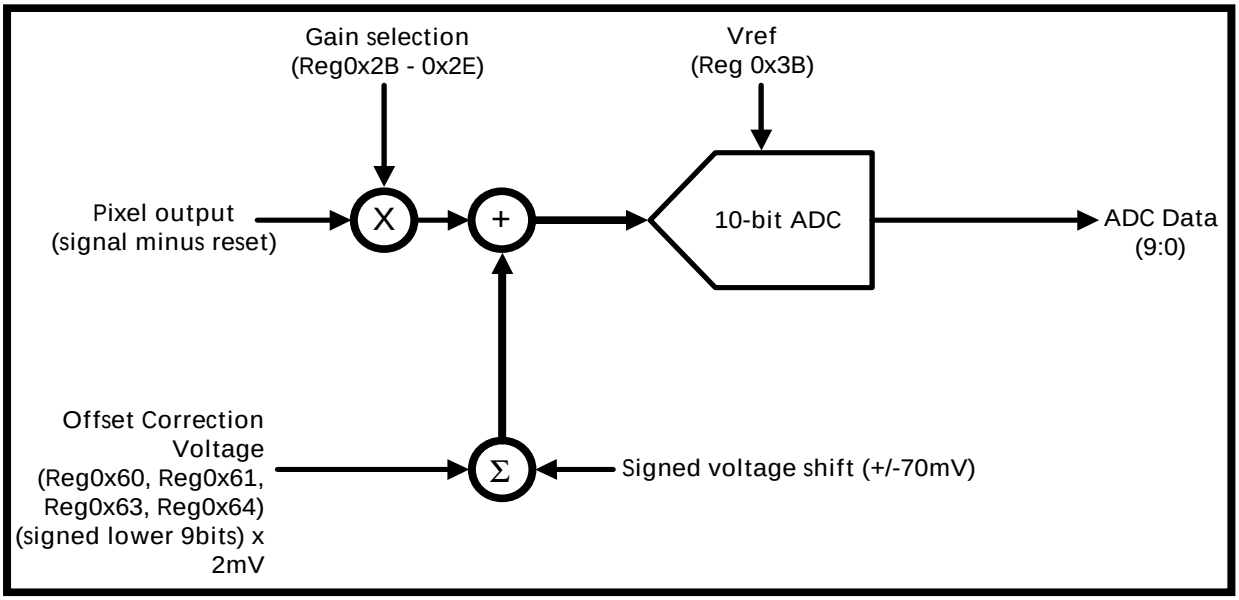
REGISTER	BIT	DESCRIPTION
3C		This register sets the on-chip current references. Iref = 10uA * (Reg0x3C, bits 7:4) - 0.625µA * (Reg0x3C, bits 3:0). If Reg0x3C, bits 7:4 = 0000, the master current will be 0µA.
Black Level Calibration These registers are used in the black level calibration. Their functionality is described in Table 7.		
Digital Clocking Register This register disables the digital logic power reduction. The user should not change this register.		
65	0	Two-wire serial interface clock: 0 = only clock two-wire serial interface logic during two-wire serial interface reads/writes (default) 1 = continuous two-wire serial interface clock
	1	Black level calibration clock: 0 = only clock black level calibration logic during dark rows of interest (default) 1 = continuous black level calibration logic clock
Chip Enable, Two-wire Serial Interface WriteSynchronize		
F1	0	Mirrors the functionality of Reg0x07 bit 1
	1	Mirrors the functionality of Reg0x07 bit 0

Feature Description

Signal Path

The signal path consists of a programmable gain, independently adjustable for each color; a programmable analog offset, also independently adjustable for each color; and a 10-bit ADC. The programmable offset operation is described below, in the section on automatic black level calibration.

Figure 10: Signal Path



ADC Voltage Reference

The ADC voltage reference is programmed through register 0x3B, bits 7:4. The ADC reference can be determined from the following formula:

ADC Vref=1.045+0.11*(Reg0x3B, bits 7:6)
-0.11 * (Reg0x3B), bits 5:4)

The default programmed value for ADC Vref is 0110 (binary) = 0.935V. This is the recommended operational setting.

The effect of the ADC calibration does not scale with Vref. Instead it is a fixed value relative to the output of the analog gain stage. Therefore, a 1LSB shift in the calibration value does not correspond to a 1 LSB shift in the output data.

It is very important to preserve the correct values of the other bits in register 0x3B. The default register setting is 0x0260. Any change to Vref should cause the new register value to be: 0x02X0, where the X represents the changed value. An incorrect setting of bits 8 and 9 could cause the sensor to fail under certain operating conditions.

Recommended Gain Settings

The analog gain circuitry (pre-ADC) is designed to offer signal gains from 1 to 15.75.

The minimum gain of 1 (register set to 0x0010) corresponds to the lowest setting where the pixel signal is guaranteed to saturate the ADC under all specified operating conditions. Any reduction of the gain below this value may cause the sensor to saturate at ADC output values less than the maximum, under certain conditions. It is recommended that this guideline be followed at all times.

Since bits 6 and 7 of the gain registers are multiplicative factors for the gain settings, there are alternative ways of achieving certain gains. Some settings offer superior noise performance to others, despite providing the same overall gain. Table 6 lists the recommended gain settings.

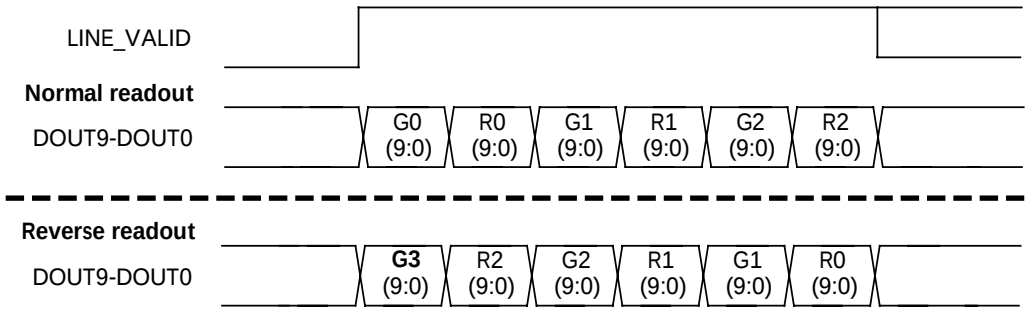
Table 6: Recommended Gain Settings

DESIRED GAIN	RECOMMENDED SETTINGS (GAIN REGISTER)	CONVERSION FORMULA (DECIMAL ARITHMETIC)
1 to 3.9375	0x10 to 0x3F	(Register value)/16
4 to 7.875	0x60 to 0x7F	(Register value - 64)/8
8 to 15.75	0xE0 to 0xFF	(Register value - 192)/4

Column and Row Mirror Image

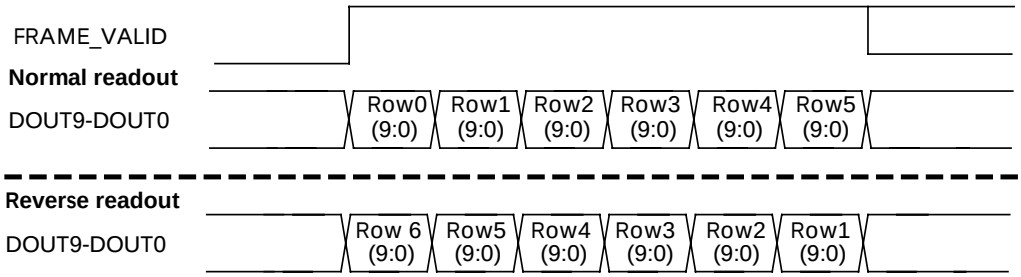
By setting bits 14 and 5 of Register 32 (0x20), the readout order of the columns will be reversed as shown in Figure 11.

Figure 11: Readout of 6 Pixels in Normal And Column Mirror Output Mode



By setting bits 15 and 7 of Register 32 the readout order of the rows will be reversed as shown in Figure 12.

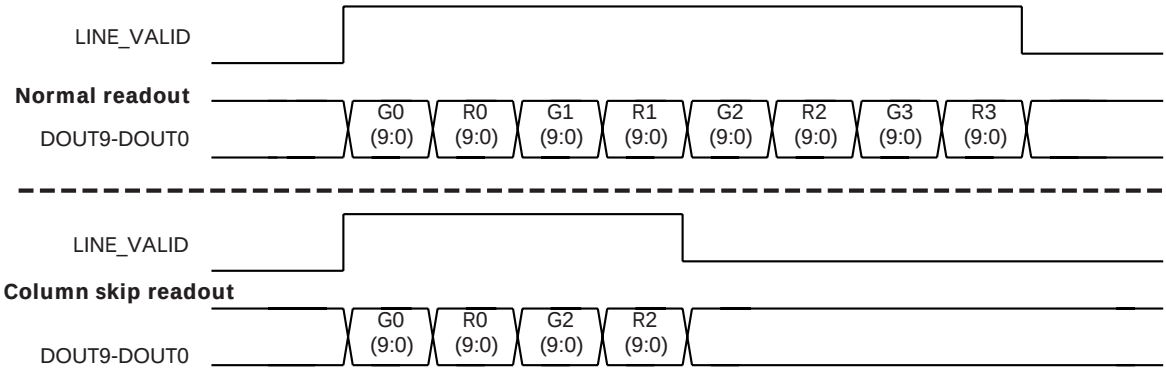
Figure 12: Readout of 6 Rows in Normal And Row Mirror Output Mode



Column and Row Skip

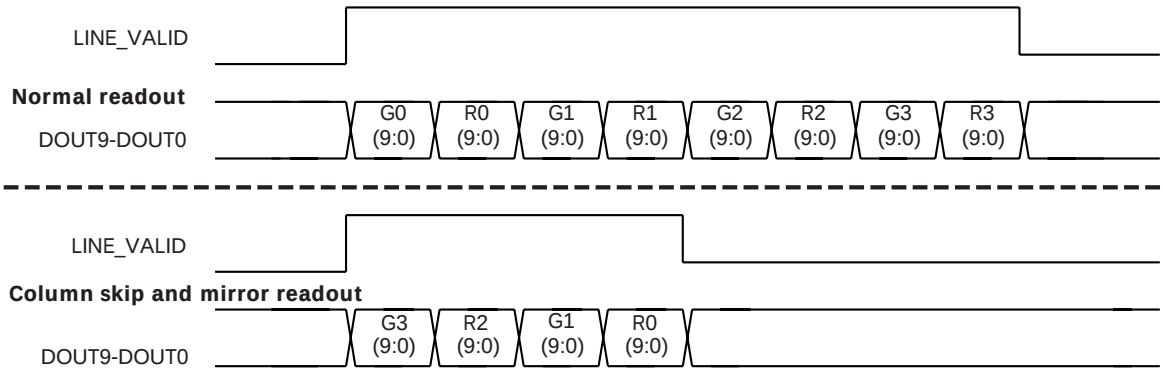
By setting bit 3 of Register 32 (0x20), only half of the column sets will be read out. An example is shown in Figure 13. Only columns with bit1 equal to 0 will be read out (xxxxxxx0x) since in default mode switch-color bit is not enabled (bit 5 of Register 32). The functionality of switch-color bit is explained in the next section. The row skip works in the same way and will only read out rows with bit 1 equal to 0. Row skip mode is enabled by setting bit 4 of Register 32 (0x20). For both row and column skips, the number of rows or columns read out will be half of what is set in Register 3 (0x03) or 4 (0x04) respectively.

Figure 13: Readout of 8 Pixels in Normal and Column Skip Output Mode



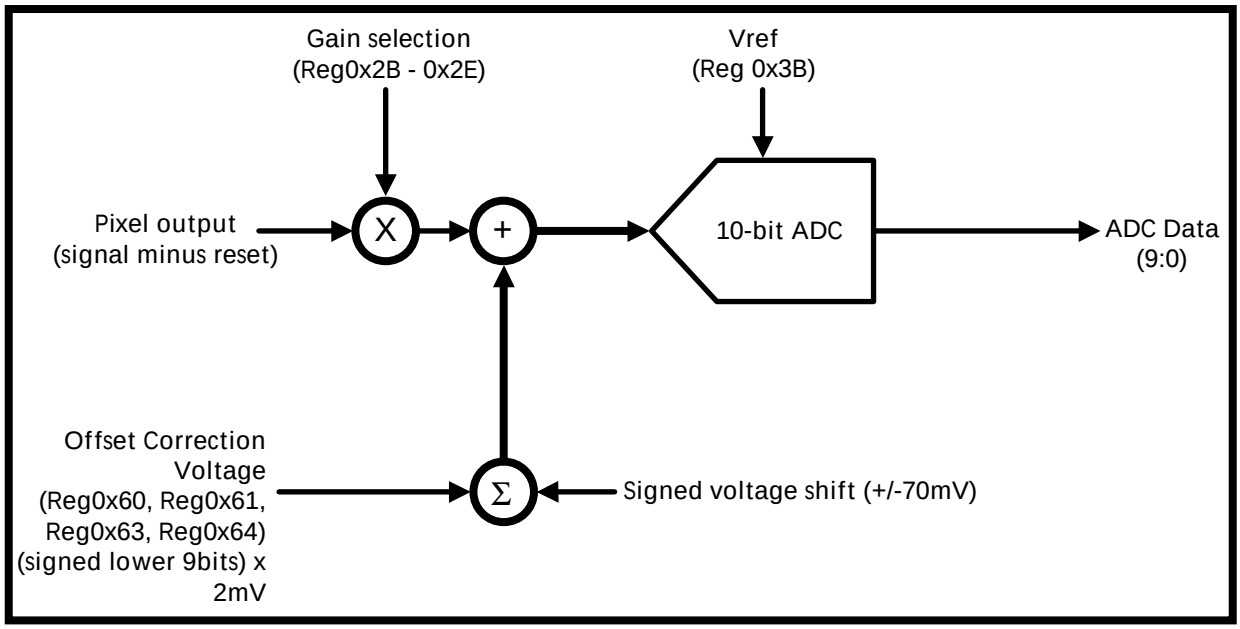
In mirror mode (Register 0x20, bits 14 and 15 set), the column skip works to maintain the correct color order. In this case, the first pixel out will be the pixel immediately after the last pixel in un-mirrored skip mode output, as shown in Figure 14.

Figure 14: Readout of 8 Pixels in Normal And Column Skip and Mirror Set



Black Level Calibration

Figure 15: Black Level Calibration Flow Chart



The MT9V043 has automatic black level calibration on-chip. This can be overridden by the user as described below.

The automatic black level calibration measures the average value of 256 pixels from two dark rows of the chip for each of the 4 colors. (The pixels are averaged as if they were light sensitive and passed through the appropriate color gain). This average is then digitally filtered over many frames.

For each color, the new filtered average is compared to a minimum acceptable level (to screen for too low a black level) and a maximum acceptable level. If the average is lower than the minimum acceptable level, the offset correction voltage for that color is increased by 1 offset LSB (Note: Offset LSBs do not match ADC LSBs. Typically, 1 offset LSB is approximately 2mV. If it is above the maximum level, the level is decreased by 1 LSB (2mV). The upper threshold is automatically adjusted upwards whenever an upward shift in the black level from below the minimum results in a new black level above the maximum. This prevents black level oscillation from below the minimum to above the maximum. The lower threshold is increased with the maximum gain setting (out of all 4 colors), according to the formula described under Reg0x5F. This prevents clipping of the black level.

Whenever the gain or any of the readout timing registers is changed (shutter width, vertical blank, number of rows or columns, or the shutter delay) or if the black level recalculation bit, reset bit or restart bit is set, the running digitally filtered average is reset to the first average of the dark pixels. The digital filtering over many frames is then restarted. Whenever the gain or the readout timing registers are changed, the upper threshold is restored to its default value.

After changes to the sensor configuration, large shifts in the black level calibration can result. To quickly adapt to this shift, a rapid sweep of the black level during the dark row readout is performed on the first frame after certain changes to the sensor registers. Any changes to the registers listed above will cause this recalculation. The data from this sweep allows the sensor to choose an accurate new starting point for the running average. This procedure can be disabled as described below.

There is a built-in voltage skew between calibration values of -1 and 0, forcing the calibration corresponding to -1 to be equivalent to a positive calibration higher than 0. This ensures that there are no unreachable desired calibrations, despite chip-to-chip variations.

Table 7: Black Level Registers

REGISTER	BIT	DESCRIPTION
Reg0x5F This register controls the operation of the black level calibration thresholds.		
	15	No gain dependence: 1 = Thres_lo is set by the programmed value of bits 5:0, Thres_hi is reset to the programmed value (bits 14:8) after every black level average restart 0 = Thres_lo and Thres_hi are set automatically as described below
	14 -8	Thres_hi: Maximum allowed black level in ADC LSBs (default = Thres_lo + 5) Black level maximum is set to this value when bit 7 = 1, black level maximum is reset to this value after every black level average restart if Bit 15 = 1 and bit 7 = 0
	7	1 = Override automatic Thres_hi and Thres_lo adjust (Thres_hi always = bits 14:8, Thres_lo always = bits 5:0) 0 = Automatic Thres_hi and Thres_lo adjustment
	5-0	Thres_lo: Lower threshold for black level in ADC LSBs Under default automatic operation (bit 7 = 0, bit 15 = 0) Thres_lo = RegGainmax/4 x (RegGainmax, bit 6 +1) x (RegGainmax, bit 7 +1), where RegGainmax is the maximum of the four independent gain register settings. Whenever a jump in the calibration causes the black level data to change from below Thres_lo to above Thres_hi, Thres_hi is adjusted according to the following: If new black level < 64: Thres_hi = Thres_lo + 2 + (2 x Delta), where Delta = new black level - Thres_lo If new black level > 63 and < 119: Thres_hi = new black level + 4 If new black level > 119: Thres_hi = 123 After any recalculation of the black level and average restart, Thres_hi is reset to either Thres_lo + 5 (automatic, default mode), Thres_hi (bit 7 = 1). Reg0x62, bit 11 will override this.
Reg0x62 This register is used to control the automatic black level calibration circuitry.		
	15	1 = Do not perform the rapid black level sweep on new gain settings 0 = normal operation
	14	No functionality
	13	Extend bit for offset correction 1 = 3mV offset LSB 0 = 2mV offset LSB (default)
	12	1 = Start a new running digitally filtered average for the black level (this is internally reset to 0 immediately), and do a rapid sweep to find the new starting point.
	11	1 = do not reset the upper threshold after a black level recalculation sweep 0 = reset the upper threshold after a black level recalculation sweep (default)
	10	Enable analog signal chain. 1 = analog signal chain enabled (default) 0=analog chain input to ADC disconnected (Note: this disconnects the pixel array from the ADC!)
	9	ADC test mode. 1=ADC digitizes VAAPIX-AGND 0 = normal operation (default)
	8-6	Skew magnitude control Skew voltage = 100mV * Bit8 + 75mV * Bit7 + 50mV * Bit 6, Default = 010 (75mV)
	5	Skew flip: 1= negative skew 0 = positive skew (default). Note that the sign of the skew is automatically flipped when the calibration value is negative.

Table 7: Black Level Registers (Continued)

REGISTER	BIT	DESCRIPTION
	4	Enable offset voltage DAC 1= enable DAC (default) 0 = disable DAC (Offset Correction Voltage = 0.0V)
	3	Enable skew DAC. 1= enable skew DAC (default) 0 = disable skew DAC (Skew Voltage = 0.0V)
	2-1	Force/disable black level calibration 00 = apply black level calibration during ADC operation only (default). 10 = apply black level calibration continuously X1= disable black level correction (Offset Correction Voltage = Skew Voltage = 0.0V) (In this case, no black level correction is possible.)
	0	Bit 0: Manual override of black level correction 1 = Override automatic black level correction with programmed values 0 = normal operation (default)
Reg0x60, Reg0x61, Reg0x63, Reg0x64		These registers contain the 9-bit signed black level calibration values for the 4 colors in the Bayer pattern. In normal operation, these values are calculated at the beginning of each frame. However, if Reg0x62, bit 0 is set to 1, these registers can be written to, overriding the automatic black level calculation. This feature can be used in conjunction with readout of the black rows (Reg0x20, bit 11) if the user would like to use an external black level calibration circuit. The offset correction voltage is generated according to the following formula: Offset Correction Voltage = (9-bit signed calibration value, -256 to 255) x (2mV + 1mV x Extend bit) x Enable bit Skew Voltage = (+1 - 2 x (calibration bit 9)) x (-1 + 2 x (flip skew bit)) x (Enable skew bit) x (50mV x sw0 + 75mV x sw1 +100mV x sw2) ADC input voltage = Pixel Output Voltage x Analog Gain - Offset Correction Voltage + Skew Voltage

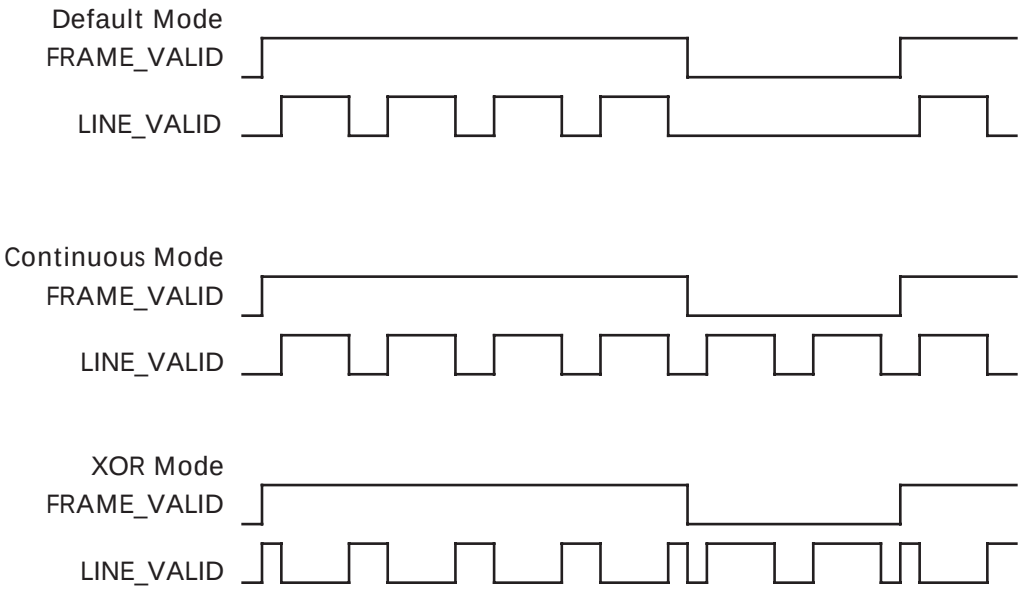
Pixel Clock Speed

The pixel clock speed is set by Reg0x0A. The pixel clock period will be the number set plus two master clock cycles. The default value is 0, which is equal to 2 master clock cycles. With a master clock frequency of 27 MHz the PIX_CLK frequency will be 13.5 MHz.

Line Valid Signal

By setting Bit 9 and 10 of Reg0x20 the line valid signal can get three different output formats. The output formats are shown in Figure 16 when reading out 4 rows and 2 vertical blanking rows. In the last mode, the line valid signal is the XOR between the continuous mode line valid signal and the frame valid signal.

Figure 16: Different Line Valid Formats



Electrical Specifications

Recommended Die Operating Temperature: -20°C to +40°C

Table 8: DC Electrical Characteristics

(Vpwr = 2.8 ± 0.25V; T_A = 25°C)

SYMBOL	DEFINITION	CONDITION	MIN	TYP	MAX	UNIT
V_{IH}	Input High Voltage		Vpwr -0.3		Vpwr+0.3	V
V_{IL}	Input Low Voltage		-0.3		0.8	V
I_{IN}	Input Leakage Current	No Pull-up Resistor; Vin = Vpwr or Vgnd	-15		15	µA
V_{OH}	Output High Voltage		Vpwr-0.2			V
V_{OL}	Output Low Voltage				0.2	V
I_{OH}	Output High Current				20	mA
I_{OL}	Output Low Current				28	mA
I_{OZ}	Tri-state Output Leakage Current				15	µA
$I_{PWR}A$	Analog Quiescent Supply Current	Default settings	8.5	9.6	10.7	mA
$I_{PWR}D$	Digital Quiescent Supply Current	CLK_IN = 27 MHz; default setting, Cload = 10pF	4.8	5.1	5.4	mA
$I_{PWR}A$ Standby	Analog Standby Supply Current Current	STDBY=V_{DD}	0.0	0.5	5	µA
						µA
$I_{PWR}D$ Standby	Digital Standby Supply Current with Clock Off	STDBY=V_{DD}, CLK_IN = 0 MHz	0.0	0.5	5	µA
$I_{PWR}D$ Standby	Digital Standby Supply with Clock On	STDBY=V_{DD}, CLK_IN=27 MHz	0.0	32	50	µA

Table 9: AC Electrical Characteristics

(Vpwr = 2.8 ± 0.25V; T_A = 25°C)

SYMBOL	DEFINITION	CONDITION	MIN	TYP	MAX	UNIT
Tplh	Output propagation delay (Data output propagation delay for low to high transition)	Cload = 10pF		7.5		ns
Tphl	Output propagation delay (Data output propagation delay for high to low transition)	Cload = 10pF		7.5		ns

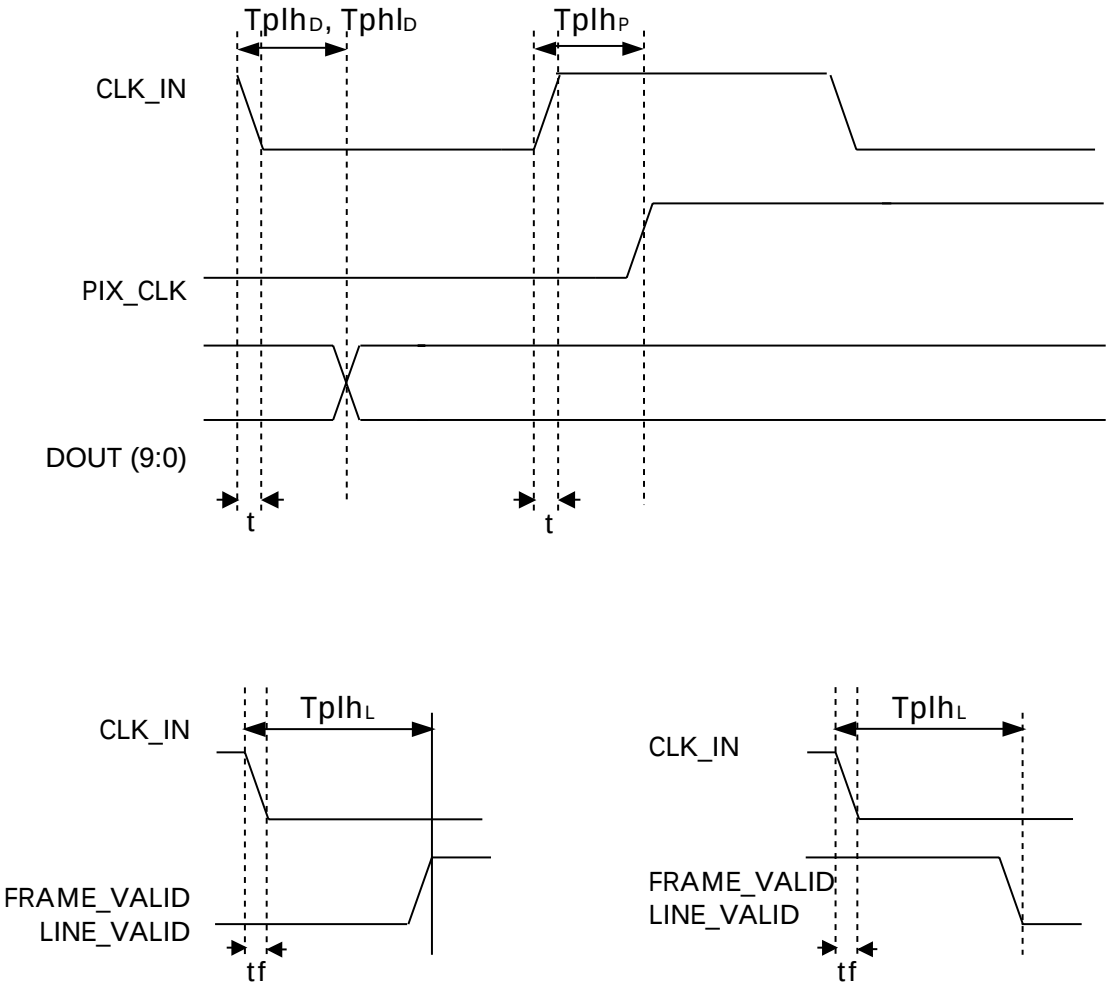
Propagation Delay for Frame Valid and Line Valid Signals

The typical output delay, relative to the master clock edge, is 7.5 ns. Note that the data outputs change on the falling edge of the master clock, with the pixel clock rising on the subsequent rising edge of the master clock.

The line valid and frame valid signals change on the same falling master clock edge as the data output. The line valid goes high on the same falling master clock edge as the output of the first valid pixel's data and returns low on the same master clock falling edge as the end of the output of the last valid pixel's data.

As shown in the Output Data Format and Timing section, frame valid goes high 114 pixel clocks prior to the time that the first line valid goes high. It returns low at a time corresponding to (Horizontal Blank register - 7 pixel clocks) after the last line valid goes low.

Figure 17: Propagation Delays for Frame Valid and Line Valid Signals



Two-Wire Serial Bus Timing

The two-wire serial bus operation requires certain minimum master clock cycles between transitions. These are specified in the following diagrams in master clock cycles.

Figure 18: Serial Host Interface Start Condition Timing

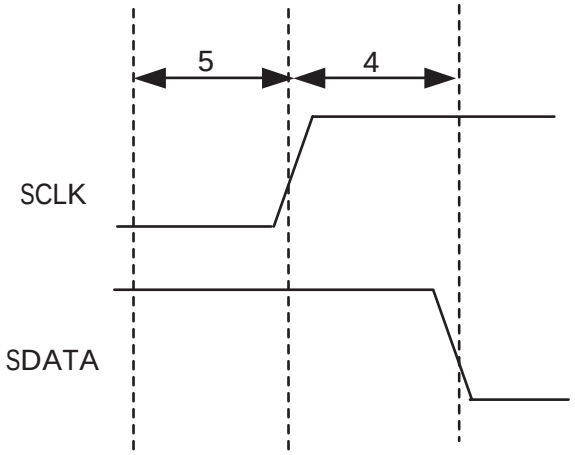
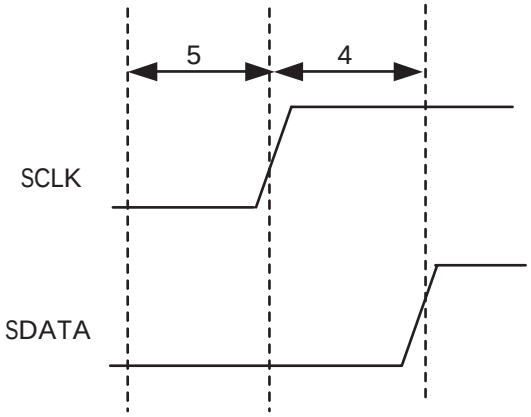
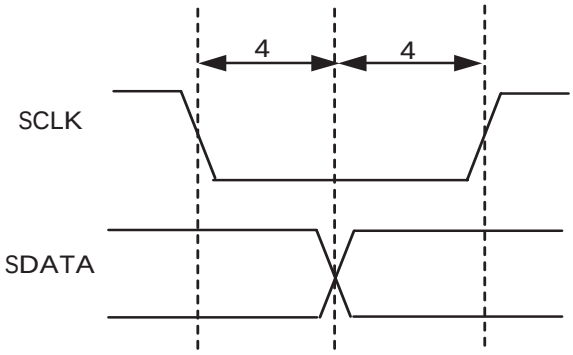


Figure 19: Serial Host Interface Stop Condition Timing



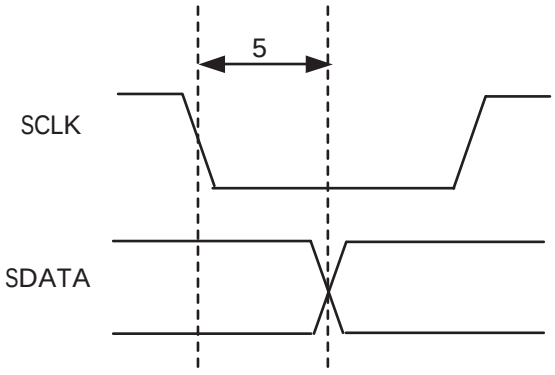
NOTE: All timing in units of master clock cycle

Figure 20: Serial Host Interface Data Timing for Write



NOTE: SDATA is driven by off-chip transmitter

Figure 21: Serial Host Interface Data Timing for Read



NOTE: SDATA is pulled low by sensor or allowed to pull high by pull-up resistor off-chip

Figure 22: Acknowledge Signal Timing After an 8-bit Write to the Sensor

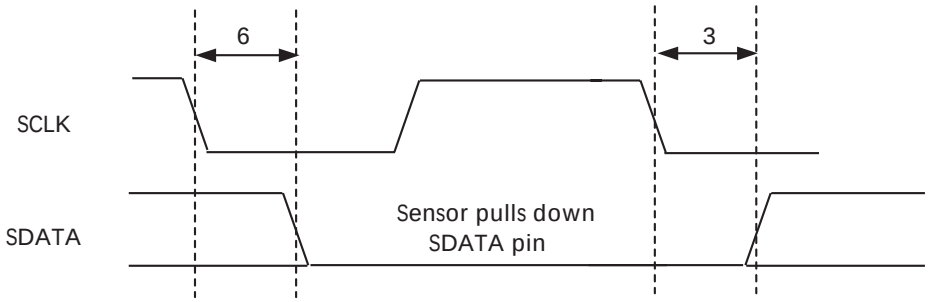
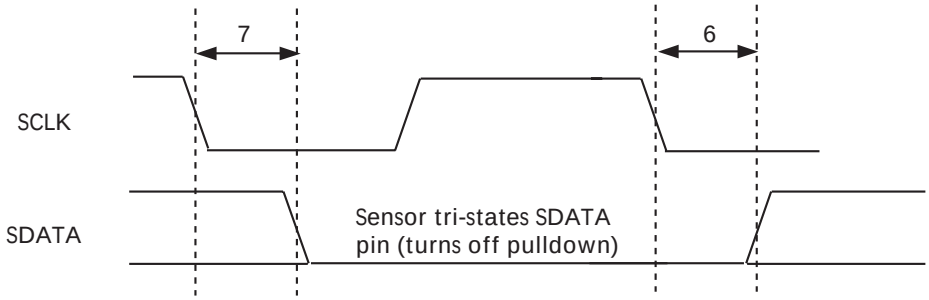


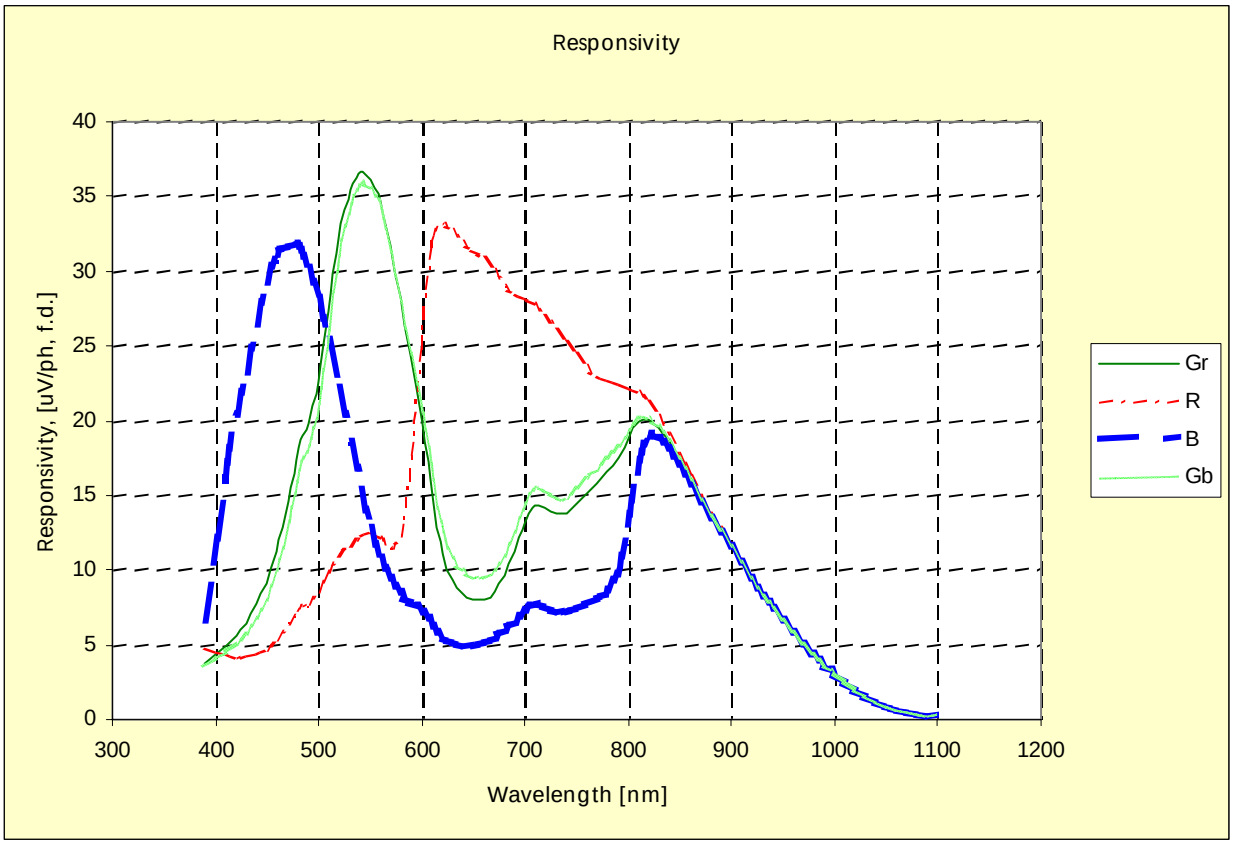
Figure 23: Acknowledge Signal Timing After an 8-bit Read From the Sensor



NOTE:

After a read, the master receiver must pull down SDATA to acknowledge receipt of data bits. When read sequence is complete, the master must generate a no acknowledge by leaving SDATA to float high. On the following cycle a start or stop bit may be used.

Figure 24: Spectral Response



Die Data

Figure 25: Die Layout

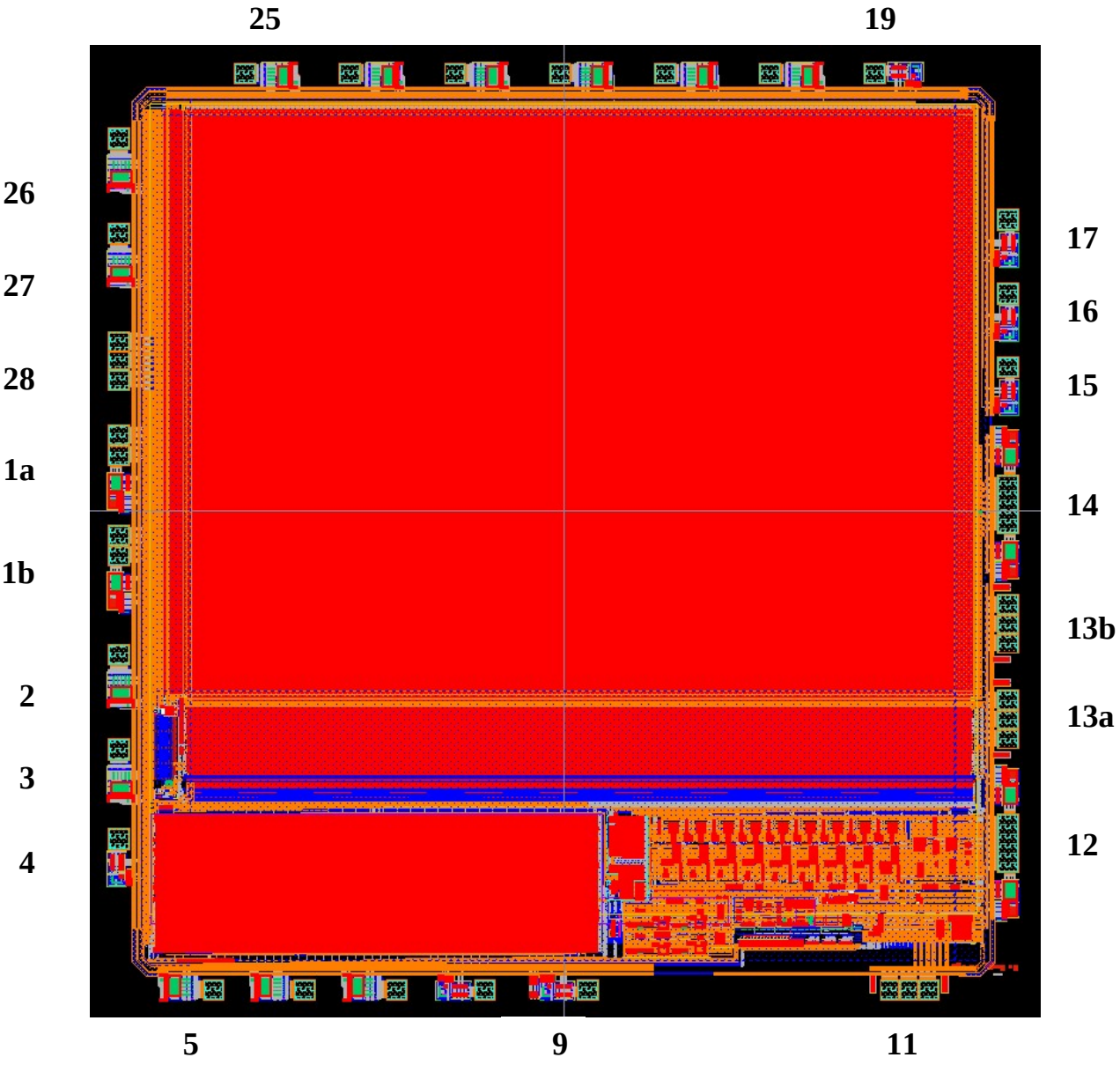


TABLE 10 Optical Area

OPTICAL AREA	PIXEL	X-DIMENSION	Y-DIMENSION
	(first pixel is 0,0)	X	Y
VGA	First Active Pixel, Bottom Left of Pixel Array (20,8)	331.05	270.04
	Last Active Pixel, Top Right of Pixel Array (660,488)	3915.05	2958.4
	Optical Center	2123.05	1614.22
Chip Size, mm	(Including Seal Ring)	4.375	4.693
	(Including Scribe)	4.500	4.910

TABLE 11 Pad Descriptions/Location Die

PAD #	PAD NAME	X POSITION CENTER, µM	Y POSITION CENTER, µM	PAD OPENING SIZE µM
1a	VDD (Digital Power)	4285.00	1815.50	180 (2x)
1b	VDD (Digital Power)	4285.00	2290.50	180 (2x)
2	D1	4285.00	2810.50	90
3	D0	4285.00	3260.50	90
4	Master Clock	4285.00	3685.50	90
5	Pixel Clock	3833.81	4403.00	90
6	Frame Valid	3400.01	4403.00	90
7	Line Valid	2961.71	4403.00	90
8	SCLK	2541.71	4403.00	90
9	SDATA	2050.56	4403.00	90
11	AGND (Analog Ground)	519.54	4403.00	270 (3x)
12	Vaa (Analog Power)	50.00	3706.35	270 (3x)
13a	AGND (Analog Ground)	50.00	3117.40	270 (3x)
13b	AGND (Analog Ground)	50.00	2664.20	270 (3x)
14	Vaapix (Pixel Power)	50.00	2096.35	270 (3x)
15	Scan Enable	50.00	1444.55	90
16	Reset Bar	50.00	1094.55	90
17	Standby	50.00	744.55	90
19	Output Enable Bar	684.05	50.00	90
20	D9	1184.05	50.00	90
21	D8	1684.05	50.00	90
22	D7	2184.05	50.00	90
23	D6	2684.05	50.00	90
24	D5	3184.05	50.00	90
25	D4	3684.05	50.00	90
26	D3	4285.00	360.50	90
27	D2	4285.00	810.50	90
28	DGND (Digital Ground)	4285.00	1415.50	270 (3x)

NOTE:

In packaged samples, pins 1a and 1b are tied together and pins 13a and 13b are tied together.

Figure 26: Image Center Offset

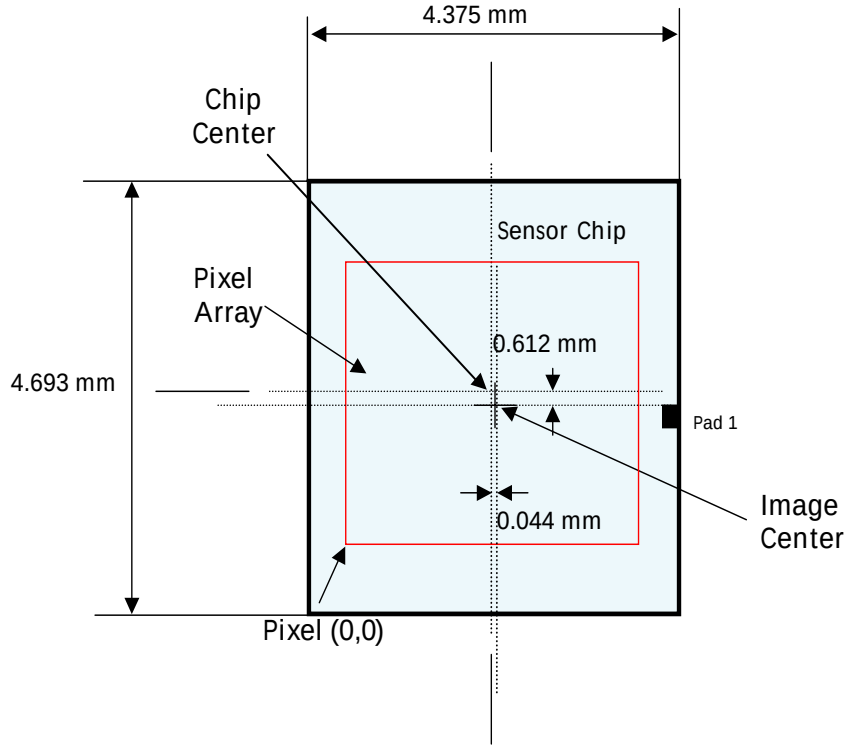


Figure 27: Die Placement

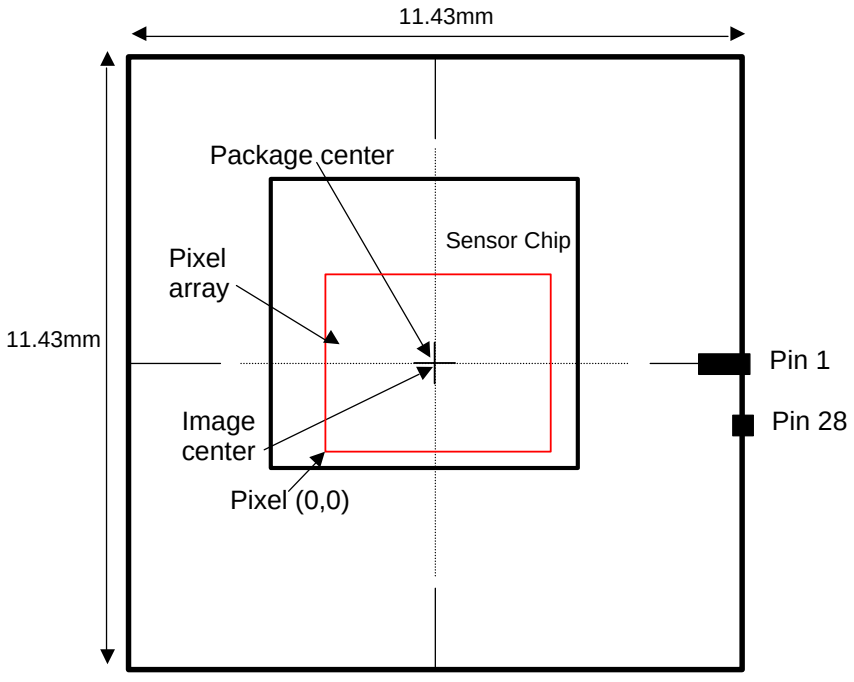
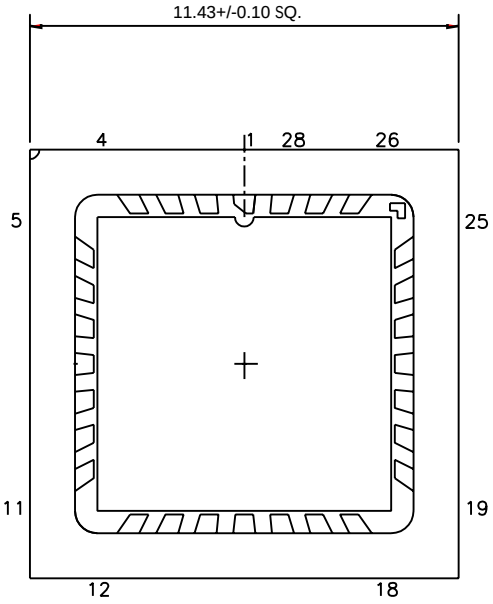


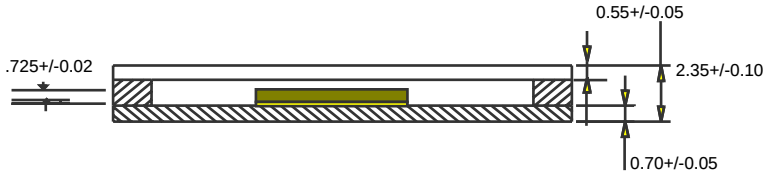
Image Center = Package Center

Figure 28: Package Mechanicals

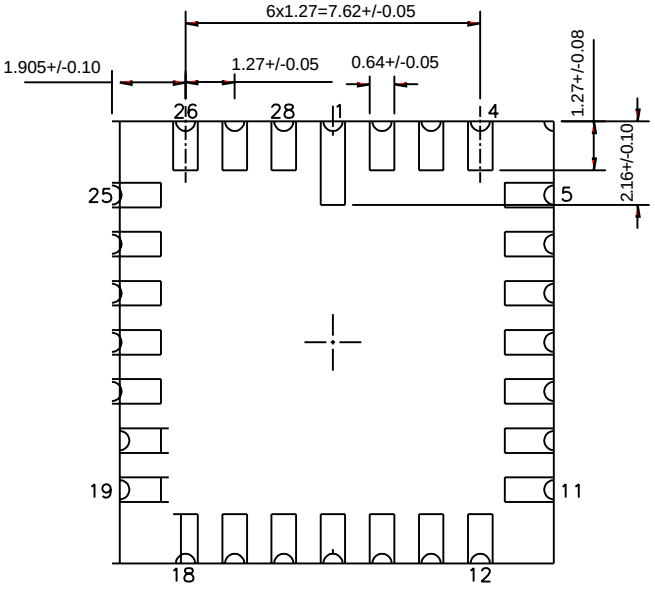
Top View



Side View



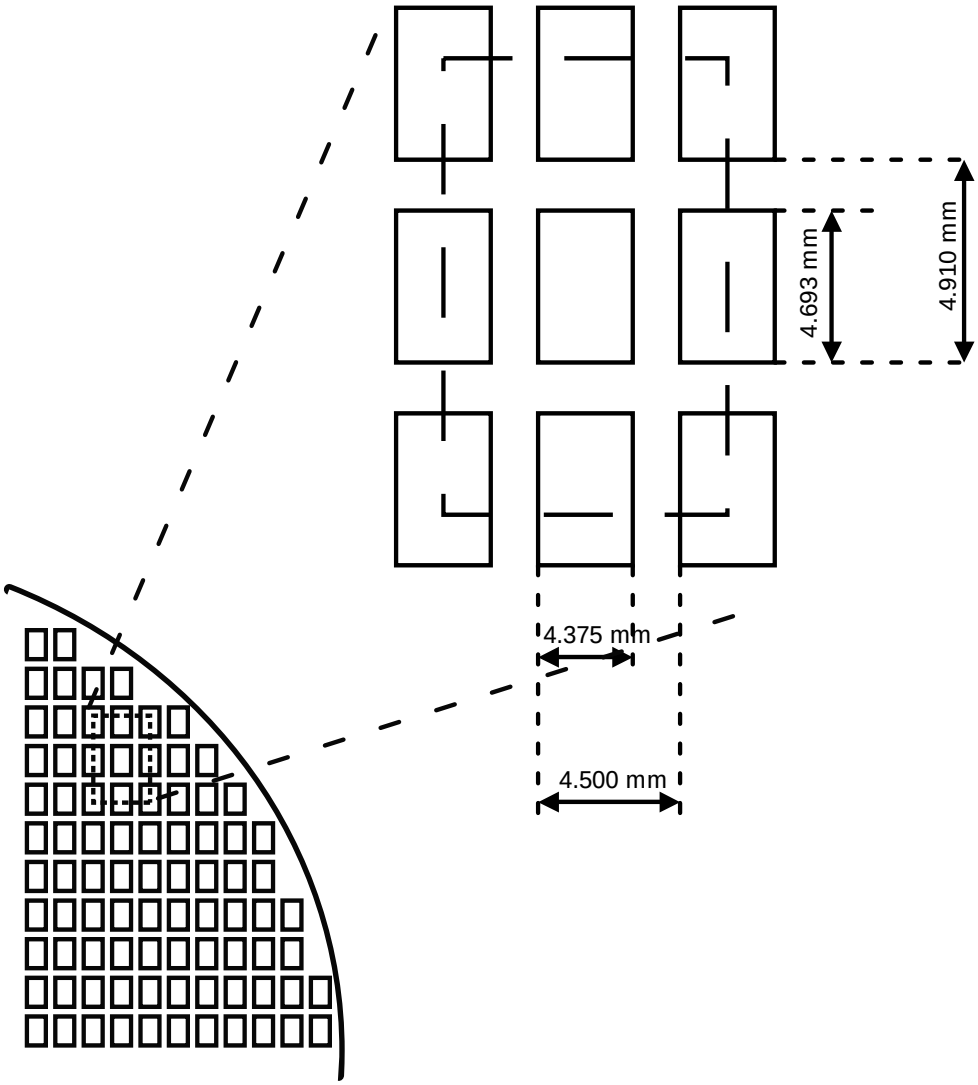
Bottom View



Wafer Dicing Instructions

The primary method of shipping for the MT9V043 is in wafer format. The die size is 4.375mm x 4.693mm, not including scribe lines. The actual width of the vertical scribe line is 0.125mm. The actual width of the horizontal scribe line is 0.217mm. The chip-to-chip spacing is, therefore, 4.500mm x 4.910mm.

Figure 29: Wafer Dicing



Specification of Sensor Quality

A sensor shall be considered “good and billable” if it meets or exceeds the following criteria as determined by Micron during outgoing inspection.

1. The sensor passes the electrical specifications set forth in the MT9V043 product data sheet.
2. The sensor passes the pixel defect specification set forth herein.

Table 12: Example of a Cluster Defect: In the 3 x 3 Array

R11	G12	R13
G21	B22	G23
R31	G32	R33

Defect Specification

Point defect is defined as - Any pixel that produces an electrical signal that does not vary with illumination or any pixel that produces an electrical signal that is 10% above or below the local mean of the same color of a 13 x 13 array at 50% ADC range.

Cluster defect is defined as - Any two point defect pixels of the same color within a 3 x 3 array.

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