

**Video output amplifier****TDA6101Q****FEATURES**

- High bandwidth and high slew rate
- No external heatsink required
- Black-current measurement output for Automatic Black-current Stabilization (ABS)
- Two cathode outputs; one for DC currents, and one for transient currents
- A feedback output separated from the cathode outputs
- Internal protection against positive appearing Cathode-Ray Tube (CRT) flashover discharges
- ESD protection
- Simple application with a variety of colour decoders
- Differential input with a designed maximum common mode input capacitance of 3 pF, a maximum differential mode input capacitance of 0.5 pF and a differential input voltage temperature drift of 20  $\mu\text{V}/\text{K}$
- Defined switch-off behaviour.

**GENERAL DESCRIPTION**

The TDA6101Q is a video output amplifier with 9 MHz bandwidth. The device is contained in a single in-line 9-pin medium power (DBS9MPF) package, using high-voltage DMOS technology, intended to drive the cathode of a colour CRT.

**QUICK REFERENCE DATA**

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{DDH}$	high level supply voltage		0	–	250	V
$V_{DDL}$	low level supply voltage		0	–	14	V
$I_{DDH}$	quiescent high voltage supply current	$V_{oc} = 0.5V_{DDH}$	3.5	4.4	5.5	mA
$I_{DDL}$	quiescent low voltage supply current	$V_{oc} = 0.5V_{DDH}$	2.2	2.8	3.5	mA
$V_I$	input voltage		0	–	$V_{DDL}$	V
$V_{oc}, V_{fb}$	output voltage		$V_{DDL}$	–	$V_{DDH}$	V
$T_{stg}$	storage temperature		–55	–	+150	$^{\circ}\text{C}$
$T_{amb}$	operating ambient temperature		–20	–	+65	$^{\circ}\text{C}$

**ORDERING INFORMATION**

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA6101Q	DBS9MPF	plastic DIL-bent-SIL medium power package with fin; 9 leads	SOT111-1

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BLOCK DIAGRAM

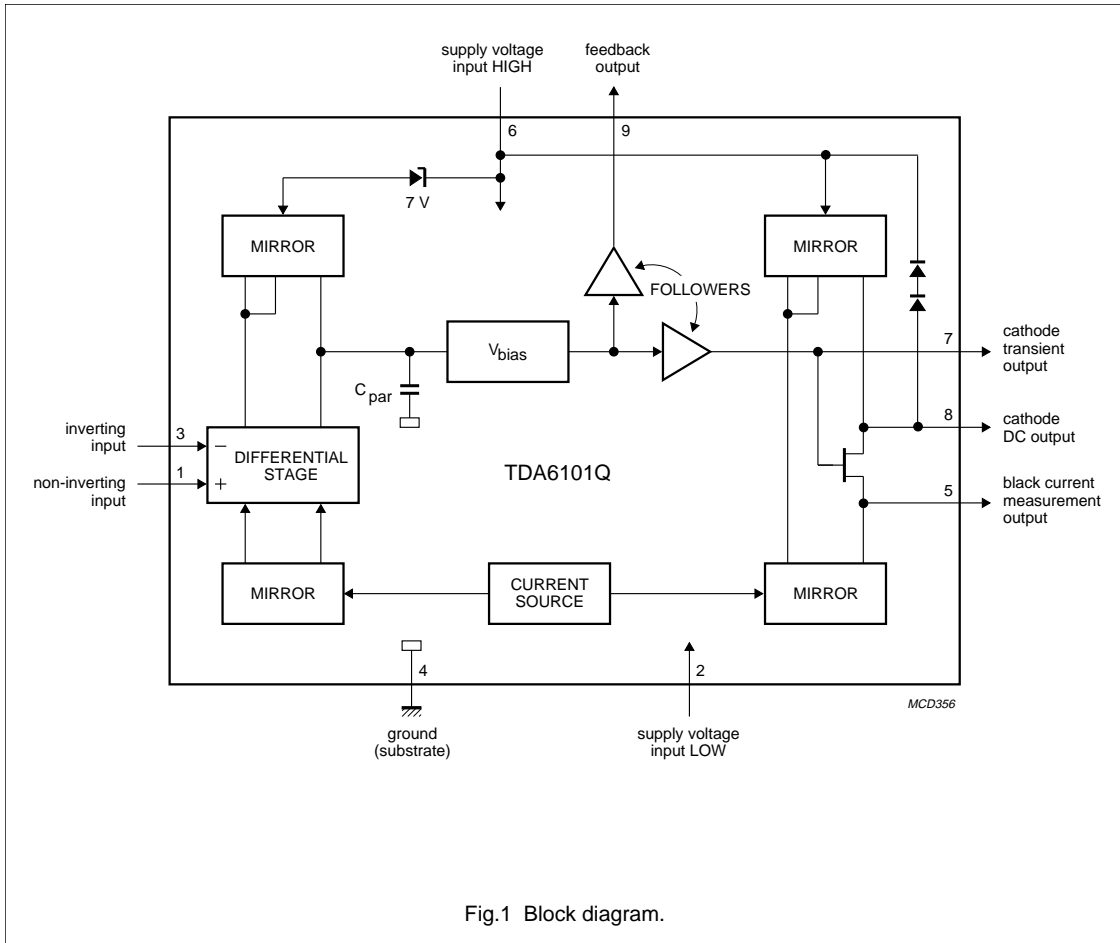


Fig.1 Block diagram.

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## PINNING

SYMBOL	PIN	DESCRIPTION
$V_{ip}$	1	non-inverting voltage input
$V_{DDL}$	2	supply voltage LOW
$V_{in}$	3	inverting voltage input
GND	4	ground, substrate
$I_{om}$	5	black current measurement output
$V_{DDH}$	6	supply voltage HIGH
$V_{cn}$	7	cathode transient voltage output
$V_{oc}$	8	cathode DC voltage output
$V_{fb}$	9	feedback voltage output

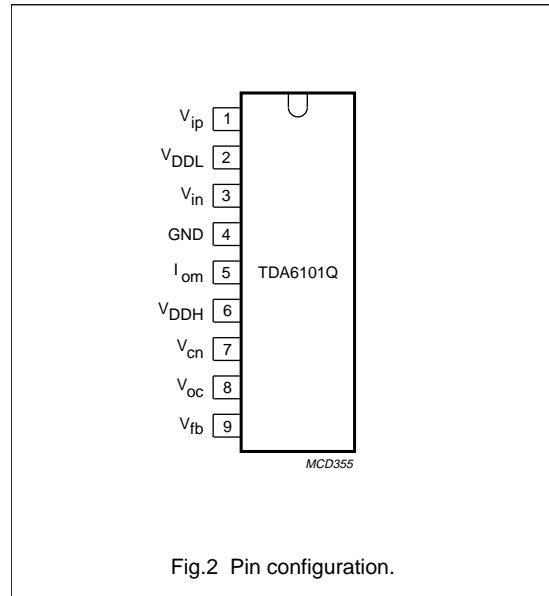


Fig.2 Pin configuration.

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**LIMITING VALUES**

In accordance with the Absolute Maximum Rating System (IEC 134). Voltages measured with respect to GND (pin 4); currents as specified in Fig.1; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V <sub>DDH</sub>	high level supply voltage		0	250	V
V <sub>DDL</sub>	low level supply voltage		0	14	V
V <sub>I</sub>	input voltage		0	V <sub>DDL</sub>	V
V <sub>Idm</sub>	differential mode input voltage		-6	+6	V
V <sub>om</sub>	measurement output voltage		0	V <sub>DDL</sub>	
V <sub>oc</sub>	cathode output voltage		V <sub>DDL</sub>	V <sub>DDH</sub>	V
V <sub>fb</sub>	feedback output voltage		V <sub>DDL</sub>	V <sub>DDH</sub>	V
I <sub>in</sub> , I <sub>ip</sub>	input current		0	1	mA
I <sub>ocsmL</sub>	low non-repetitive peak cathode output current	flashover discharge = 100 µC	0	5	A
I <sub>ocsmH</sub>	high non-repetitive peak cathode output current	flashover discharge = 100 nC	0	10	A
P <sub>tot</sub>	total power dissipation		0	1.9	W
T <sub>stg</sub>	storage temperature		-55	+150	°C
T <sub>j</sub>	junction temperature		-20	+150	°C
V <sub>es</sub>	electrostatic handling				
	human body model (HBM)		-	> 1500	V
	machine model (MM)		-	> 400	V

**HANDLING**

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see "Handling MOS Devices").

**QUALITY SPECIFICATION**

Quality specification "SNW-FQ-611 part E" is applicable, except for ESD Human body model see Chapter "Limiting values", and can be found in the "Quality reference handbook" (ordering number 9398 510 63011).

**THERMAL CHARACTERISTICS**

SYMBOL	PARAMETER <sup>(1)</sup>	VALUE	UNIT
R <sub>th j-a</sub>	thermal resistance from junction to ambient in free air	56	K/W
R <sub>th j-c</sub>	thermal resistance from junction to case	12	K/W

**Note**

- External heatsink not required.

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**CHARACTERISTICS**

Operating range:  $T_{amb} = -20$  to  $65$  °C;  $V_{DDH} = 180$  to  $210$  V;  $V_{DDL} = 10.8$  to  $13.2$  V;  $V_{ip} = 2.6$  to  $5$  V;  
 $V_{om} = 1.4$  V to  $V_{DDL}$ .

Test conditions (unless otherwise specified):  $T_{amb} = 25$  °C;  $V_{DDH} = 200$  V;  $V_{DDL} = 12$  V;  $V_{ip} = 5$  V;  $V_{om} = 6$  V;  $C_L = 10$  pF  
( $C_L$  consists of parasitic and cathode capacitance); measured in test circuit Fig.3.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$I_{DDH}$	quiescent HIGH voltage supply current	$V_{oc} = 0.5V_{DDH}$	3.5	4.4	5.5	mA
$I_{DDL}$	quiescent LOW voltage supply current	$V_{oc} = 0.5V_{DDL}$	2.2	2.8	3.5	mA
$I_{bias}$	input bias current	$V_{oc} = 0.5V_{DDH}$	0	–	20	$\mu$ A
$I_{offset}$	input offset current	$V_{oc} = 0.5V_{DDH}$	–3	–	+3	$\mu$ A
$I_{om(offset)}$	offset current of measurement output	$I_{oc} = 0$ $\mu$ A; $-1.0$ V < $V_{1-3}$ < $1.0$ V; $1.4$ V < $V_{om}$ < $V_{DDL}$	–5	0	+5	$\mu$ A
$\frac{\Delta I_{om}}{\Delta I_{oc}}$	linearity of current transfer	$-10$ $\mu$ A < $I_{oc}$ < $3$ mA; $-1.0$ V < $V_{1-3}$ < $1.0$ V; $1.4$ V < $V_{om}$ < $V_{DDL}$	0.9	1.0	1.1	
$V_{offset}$	input offset voltage	$V_{oc} = 0.5V_{DDH}$	–50	–	+50	mV
$V_{oc(min)}$	minimum output voltage	$V_{1-3} = -1$ V	–	–	20	V
$V_{oc(max)}$	maximum output voltage	$V_{1-3} = -1$ V	$V_{DDH} - 12$	–	–	V
GB	gain-bandwidth product of open-loop gain: $V_{fb} / V_{i, dm}$	$f = 500$ kHz; $V_{ocDC} = 100$ V	–	0.8	–	GHz
$B_S$	small signal bandwidth	$V_{ocAC} = 60$ V (p-p); $V_{ocDC} = 100$ V	7	9	–	MHz
$B_L$	large signal bandwidth	$V_{ocAC} = 100$ V (p-p); $V_{ocDC} = 100$ V	5.5	7	–	MHz
$t_{pd}$	cathode output propagation delay time 50% input to 50% output	$V_{ocAC} = 100$ V (p-p); $V_{ocDC} = 100$ V square wave; $f < 1$ MHz; $t_r = t_f = 40$ ns; see Figs 4 and 5	27	38	49	ns
$t_r$	cathode output rise time 10% output to 90% output	$V_{oc} = 50$ to $150$ V square wave; $f < 1$ MHz; $t_f = 40$ ns; see Fig.4	43	55	68	ns
$t_f$	cathode output fall time 90% output to 10% output	$V_{oc} = 150$ to $50$ V square wave; $f < 1$ MHz; $t_r = 40$ ns; see Fig.5	43	55	68	ns
$t_s$	settling time 50% input to (99% < output < 101%)	$V_{ocAC} = 100$ V (p-p); $V_{ocDC} = 100$ V square wave; $f < 1$ MHz; $t_r = t_f = 40$ ns; see Figs 4 and 5	–	–	350	ns
SR	slew rate between 50 V to 150 V	$V_{1-3} = 2$ V (p-p) square wave; $f < 1$ MHz; $t_r = t_f = 40$ ns	–	1700	–	V/ $\mu$ s

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$O_V$	cathode output voltage overshoot	$V_{ocAC} = 100$ V (p-p); $V_{ocDC} = 100$ V square wave; $f < 1$ MHz; $t_r = t_f = 40$ ns; see Figs 4 and 5; note 1	–	9	–	%
SVRRH	high supply voltage rejection ratio	$f < 50$ kHz; note 2	–	85	–	dB
SVRRL	low supply voltage rejection ratio	$f < 50$ kHz; note 2	–	70	–	dB

**Notes**

1. If the difference between  $V_{DDL}$  and  $V_{ip}$  is less than 7 V, overshoot cannot be specified.
2. SVRR: The ratio of the change in supply voltage to the change in input voltage when there is no change in output voltage.

**Cathode output**

The cathode output is protected against peak currents (caused by positive voltage peaks during high-resistance flash) of 5 A maximum with a charge content of 100  $\mu$ C.

The cathode is also protected against peak currents (caused by positive voltage peaks during low-resistance flash) of 10 A maximum with a charge content of 100 nC.

**Flashover protection**

The TDA6101Q incorporates protection diodes against CRT flashover discharges that clamp the cathode output pin to the  $V_{DDH}$  pin. The DC supply voltage at the  $V_{DDH}$  pin has to be within the operating range of 180 to 210 V to ensure that the Absolute Maximum Rating for  $V_{DDH}$  of 250 V will not be exceeded during flashover. To limit the diode current, an external 820  $\Omega$  carbon high-voltage resistor in series with the cathode output and a 2 kV spark gap are needed (for this resistor-value, the CRT has to be connected to the main PCB). This addition produces an increase in the rise and fall times of approximately 5 ns and a decrease in the overshoot of approximately 3%.

$V_{DDH}$  to GND must be decoupled:

1. With a capacitor  $>20$  nF with good HF behaviour (e.g. foil). This capacitance must be placed as close as possible to pins 6 and 4, but definitely within 5 mm.
2. With a capacitor  $>10$   $\mu$ F on the picture tube base print (common for three output stages).

$V_{DDL}$  to GND must be decoupled:

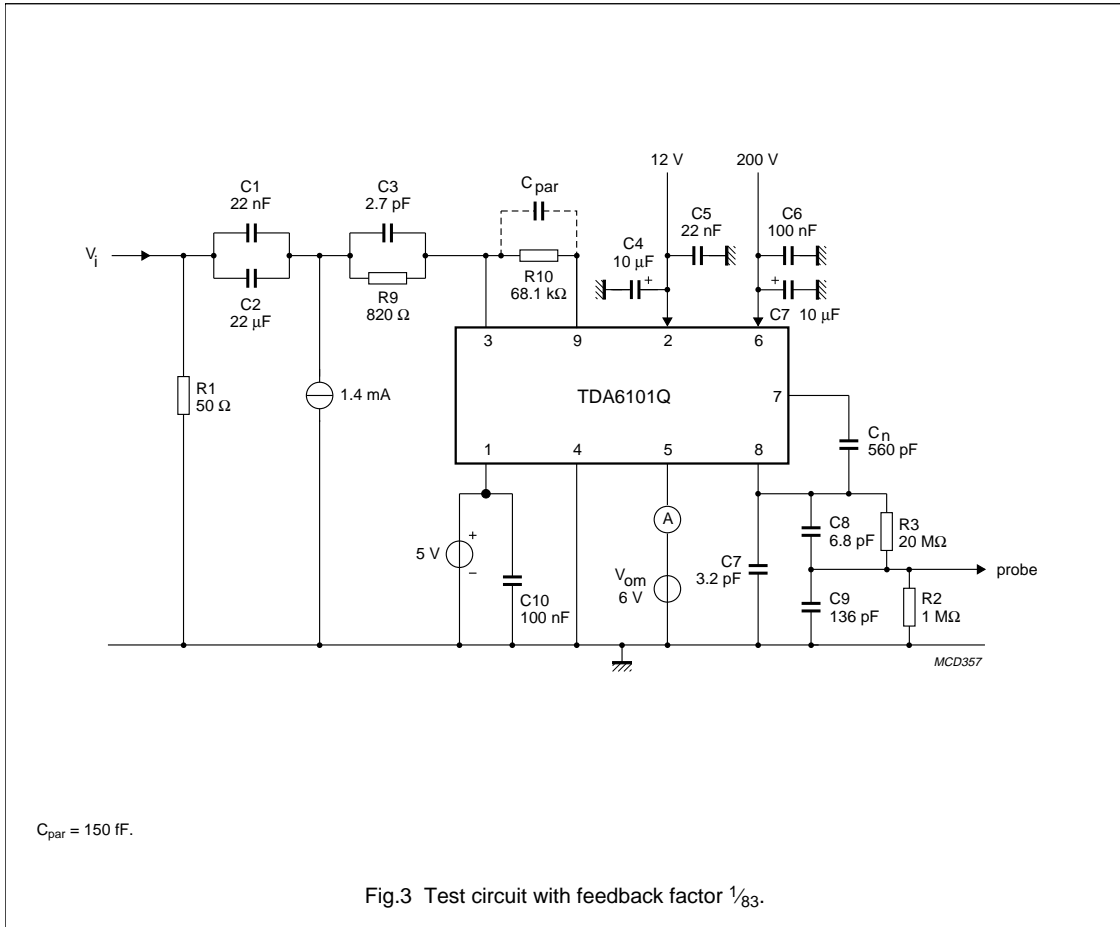
1. With a capacitor  $>20$  nF with good HF behaviour (e.g. ceramic). This capacitance must be placed as close as possible to pins 2 and 4, but definitely within 10 mm.

**Switch-off behaviour**

The switch-off behaviour of the TDA6101Q is defined: when the bias current becomes zero, at  $V_{DDL}$  (pin 2) lower than approximately 5 V, all the output pins (pins 7, 8 and 9) will be high.

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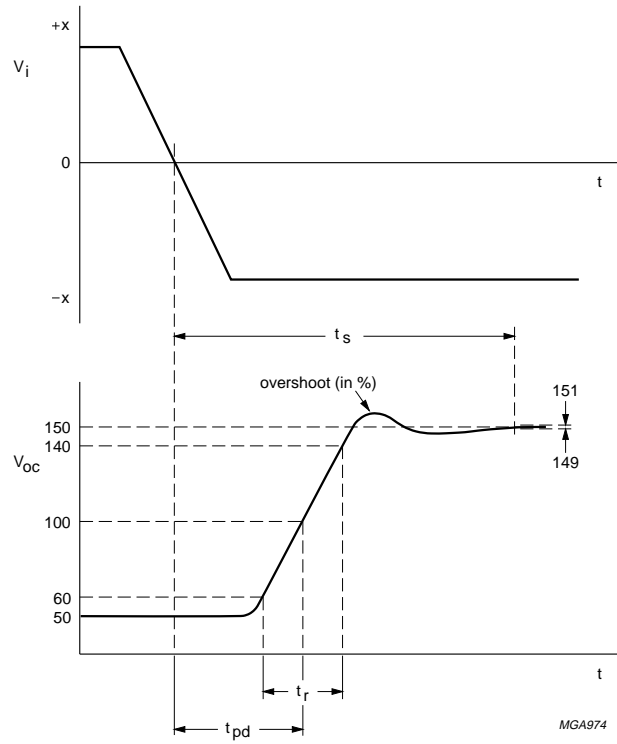


Fig.4 Output voltage (pin 8) rising edge as a function of the AC input signal.



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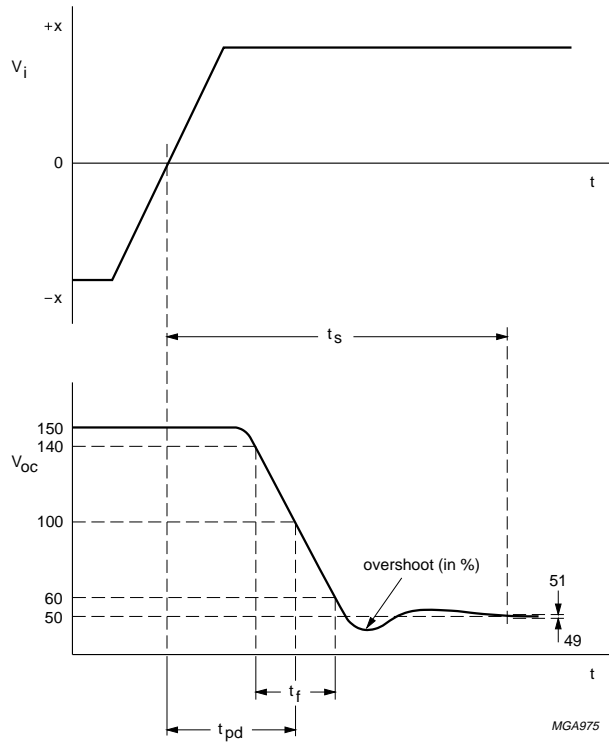


Fig.5 Output voltage (pins 8) falling edge as a function of the AC input signal.

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**TEST AND APPLICATION INFORMATION****Dissipation**

Regarding dissipation, distinction must first be made between static dissipation (independent of frequency) and dynamic dissipation (proportional to frequency).

The static dissipation of the TDA6101Q is due to high and low voltage supply currents and load currents in the feedback network and CRT.

The static dissipation equals:

$$P_{\text{stat}} = V_{\text{DDL}} \times I_{\text{DDL}} + V_{\text{DDH}} \times I_{\text{DDH}} + V_{\text{oc}} \times I_{\text{oc}} - V_{\text{fb}} \times \left( \frac{V_{\text{fb}}}{R_{\text{fb}}} \right)$$

$R_{\text{fb}}$  = value of feedback resistor.

$I_{\text{oc}}$  = DC value of cathode current.

The dynamic dissipation equals:

$$P_{\text{dyn}} = V_{\text{DDH}} \times (C_{\text{L}} + C_{\text{fb}} + C_{\text{int}}) \times f_{\text{i}} \times V_{\text{o(p-p)}} \times \delta$$

$C_{\text{L}}$  = load capacitance.

$C_{\text{fb}}$  = feedback capacitance ( $\approx 150$  fF).

$C_{\text{int}}$  = internal load capacitance ( $\approx 4$  pF).

$f_{\text{i}}$  = input frequency.

$V_{\text{o(p-p)}}$  = output voltage (peak-to-peak value).

$\delta$  = non-blanking duty-cycle ( $\approx 0.8$ ).

The IC must be mounted on the picture tube base print to minimize the load capacitance ( $C_{\text{L}}$ ).